IEEE 802.11
Wireless Access Methods and Physical Layer Specifications

TITLE: Definition of the Transmit and Receive Timing Parameters of the FH PHY Layer

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Introduction

This submission is intended to identify and illustrate the various timing parameters associated with transferring packets of data between two PMD's in a FHSS network. These parameters include some of the physical switching times needed to turn a transceiver into either a transmitter or a receiver, the delay times in placing data bits onto or recovering data bits from the medium, the time required for performing the function of diversity, and others. These parameters help us to define the timings associated with diversity, clear channel assessment (CCA), end-to-end packet delays, and receiver/transmitter delays that make up the complete Rx-to-Tx and Tx-to-Rx turn-around times.

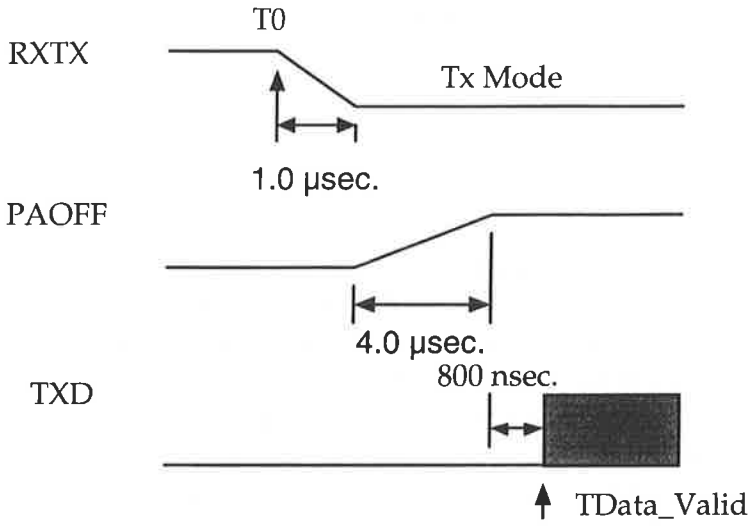
1.0 Transmitter Timing Parameters

1.1 Time for the First Valid Data Bit to Appear on the Medium

Below is an example of how our radio transitions from receive mode into transmit mode on the SAME frequency. The assumptions are that the output frequency of the transmitter has settled to within ± 40 kHz of the center frequency on the desired channel and the first data bit will appear at the output of the transmitter's antenna port at the end of this time:

$$T_{Rx\_Tx} + T_{PAON} + T_{First\_Bit} = T_{Data\_Present}$$

$T_{Data\_Present}$ = 5.8 µseconds **(T_0 = Time when mode change is initiated)**



From the time designated as T_0 (the time at which the command that controls the radio transceiver's actions, initiates the move from Receive mode into Transmit mode) until T_{Data_Valid} (the time at which the first transmitted data bit appears at the output port of the transmitting antenna) the elapsed time is 5.8 µseconds.

1.2 Changing from Tx to Rx for Hopping between Tx Bursts (Apple protocol specific)

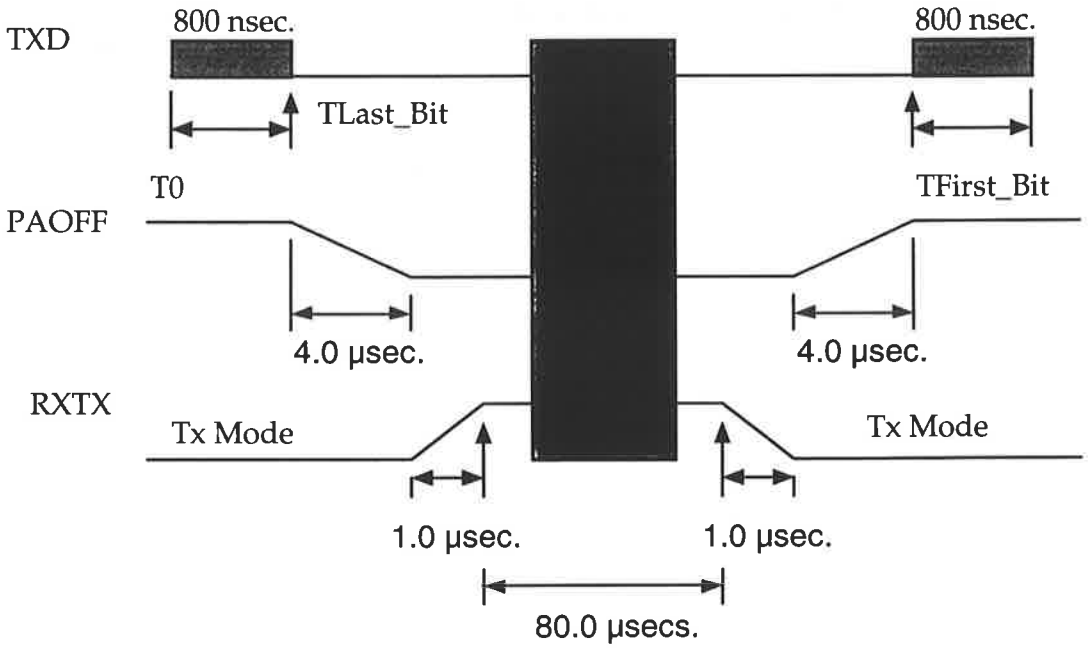
This timing is best described as what happens to the transceiver when transmitting the five bursts of data on each of the selected transmit frequencies per the Apple protocol. The transceiver changes into the receive mode simply as a precaution prior to hopping to the next frequency to insure that the spectrum splatter is minimized during the hopping sequence. It will never actually attempt to recover data while in the receive mode on that frequency, so we are only concerned with the physical switching times needed to change between the two modes. It can be illustrated as follows:

$$T_{Last\_Bit} + T_{PAOFF} + T_{Tx\_Rx} + T_{Hop} + T_{Rx\_Tx} + T_{PAON} + T_{First\_Bit}$$

$T_{Last\_Bit} = T_{First\_Bit} = 0.8$ **µseconds**	(Time for data bit to pass through transmitter)
$T_{PAOFF} = T_{PAON} = 4.0$ **µseconds**	(Time to ramp OFF and ON the PA)
$T_{Tx\_Rx} = T_{Rx\_Tx} = 1.0$ **µseconds**	(Time to physically switch modes in the transceiver)
$T_{Hop} = 80.0$ **µseconds**	(Time to change to the next frequency)

The total time required to complete this process is **91.6 µseconds.**

The assumptions are that the output frequency of the transmitter has settled to within ± 40 kHz of the center frequency of the desired channel and the first data bit will appear at the output of the transmitter's antenna port at the end of this time. The diagram listed below shows the sequence of events for the transmitting unit as it cycles through this process:



2.0 Receiver Timing Parameters

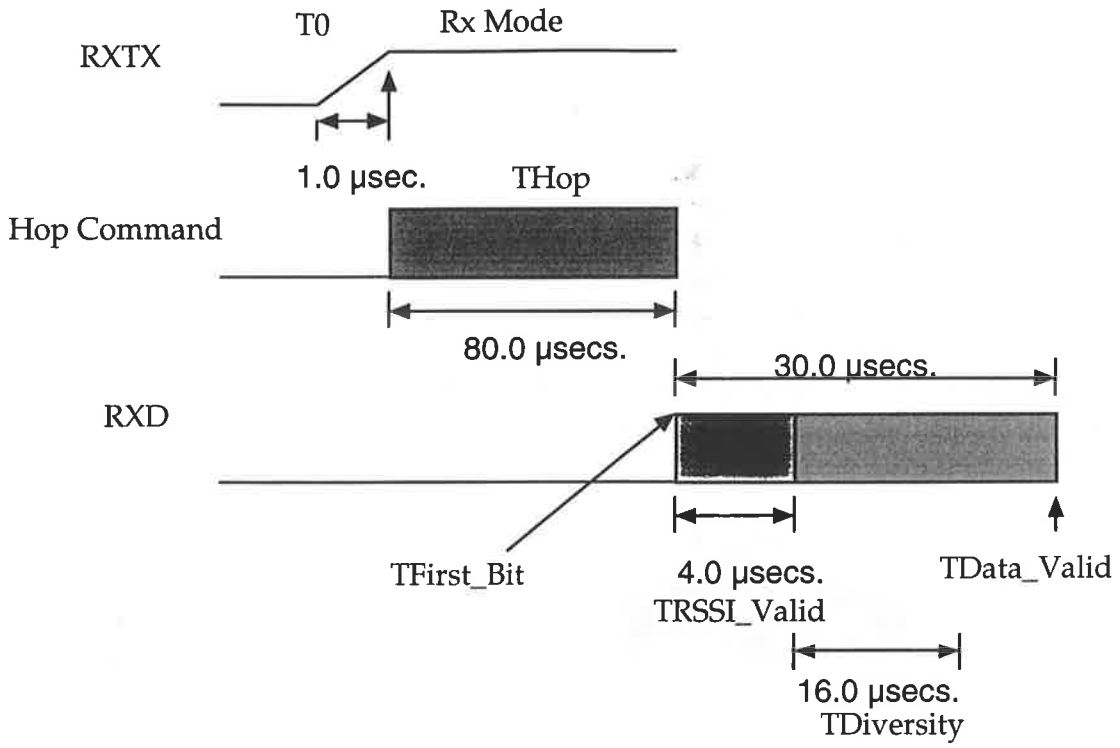
2.1 Changing from Tx to Rx and Preparing to Receive Data:

This timing is best described as what happens to the transceiver after it has completed transmitting the five bursts of data on each of the selected transmit frequencies and needs to turn-around and be ready to begin receiving data on a selected channel. For operation under the DFWMAC, it can be compared to the scan or carrier sense mode of operation, whereby a node that has finished transmitting must begin its clear channel assessment algorithm to determine if there is anything (like an ACK) out on the medium for itself. It can be illustrated as follows:

$T_{Tx\_Rx} + T_{Hop} + T_{RSSI\_Valid} + T_{Diversity}$ (This sequence of events begins after the last bit has exited the transmitter)

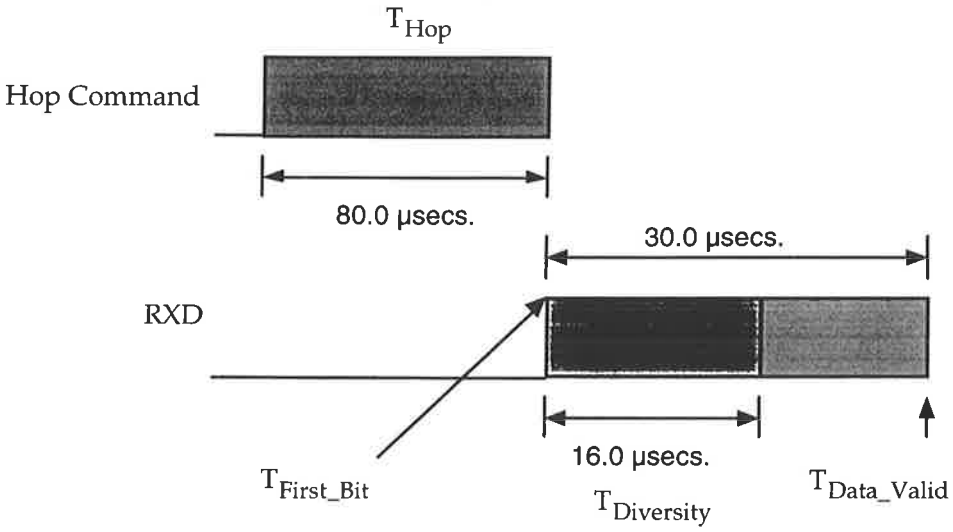
T_{Tx_Rx} = **1.0 µseconds** (Time to physically switch modes in the transceiver)
T_{Hop} = **80.0 µseconds** (Time to change to the next frequency)
T_{RSSI_Valid} = **4.0 µseconds** (Time for energy to build up in the receiver, including any delays)
$T_{Diversity}$ = **16.0 µseconds** (Time to perform diversity and select the correct receive antenna)

The total time required to complete this process is **111.0 µseconds.** The assumptions for these timing requirements are that at the time the first data bit enters the receiver at the selected antenna port, defined as T_{First_Bit}, until the time when the RSSI output is valid for measuring input power level, defined as T_{RSSI_Valid}, is equal to 4.0 µseconds. From this point until the time when the diversity function is completed, defined as $T_{Diversity}$, is 16.0 µseconds. At this point in time, the receiver should be ready to deliver valid data bits to the agreed upon bit mask to the clock recovery circuitry.


T0
Rx Mode
RXTX
1.0 µsec.
THop
Hop Command
80.0 µsecs.
30.0 µsecs.
RXD
TFirst_Bit
4.0 µsecs.
TRSSI_Valid
TData_Valid
16.0 µsecs.
TDiversity

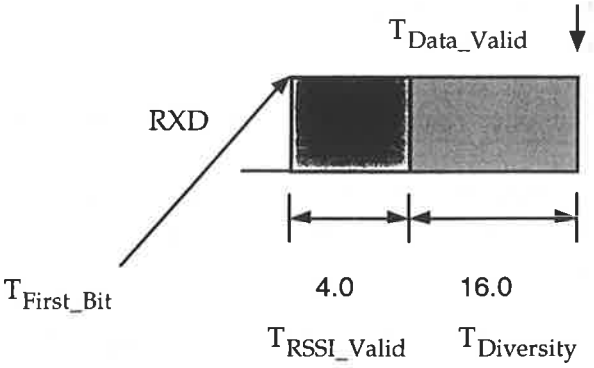
2.2 Scanning or Channel Sensing while in Continuous Receive Mode

This time is best descibed as what happens to the transceiver when it is in a continuous scan or channel sense loop per the DFWMAC, or when the receiver is hopping in synchronization with a transmitter and attempting to recover each of the five transmitted bursts per the Apple protocol. During this action, the receiver performs a diversity measurement on each frequency and needs to provide valid RSSI information and data at the output of the receiver in a determined time frame. For our current implementation, this needs to include the delay time through the receiver and any necessary DC compensation needed to establish valid data bits per the required bit mask specification. These timing requirements are similar to section 2.1 of this document with the physical switching times of T_{Tx_Rx} and T_{RSSI_Valid} removed. This implementation assumes that diversity is performed on energy level only and takes into account the effects of temperature and voltage variations in establishing a valid bit width per the required bit mask specification.



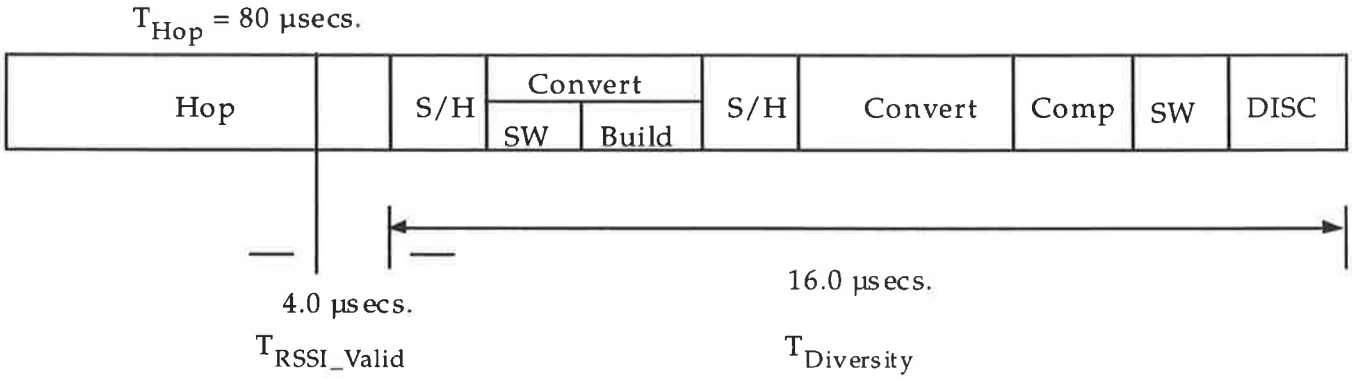
2.3 Switching Antennas for the Diversity Function

This time is related to the receiver's ability to switch antennas after the diversity decision has been made and maintain valid data, to the agreed upon bit mask, at the clock recovery circuitry input. This timing requirement can be described by the following two scenarios. Scenario one is the case where the selected antenna is the last antenna that was sampled during the diversity measurement, and scenario two is the case where the transceiver needs to switch back to the first sampled antenna before attempting to recover the data. In both cases, data needs to be valid at the conclusion of the diversity measurement, whether or not a final antenna switch was required as a result of the diversity function.



(All times are in μseconds)

The diagram below is an illustration of how the diversity function is implemented in the Apple protocol. This measurement only uses energy levels to determine which antenna to use during reception of the next burst of data. Bit synchronization is performed at the conclusion of this time and the receiver begins to look for the appropriate framing symbol. The last instance of the parameter T_{SW} is needed to switch to the first sampled antenna if it is the desired reception path, and the parameter T_{DISC} is needed to allow the receiver to build up with energy after switching states again. It should be noted that the time needed for the data to adjust to the proper bit width per the specified bit mask must be completed by the conclusion of the diversity measurement.



The timing parameters associated with the above diagram are as follows:

1) **S/H:** This is the time required for the charge on the capacitor used to measure the RSSI output voltage to build up. It will take 800 nanoseconds for the charge to be established.

2) **SW:** This is the time required for the diversity switch to change between the two antennas. This will take 500.0 nanoseconds.

3) **Build:** This is the time required for energy to build up in the receiver, referred to earlier as T_{RSSI_Valid}, and is 4.0 μseconds.

4) **Convert:** This is the time required for the A/D to convert the RSSI output voltage reading and store it in a designated register. This is specified as 4.0 μseconds.

5) **Comp:** This is the time required for the ASIC to compare the two readings taken on the antennas and decide which one has the higher value. This is specified at 800 nanoseconds.

6) **DISC:** This can be measured as the time delay from a signal entering either antenna port of the receiver until it can be recovered at the output of the receiver within the defined bit width limits. This is specified as 3.2 μseconds.

$$\mathbf{T_{Diversity} = 2*(S/H) + Convert + Comp + SW + DISC + MAX(Convert, (SW + Build))}$$
$$\mathbf{= 14.6\ \mu seconds.}$$

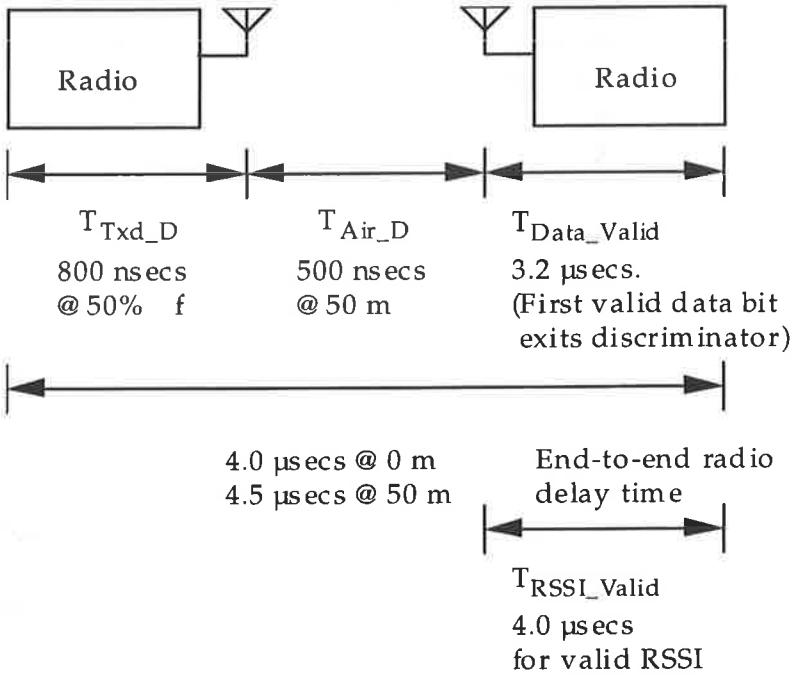
(For implementation purposes, we have chosen 16.0 μsecs. for the Apple protocol)

This assumes that during the last 4.0 μseconds of the hop time that the radio will be sufficiently settled to allow the receiver to build up with energy. This means that the output of the RSSI line will be valid at the instant the first S/H is performed. This is referenced as the diversity start time. Since the bandwidth of the RSSI measurement is roughly equal to the IF bandwidth this assumption is valid. The more stringent settling requirement of ±40.0 kHz, referred to earlier, is not required for energy to begin building up in the receiver.

3.0 System Timing Parameters

The timing diagram listed below is an illustration of the end-to-end delay associated with transferring the first bit of data out of the transmitter, through the medium, and through the intended receiver. The total delay time associated with the Apple protocol is 4.5 μseconds at a distance of 50 meters.

$$T_{Txd\_D} + T_{Air\_D} + T_{Data\_Valid} = T_{End\text{-}to\text{-}end\_Delay}$$



T_{Txd_D} = 800 nsecs. as measured at the 50% point of the input bit symbol to the transmitter. The transmitter converts the voltage of the data bit to a specific frequency (FSK) for transmission. This conversion time is 800 nsecs. and the transmission of the information is almost instantaneous. (This is identical to the terms of T_{First_Bit} and T_{Last_Bit} mentioned in the previous sections).

T_{Air_D} = 500 nsecs. as measured at 50 meter spacing between two transceivers under clear channel conditions. This is defined as (1/C*d), where d is the separation of the two transceivers.

T_{Data_Valid} = 3.2 μsecs. as measured from the input of either antenna port of the receiver to the output of the RXD line from the receiver.

T_{RSSI_Valid} = 4.0 μsecs. as measured from the input of either antenna port of the receiver to the output of the RSSI line from the receiver. This is defined as the time when the RSSI value has reached 90% of its final value for the signal under measurement.

All of the above timing requirements have a direct effect on the network dead time and the overall network throughput and performance. Therefore, it is critical that these numbers be kept to a minimum.

4.0 Conclusions

In understanding the relationship between the transmitter and receiver timing constraints, we will be able to reduce any degradations or errors associated with transferring data between two nodes in a FHSS network. For implementations of diversity and CCA algorithms, it is important to understand that clock recovery and data acquisition want to happen instantaneously after selection of the appropriate antenna or receive path, assuming that these functions are designed with an energy threshold detection mechanism only. Any additional delays for DC compensation or settling in the receiver will reduce that transceiver's ability to acquire the transmitted signal in the shortest time possible, or determine if the medium is available for transmission of data.

In addition, the channel error rate will increase if data bursts are missed or dropped because the turn-around delays are too excessive. These timing delays directly affect the clear channel access (CCA) algorithm because they determine how long a node needs to listen on a channel to determine if it is clear or if data is present.