IEEE P802.11
Wireless Access Methods and Physical Layer Specifications

Title : **GFSK FH-SS Filter Implementation Using Gaussian and Compatible Simpler FQPSK-1 Baseband Filters**

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Abstract

To meet the IEEE 802.11 FH-SS requirements which specify GFSK modulation with BT_b=0.5 [1], we present an FQPSK-1 baseband filter implementation which is practically compatible with Gaussian filters. With ROM look up table implementation of a FQPSK-1 baseband filter, which is based on Feher's filter patent [9], the hardware gate count of the filter can be reduced by a factor greater than 8 compared to a traditional Gaussian FIR-filter design. Computer simulations and hardware measurements of Gaussian filtered FSK (GFSK) and compatible FQPSK-1 baseband filtered FSK (FGFSK) are presented. Eye diagrams and power spectral densities are compared at baseband and RF.

While reducing the number of packed configurable logic blocks (CLB's) needed for the filter in a XILINX-FPGA from 67 to 8, the modulated FGFSK signal still meets the IEEE 802.11 FH-SS spectral requirements for modulation index 0.32.

1. Modulator Block Structure

All examinations in this paper are based on the incoherent VCO-structure for generating (F)GFSK modulated signals. Figure 1 shows the block structures of both FGFSK and GFSK transmitters which were used for simulations and hardware measurements.

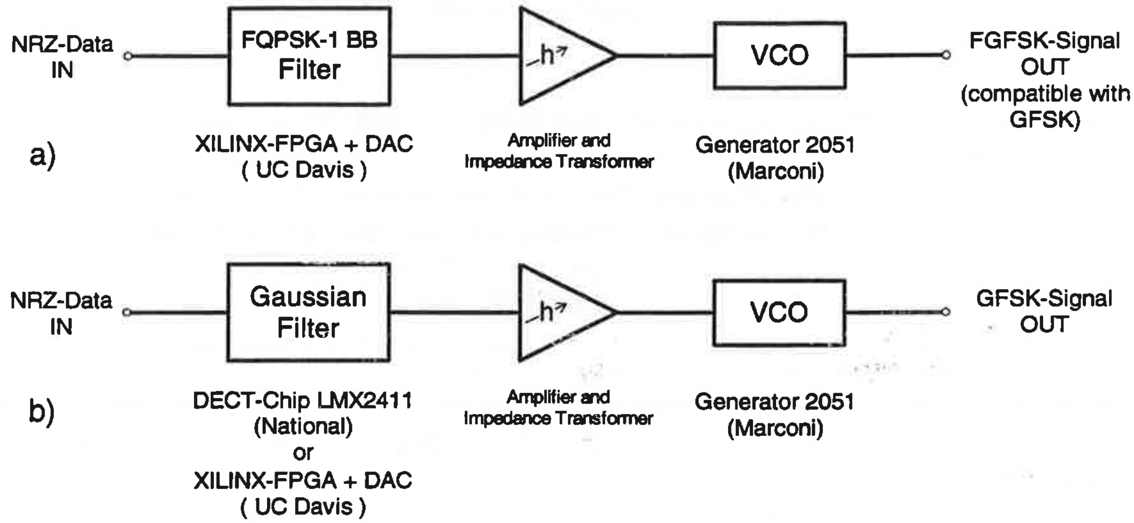

Figure 1. Block diagrams of compared FGFSK-(a) and GFSK-(b) modulator structures

In Figure 1-a the proposed FQPSK-1 baseband filter is used as a premodulation filter for FSK, where Figure 1-b shows the known reference structure with standard Gaussian filter implementations. The FQPSK-1 baseband filter was designed at UC Davis using a XILINX-FPGA which is described in the following section. We use another own FIR-filter design for gate count comparison purposes and the Gaussian baseband filter of National Semiconductor's DECT-Chip LMX2411 for the hardware reference measurements.

2. Filter Implementations

Until the 1980s, designers devoted their attention to "linear" filter implementation means, including analog (passive and active) and Digital Signal Processing (DSP) filters. The DSP filters are based on Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) designs. These "linear transversal filter structures" are in extensive use. They are implemented based on certain transfer function H(z). H(z) is only an approximation of the analog transfer function H(s) with acceptable difference.

Figure 2 shows the frequency response of a Gaussian, BT_b=0.5 FIR-Filter design which was implemented at UC Davis for gate count comparison purposes. From an implementation point of view, the increase of steps means that the number of delays, adders and multipliers is greatly increased, and each multiplier requires many gates. For high speeds such DSP-based filters could be very "power hungry", require far too many gates, be expensive, and go to an impractical range for most of today's communications applications.

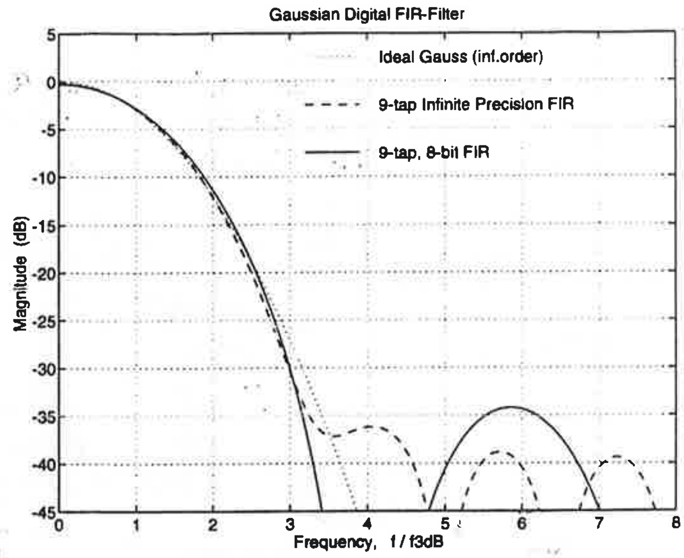

Figure 2. Frequency Response of Gaussian, BT_b=0.5 FIR-Filter Approach with 8-samples per data bit, 9-tap impulse response length, and 8-bit signal resolution

It is hard to reduce the complexity of a FIR or IIR filter, since an increasing inaccuracy comes along with the complexity reduction.

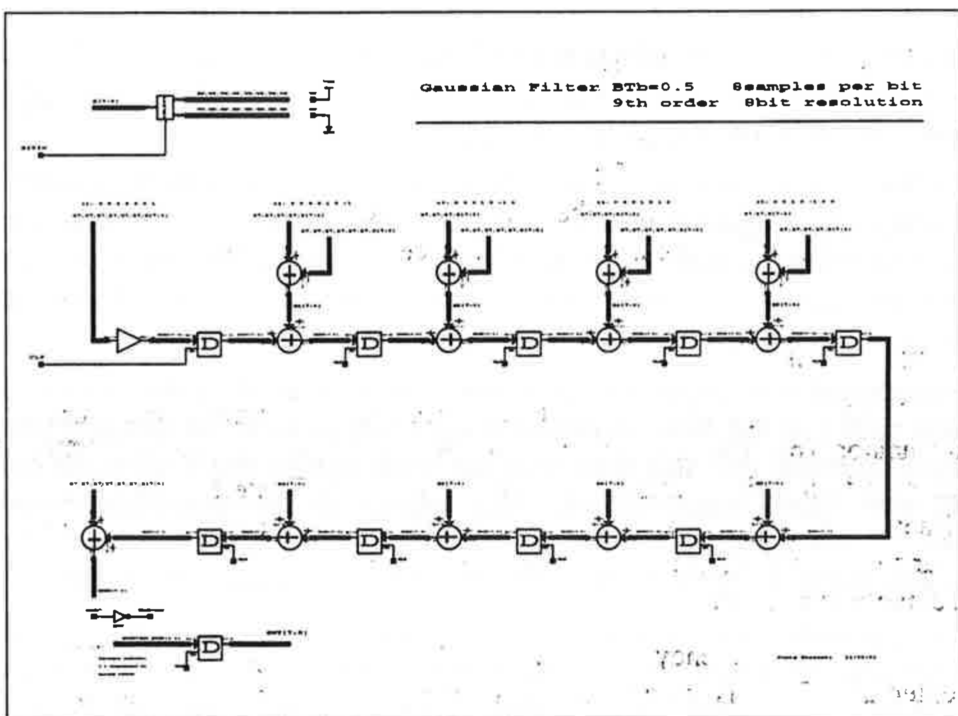

Figure 3. Schematic for the XILINX-FPGA Implementation of Gaussian, BT_b=0.5 FIR-Filter with 8-samples per data bit, 9-tap impulse response length, and 8-bit signal resolution.
The design is used for gate count comparison purposes and is based on [11].

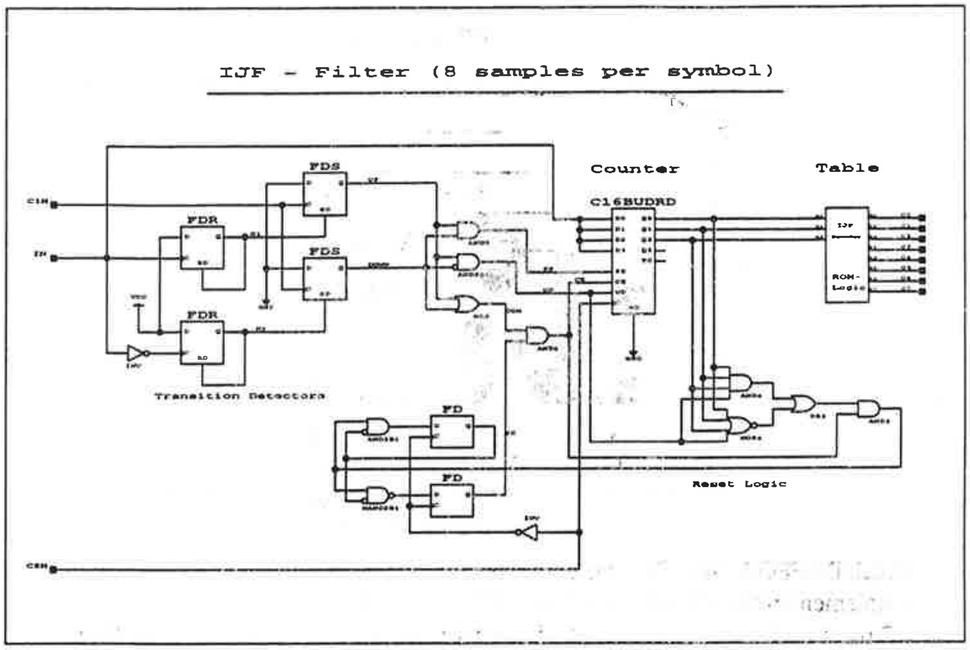

Figure 4. Schematic for the XILINX-FPGA Implementation of ROM Look-up Table based FQPSK-1 Baseband Filter with 8-samples per data bit, 1 bit signal length and 8-bit signal resolution.
This design uses Feher's patented Filter structure [9] and reduces the number of packed CLB's by a factor of about 8 compared to the design Figure 3.

The principles of the more efficient ROM based look-up table implementation of a filter or processor was presented 1979 in [8] and patented 1982 by Dr. Feher [9]. There are many references about it [6,10,12].

Feher's Filter (FF) family products have been implemented with ROM-based DSP architectures. In the ROM various signal shapes, e.g., $s_1(t)$ ..., $s_8(t)$ are stored or it is arranged that the ROM is used as a waveform selector/generator/switch. Depending on the data input, the difference between data patterns, these stored waveforms are "read out" or switched to the D/A converter, converted into an analog waveform and transmitted.

Using this method to implement a linear filter, first truncate the pulse response (or the response to be deal with) of the filter to certain length, and generate all possible combinations , then oversample, quantize and map them with the input signals into a table. As the tail of the pulse response with small magnitude has little impact on the quantified magnitude value, the inaccuracy in this approach is mainly due to the quantization noise which exists in any digital process. This implementation requires a shift register, a counter and a ROM.

The advantage of the look-up table method is its simplicity and, coming together with it, reduced power consumption, which is critical for mobile communication units. Another advantage of the ROM look up table implementation is that it could be further simplified by reducing the memory bits required. The way to do it is further truncation of the response. If it causes an impact bigger than you want, you can modify the wave shape a little bit to reduce the impact without affecting the complexity.

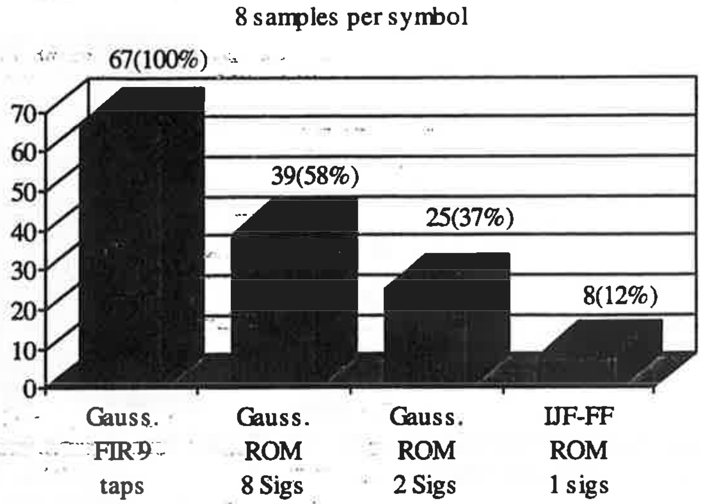

Figure 5. XILINX-FPGA Gate Count Comparison in numbers of packed CLB's for several Filter Implementations.
67 packed CLB's are needed for the Gaussian FIR-Filter Figure 3 and 8 for the FQPSK-1 Baseband Filter Design Figure 4, respectively.

The numbers of packed configurable logic blocks (CLB's) needed in the FPGA-implementations for the Gaussian FIR and the FQPSK-1 baseband (IJF-FF) filter designs are shown in Figure 5. The left column belongs to the Gaussian FIR-filter Figure 3 and the right column to the FQPSK-1 baseband filter implementation Figure 4, respectively. The both columns in the middle of the graph represent two ROM-based Gaussian filter designs, which are described in [15].

The comparison Figure 5 proofs the tremendous hardware complexity reduction of factor 8.4 when using the FQPSK-1 baseband filter instead of a standard Gaussian FIR-filter implementation. 8 packed CLB's are needed (FQPSK-1 BB) instead of 67 (Gaussian FIR). If compared to the best optimized ROM-based Gaussian filter implementation the hardware reduction for the proposed FQPSK-1 baseband filter implementation remains still a factor of 3.1 (25 CLB's vs 8).

3. Transmitter Signal Comparison

Because of its extremely low gate usage in a digital FPGA-filter implementation the FQPSK-1 baseband filter can potentially be used instead of the Gaussian, BT_b=0.5 filters in GFSK for FH-SS Wireless LAN. The eye diagrams and the power spectral densities are very similar, practically the same in both cases.

The simulated and measured eye diagrams of the filter signal outputs are shown in Figure 6 for both Gaussian, BT_b=0.5 filter and FQPSK-1 baseband filter. Both signals are jitter-free at the bit interval changes. The Gaussian, BT_b=0.5 filtered signal has a known slight intersymbol interference (ISI) in the center of the bit interval. The FQPSK-1 filtered signal is totally ISI-free in the center of the bit interval. Neglecting the unessential ISI of the Gaussian, BT_b=0.5 filtered signal the eye diagrams are the same in both cases.

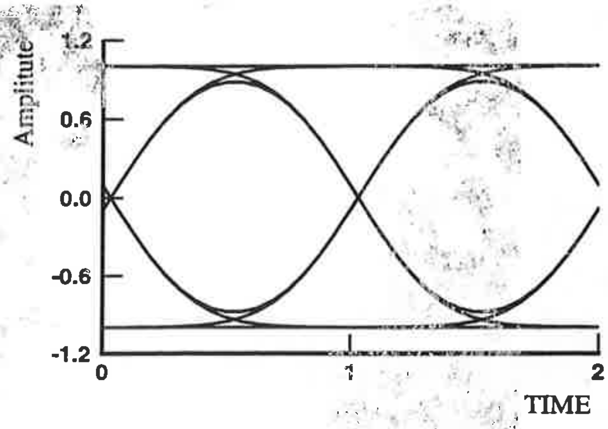

Figure 6(a). Simulated Baseband Eye Diagram after ideal Gaussian, BT_b=0.5 Filter

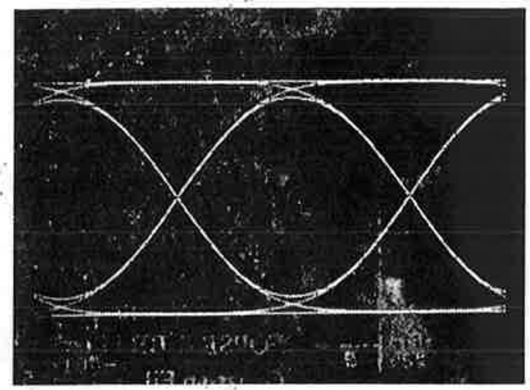

Figure 6(c). Picture of Baseband Eye Diagram after Gaussian, BT_b=0.5 Filter at normalized scaled down bit rate of 40kb/s (measurements were also done at 1Mb/s). DECT-Chip LMX2411 (National); 9 samples/bit; 8 bits resolution

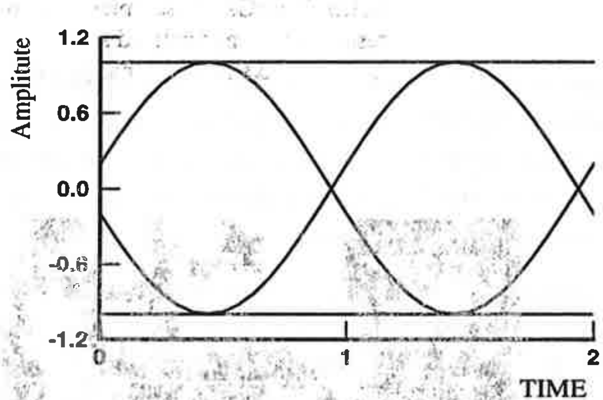

Figure 6(b). Simulated Baseband Eye Diagram after ideal FQPSK-1 Baseband Filter

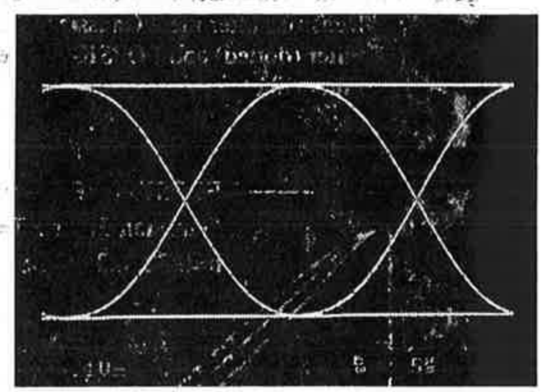

Figure 6(d). Picture of Baseband Eye Diagram after FQPSK-1 Baseband Filter at normalized scaled down bit rate of 40kb/s (measurements were also done at 1Mb/s). XILINX-FPGA (UC Davis); 8 samples/bit; 8 bits resolution

Figure 7 compares the baseband power spectral densities of the Gaussian, BT_b=0.5 and the FQPSK-1 baseband filtered signals in simulation and measurement. As expected, the baseband power spectral density of the Gaussian, BT_b=0.5 filtered signal goes down faster in the main lobe. This is caused by the mentioned ISI. Despite some small difference in the baseband power spectral density the power spectral densities after frequency modulation become nearly the same as shown in Figure 8.

The RF power spectral densities of Gaussian, BT_b=0.5 filtered FSK (GFSK) and FQPSK-1 baseband filtered FSK (FGFSK) in Figure 8-a were simulated for modulation indexes of 0.32, 0.35, 0.38. Figure 8-b shows a picture of the RF power spectral densities for the modulation index 0.32 at 915MHz carrier frequency.

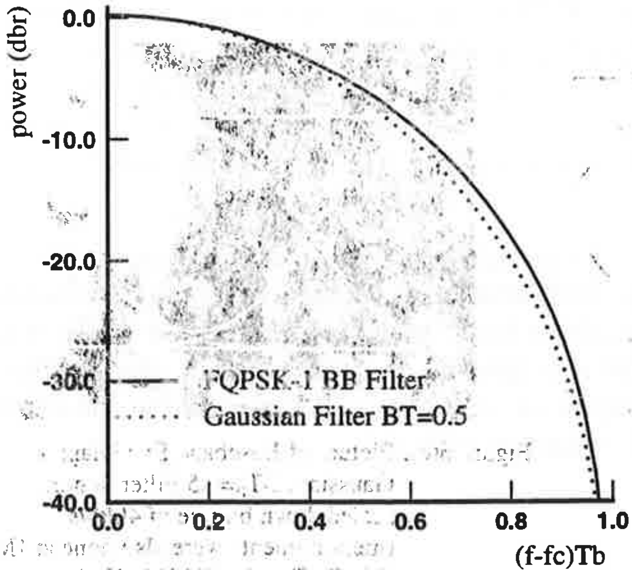

Figure 7(a). Simulated Baseband Power Spectral Densities after ideal Gaussian, BT_b=0.5 Filter (dotted) and FQPSK-1 Baseband Filter (line)

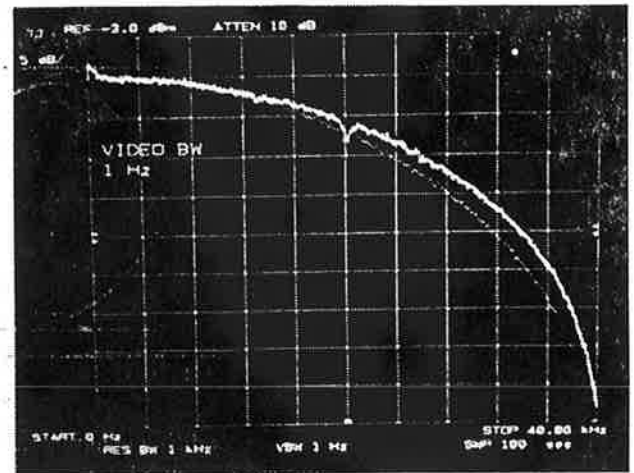

Figure 7(b). Picture of Baseband Power Spectral Densities after Gaussian, BT_b=0.5 Filter (thin curve, DECT-Chip LMX2411; 9 samples/bit; 8 bits resolution) and FQPSK-1 Baseband Filter (light curve, XILINX-FPGA; 8 samples/bit; 8 bits resolution) at normalized scaled down bit rate of 40kb/s (measurements were also done at 1Mb/s).

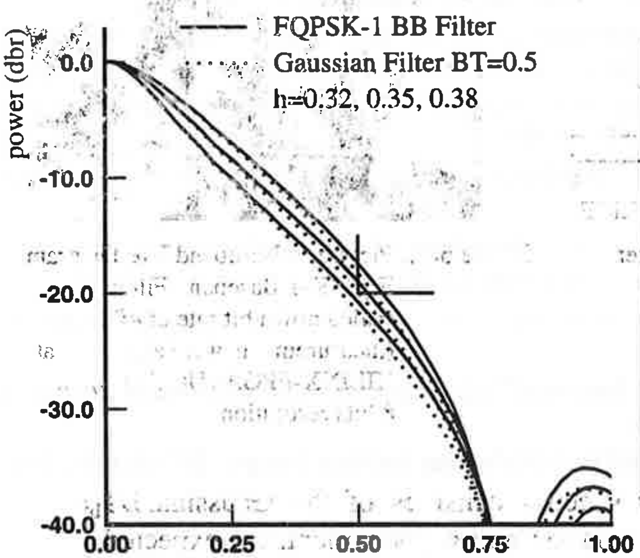

Figure 8(a). Simulated RF Power Spectral Densities with ideal Gaussian, BT_b=0.5 Filter: GFSK (dotted) and FQPSK-1 Baseband Filter: FGFSK (line) for modulation index h=0.32, 0.35, 0.38

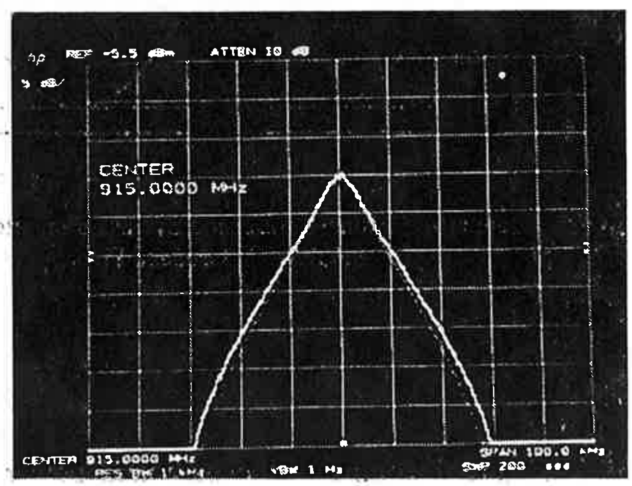

Figure 8(b). Picture of RF Power Spectral Densities with Gaussian, BT_b=0.5 Filter: GFSK (thin curve, DECT-Chip LMX2411; 9 samples/bit; 8 bits resolution) and FQPSK-1 Baseband Filter: FGFSK (light curve, XILINX-FPGA; 8 samples/bit; 8 bits resolution) with h=0.32 at normalized scaled down bit rate of 40kb/s (measurements were also done at 1Mb/s) and a carrier frequency of 915MHz.

Figure 8 demonstrates that both GFSK and FGFSK modulated signals meet the -20dB spectral requirement of the FH-SS proposed standard [1] for modulation index 0.32 (see (f-fc)Tb=0.5 in simulation and 2 divisions from the center frequency in picture). The integrated power within the transmission band ±0.5 (f-fc)Tb was calculated to be 0.9949 times the total power of the proposed FGFSK with modulation index 0.32 and is grater than the demanded 99%.

It is our belief that the ROM-based filter implementation is more cost and power efficient than the conventional IIR and FIR "transversal" DSP structures and leads to significant reduction in gate counts because it does not require multipliers and is based solely on ROM-driven waveform synthesis. Our survey of some leading DSP and filter IC products indicates the trend for higher speed systems is towards the implementation of nonlinearly switched waveform-synthesized filters which are implemented by the ROM technology [13,14].

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