NTT Wireless Systems Laboratories

Hitoshi TAKANASHI
takanasi@pcs.wslab.ntt.co.jp

1-1 Hikarino-oka Yokosuka, Kanagawa Japan
Tel: +81-468-59-3471 Fax: +81-468-55-1172

Background

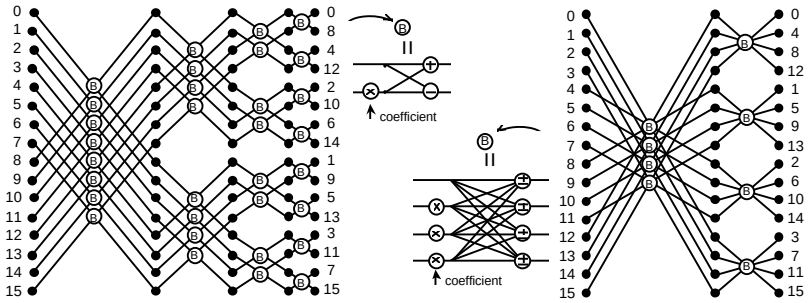
To realize high data rate (≥ 20Mbit/s) wireless LAN modem...

Higher symbol rate —problem→ larger degradation by multipath delay

Multipath countermeasure

Equalizer	Sector antenna	OFDM modulation
Large circuit scale (trade-off with performance)	Large antenna size	Hardware size? Power Consumption?
×	×	

Basic (parallel) type FFT circuit



Number of butterfly operations

FFT points N	radix - 2 r	radix - 2 number of operations m	radix -4 r	radix -4 number of operations m
8	3	12		
16	4	32	2	8
32	5	80		
64	6	192	3	48
128	7	448		
256	8	1024	4	256

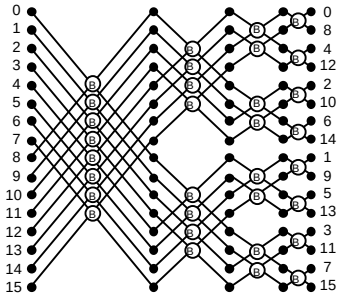
radix - 2

$m = \frac{N}{2}\log_2 N$

radix - 4

$m = \frac{N}{4}\log_4 N$

FFT circuit structure



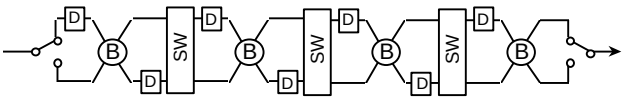
Basic (parallel) type FFT circuit

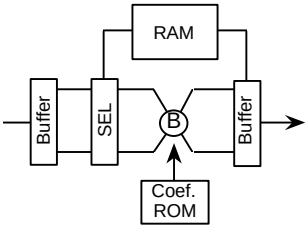
Hardware size

Loop type < Pipeline type < parallel type

Power Consumption

Loop type ? Pipeline type



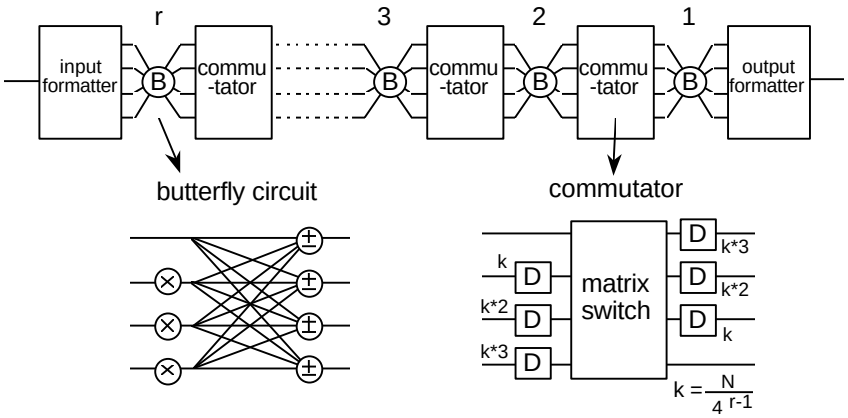


Loop type FFT circuit

Parameters

Data rate	25 Mbit/s
Modulation scheme	QPSK-OFDM
FFT point	16, 32, 64 assumed to be equal to OFDM sub carrier
Technology	0.7 µW/MHz/gate (0.35µm CMOS)

Pipelined FFT circuit (radix-4)



Hardware size and power consumption of pipelined FFT circuits

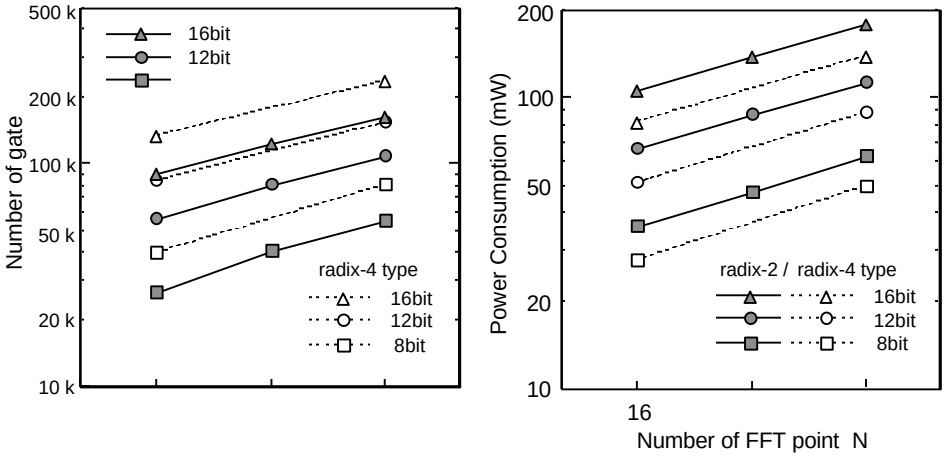
radix-4 type pipelined FFT circuits

3 quantization bits : 12 bit

circuit block		power consumption
3 butterfly circuit 1 butterfly circuit = Adder(108G)*30 + Multiplier(2250G)*12 = 30.2 kG	90.7 kG (58.6%)	55.5 mW (62.6%)
delay line (D)	26.2 kG (16.9%)	17.2 mW (19.4%)
coefficient ROM	3.5 kG (2.3%)	5.6 mW (6.3%)
matrix switch	1.8 kG (1.2%)	1.0 mW (1.1%)
bit arrangement	18 kG (11.6%)	
	(100%)	88.6 mW

Hardware size and power consumption of pipelined FFT circuits

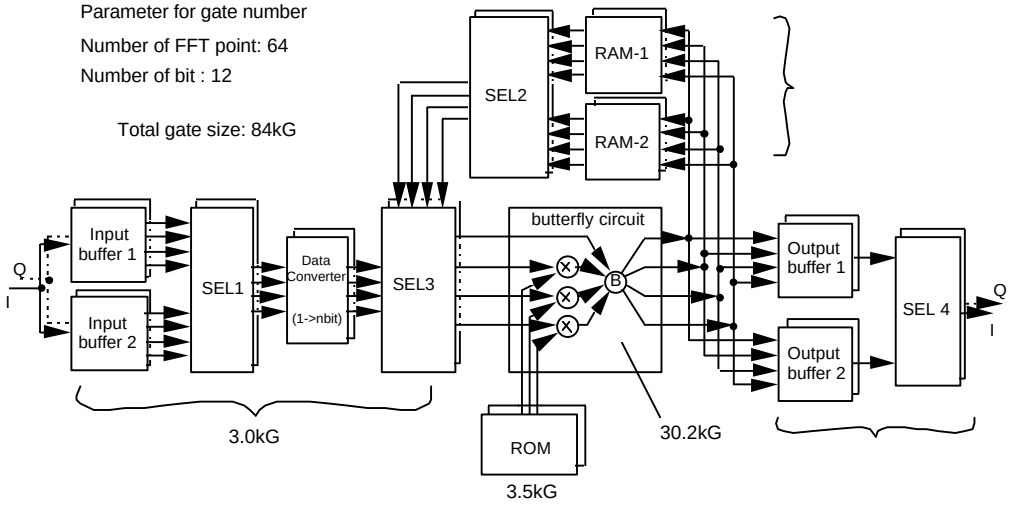
FFT clock frequency = 6.25 MHz (radix-2 type)



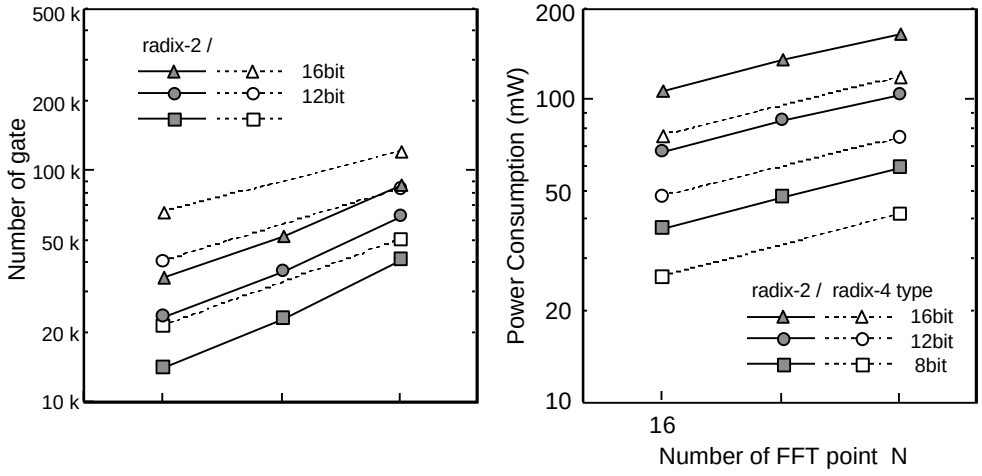
Loop type FFT circuit

Parameter for gate number
Number of FFT point: 64
Number of bit : 12

Total gate size: 84kG



Hardware size and power consumption of loop-type FFT circuits



Conclusion

e.g. 64 point FFT for 25Mbit/s QPSK-OFDM modulation
(radix-4 type, 12 bits operation)

Pipelined FFT circuits	155 kG	89 mW
Loop-type FFT circuits	84 kG	75 mW

Items to be considered

- Frequency error sensitivity (AFC)
- Clock recovery
- Preamble length
- Guard interval (multipath delay)