

# PAN Feasibility: The BodyLAN™ Experience

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INTERNETWORKING  
POWERED BY BBN

## Personal Area Networks

### *Driving requirements include:*

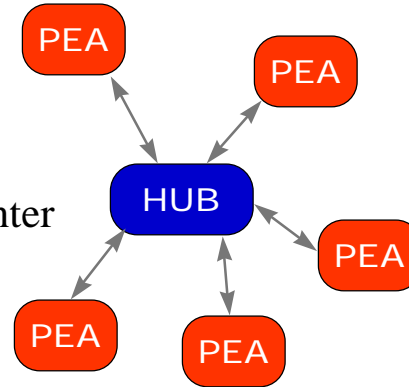
- Very low power consumption
- Very small devices (including peripherals, sensors, etc.)
- Easy integration into devices (minimal SW)
- Cross-network interference tolerance
- Very low cost

### *Simplifying characteristics include:*

- Data rate requirement is relatively low
- Range is short (2-10 meters)

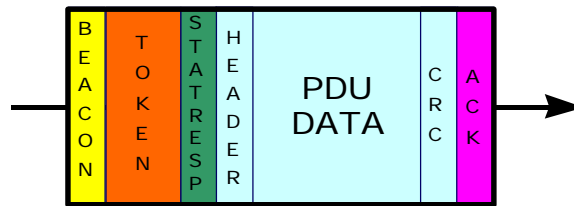
## BodyLAN Topology

- For simplicity, a STAR topology is employed.
- The *Hub* is at the center and runs the show.
- Around the edge are Personal Electronic Accessories (*PEAs*)



## Key Characteristics

- Simple TDMA structure:



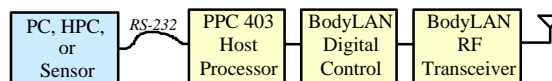
- Cross-network interference:
  - CDMA-like burst spacing using Optical Orthogonal Coding
  - Frequency agility

## Other Key Attributes

- PAN requirements demand only small networks; 7-bit MAC address is sufficient.
- Dynamic device attachment supported via a form of slotted Aloha layered on top of the TDMA structure.
- Ad Hoc networking easily supported: any device can function as a Hub.
- Prioritized bandwidth allocation is easily achieved via Hub token allocation mechanism. (*Partly demand-driven via Status Response messages from PEAs.*)
- Design readily enables single-chip Data-Link and MAC implementation.

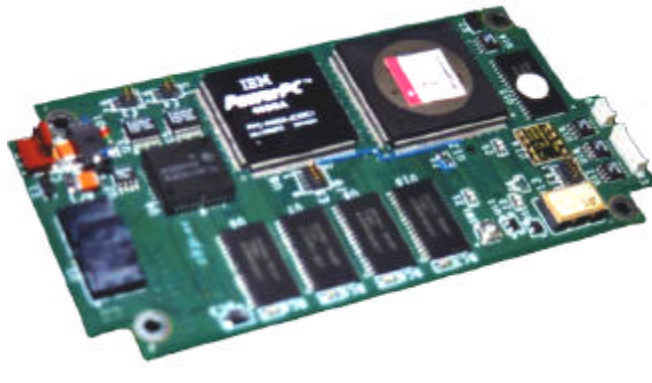
## Proof-of-Concept Demo

- Demonstrated with two real applications in early 1998.
- Basic structure:



- PowerPC (PPC) runs the device driver and protocol stack. (*PPC selected since needed to run Inertial Navigation code used by a demonstration sensor PEA.*)
- Digital board contains an Altera PLD with MAC layer implementation and debug logic.
- RF transceiver a small discrete implementation.

## Host Processor & Digital PLD



## Characteristics of POC Demo

- Fully operational, with good performance
- Dynamic attachment / detachment works
- Dynamic bandwidth allocation over TDMA structure
- 100mA with PowerPC @ 25MHz  
Transceiver draws 10mA when running (xmit/recv)  
PLD draws about 15mA (ASIC est. @ 500 $\mu$ A)  
*(lots of debug and test support, no board-level optimization)*
- Range adjusted to about 2m, have run up to about 5m

The End

Any Questions?