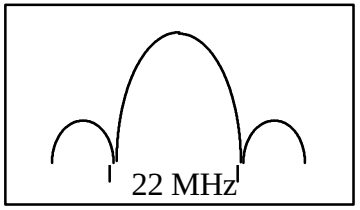
2.4 GHz QMBOK High Rate PHY

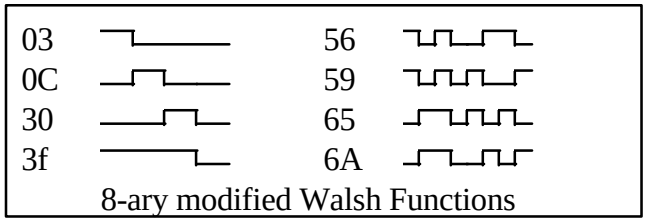
Harris Submissions for Comparison Matrix

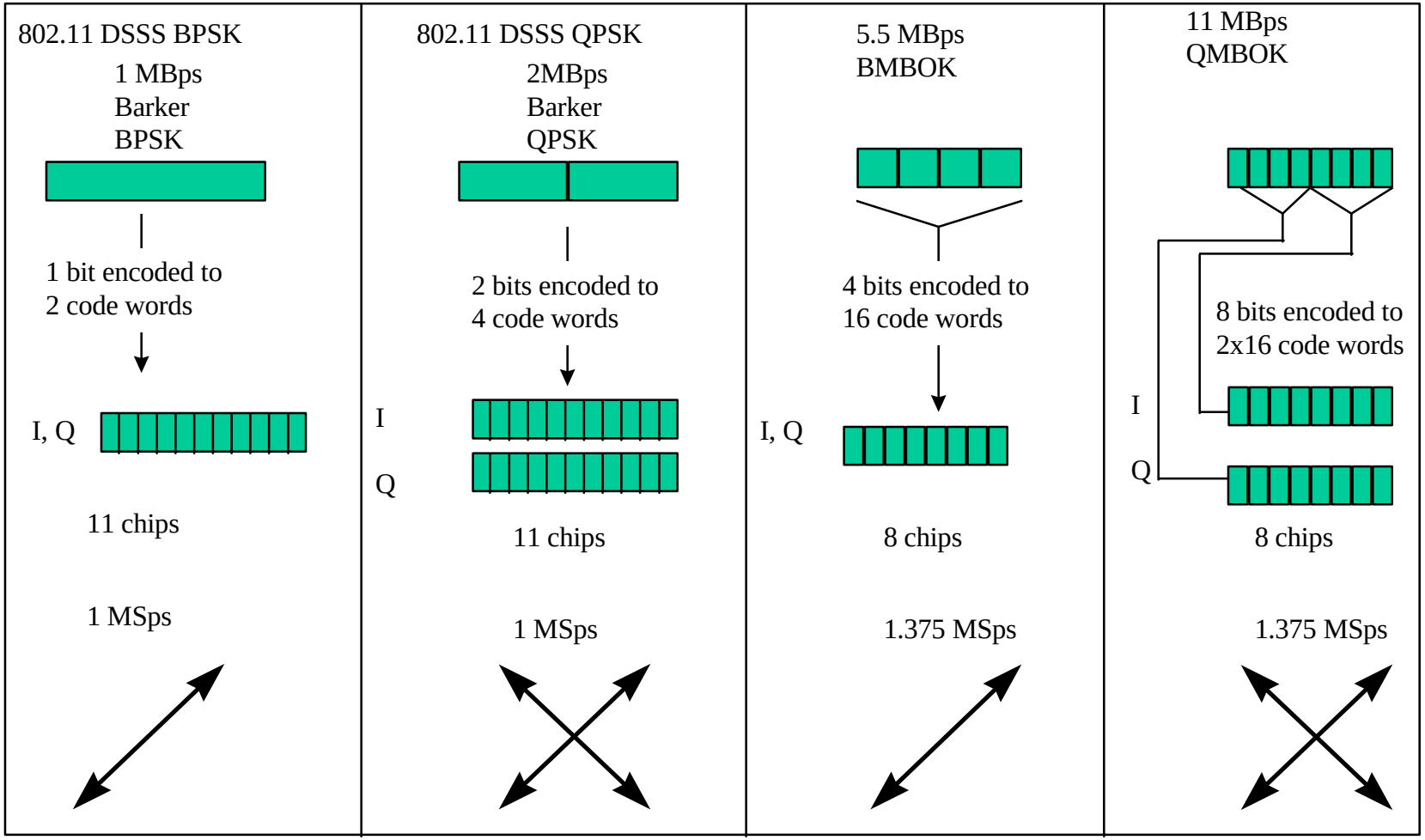
Suggested Technical Approach

- Utilize MOK/PSK modulation techniques to realize 4 to 8 bits/symbol
- Use existing preamble and header to insure interoperability.
- Increase symbol rate to 1.375 MSps (8 chip symbols) and hold existing spread rate
- Use existing 802.11 DS parts for the RF & IF circuits

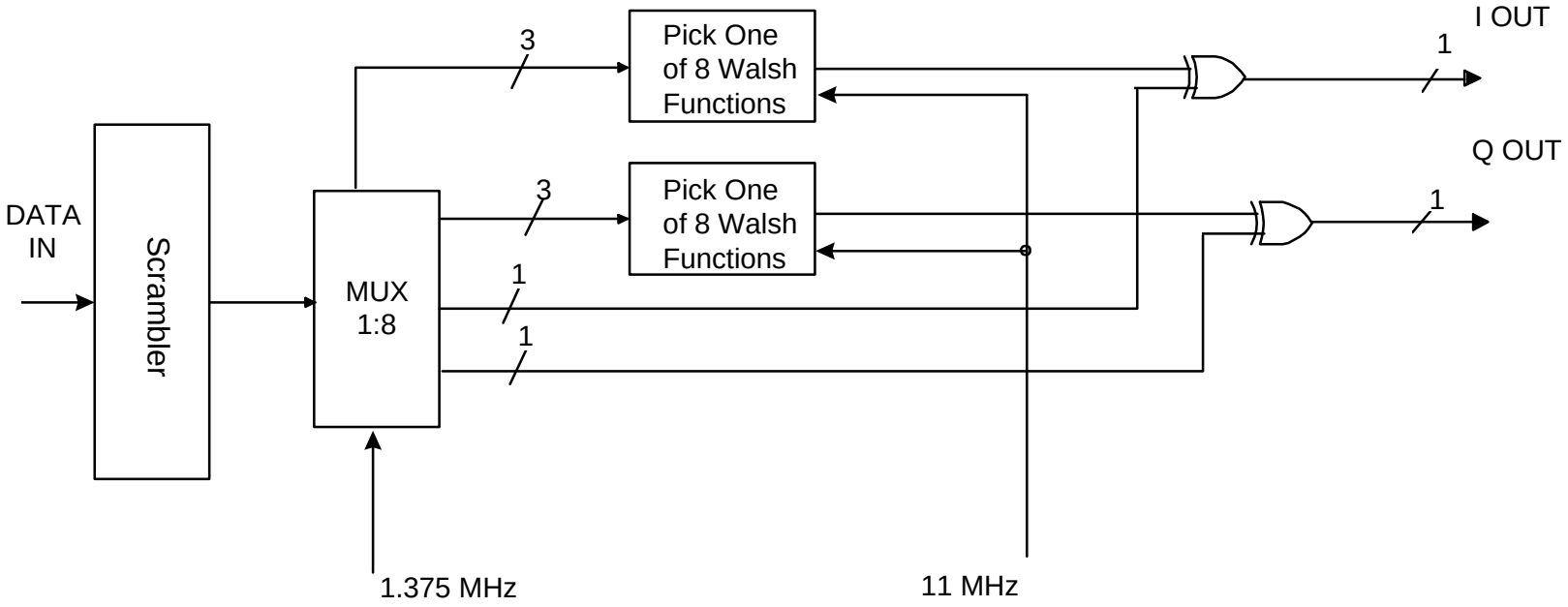
Modulation Technique and data rates







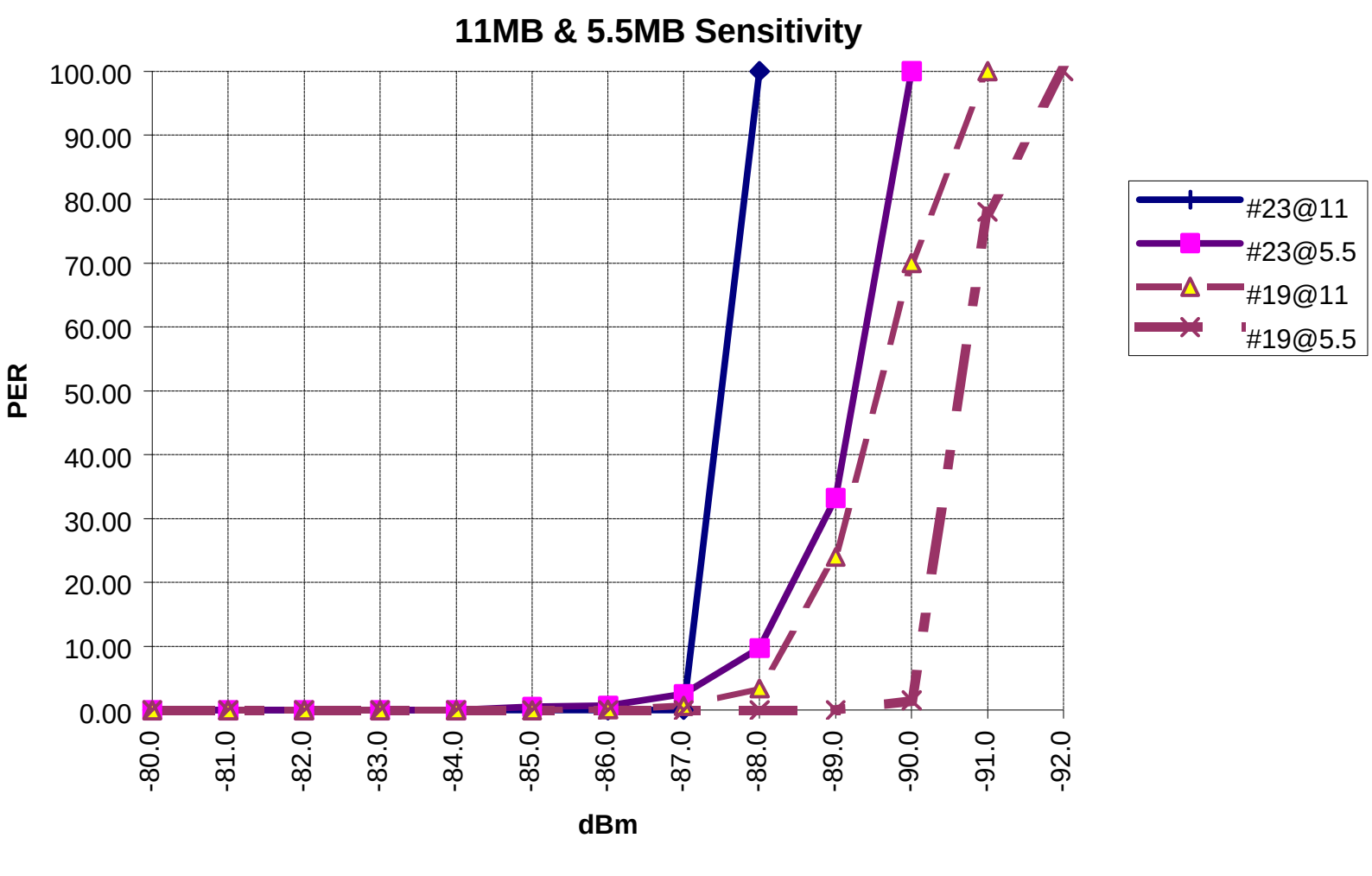
QMBOK Modulator Technique for 11 MBps



Data Rate = 8 bits/symbol * 1.375 MSps = 11 MBps

Receiver Sensitivity

Data from two different radio units at two data rates



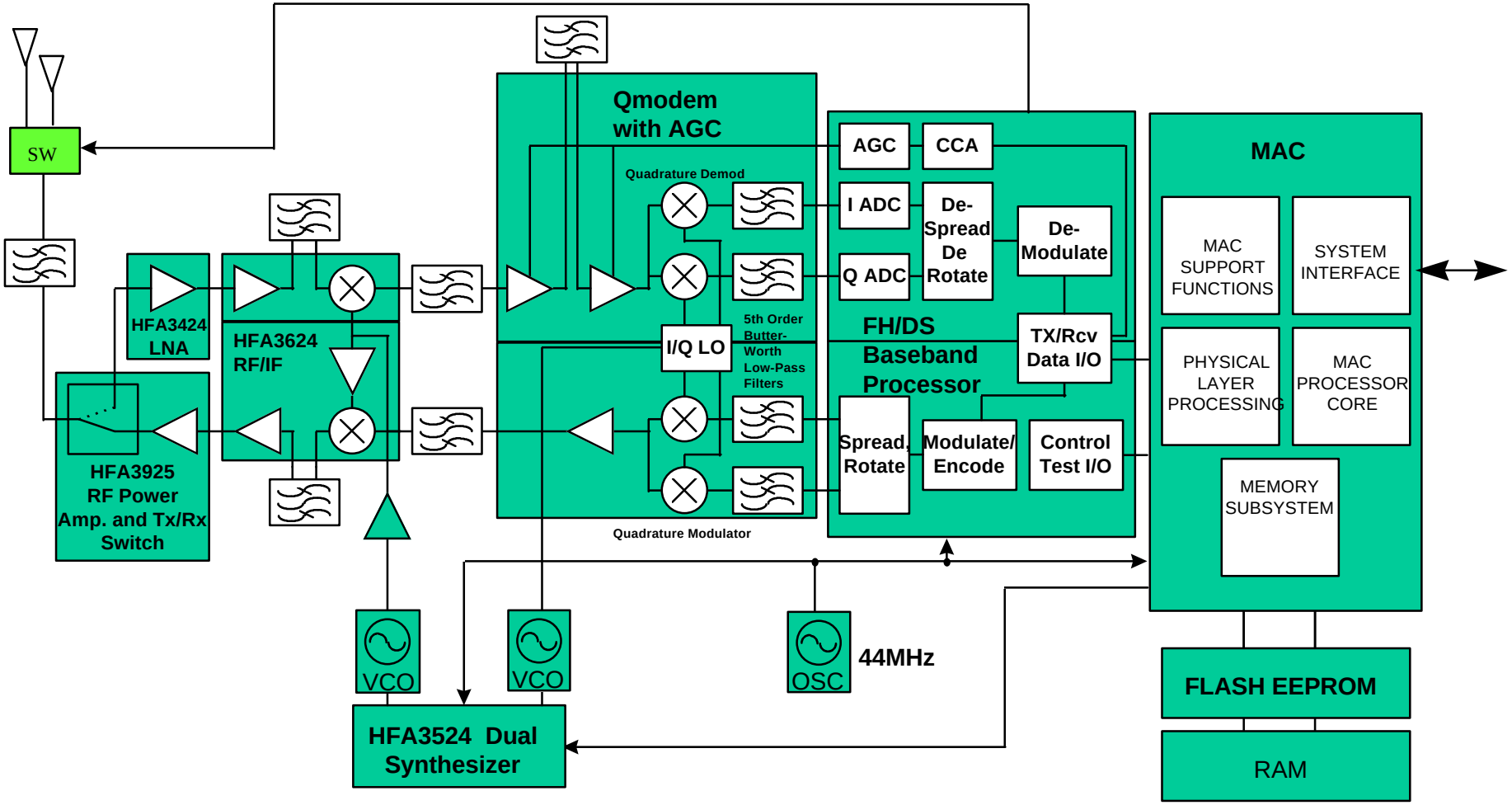
Reference Submissions

- 70254 IEEE 802.11 High data rate PHY extensions
- 70867 Suggested 802.11 High Rate PHY Technique
- 71447 Proposed 802.11 High Rate PHY Technique
- 80377 Multipath Issues & Architectures
- 80467B Harris 2.4 GHz short proposal
- 80477B Harris 2.4 GHz full Proposal
- 80557 Empirical Benchmarks
- 80567 Implementation for High Speed PHY
- 81157 Sliding DFE for Equalizing QMBOK
- 81167 Harris 2.4 GHz selection criterion
- 81347 Harris draft Text
- 81427 Harris IP Statement

RF/IF Complexity relative to current low rate PHY

- Basically uses same RF and IF as existing 802.11 DS PHY
- Equalized version replaces the IF limiter with AGC and has more A/D converter bits.
- A combined DS/FH mode uses non optimal wideband IF filters with some loss of FH performance in a crowded environment

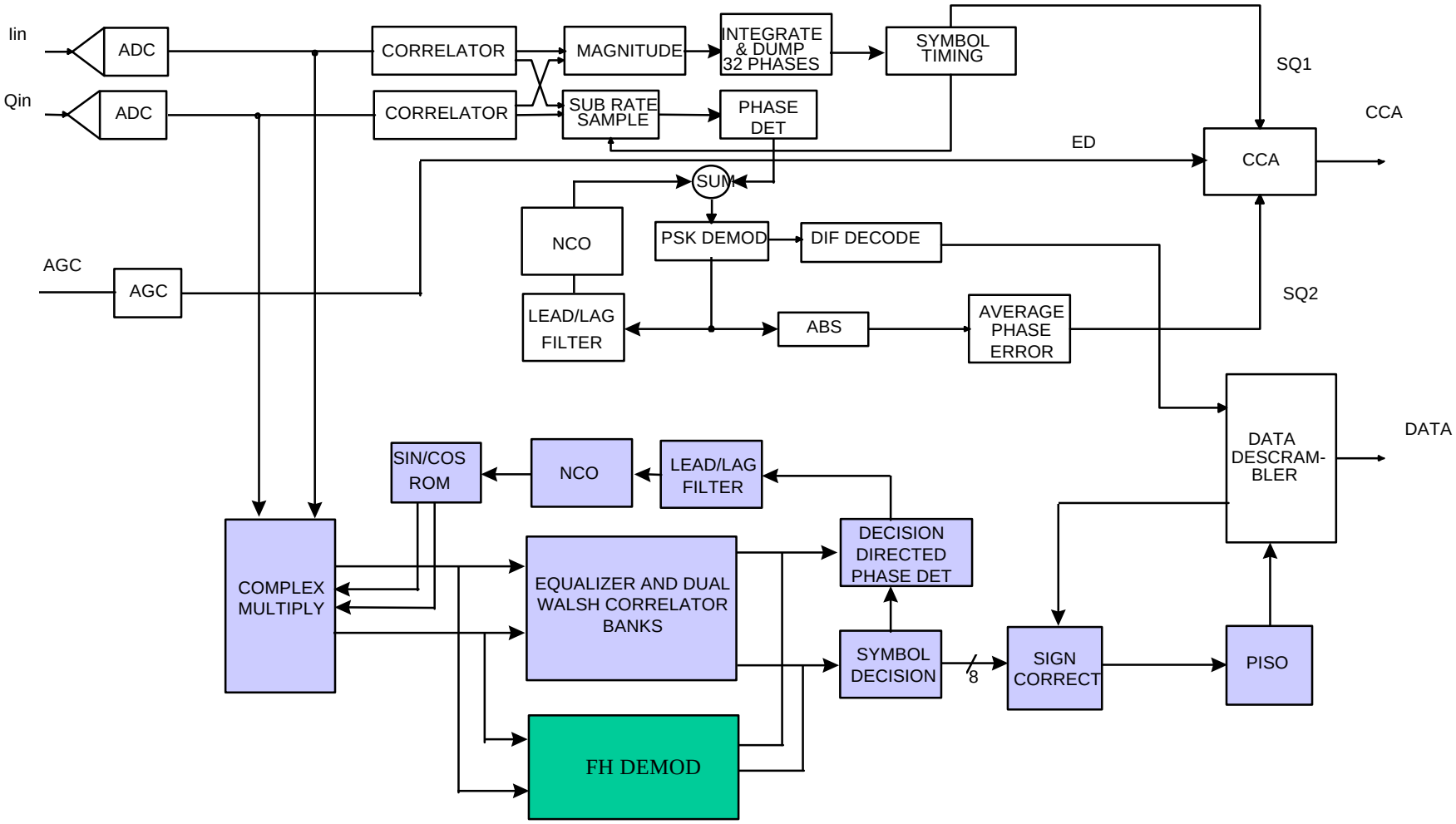
Receiver Structure Description



Baseband Processing Complexity relative to current low rate PHYs

- Addition of high rate without equalizer increases the DS only baseband processor complexity from 23K gates to 33 K gates
- Addition of equalizer to increase delay spread from 30 to 100 ns takes an additional 40 K gates
- The addition of FH interoperable mode has not been fully worked out yet

DEMODULATOR BLOCK DIAGRAM

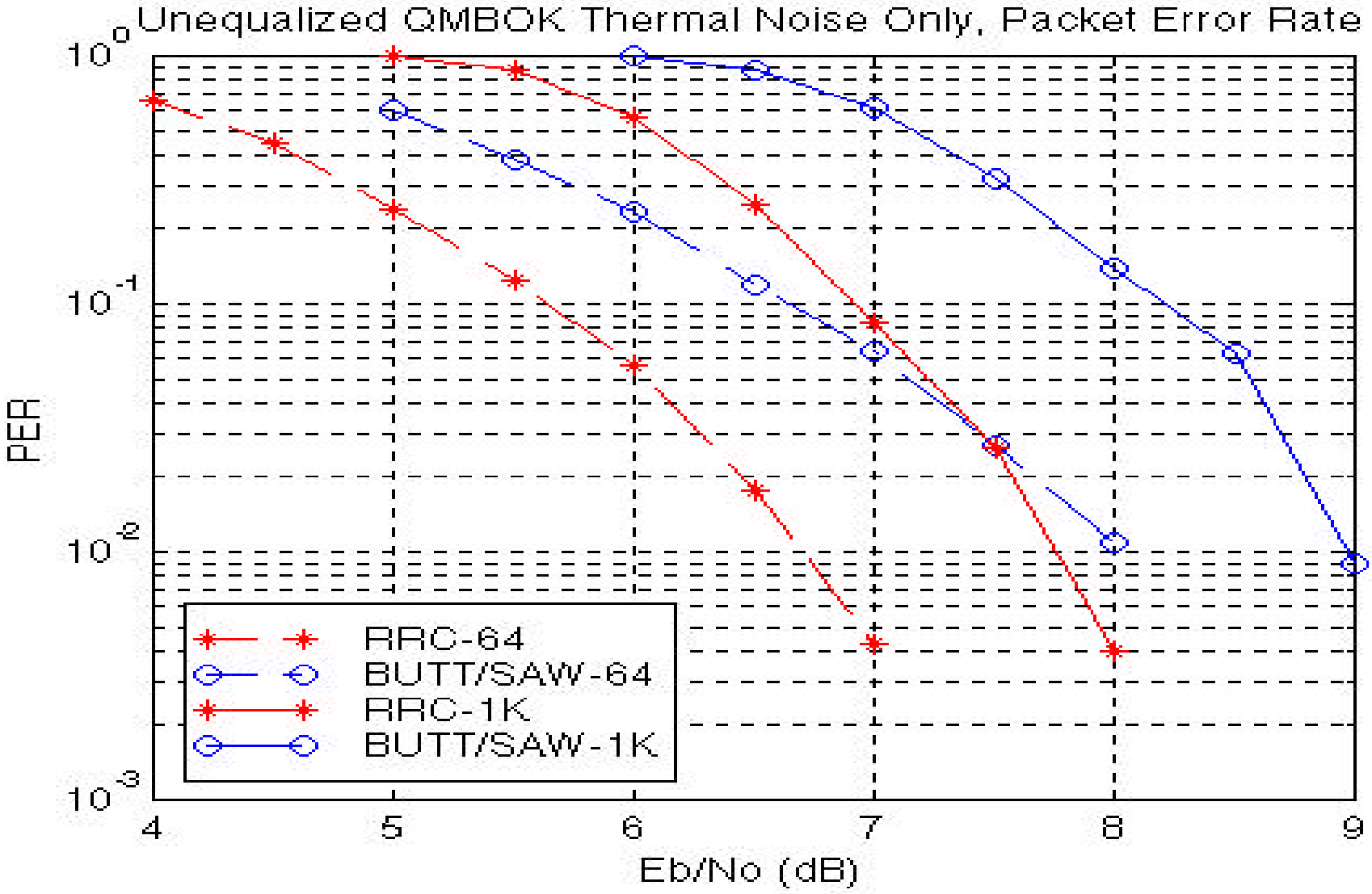


SHADED BLOCK ARE THE ADDITIONS TO DS FOR FH AND HIGH RATES

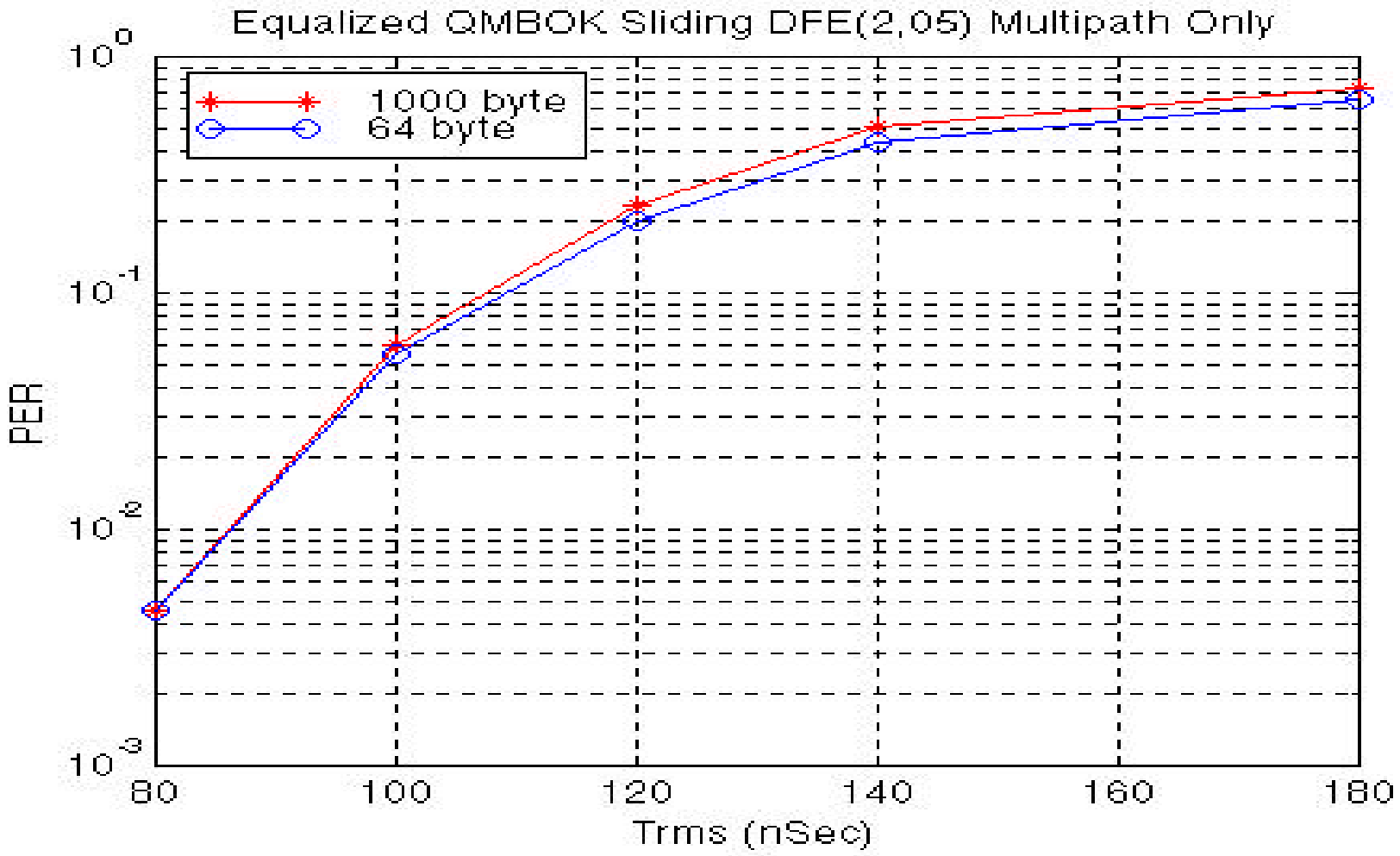
Antenna Diversity and performance impact

- Antenna diversity can improve the performance of the link more simply than an equalizer but not as much
- The performance impact has shown an improvement of a factor of 2 to 4 in PER in field testing
- The negative impact is to require additional length in the preamble (already covered by the 802.11 preamble)

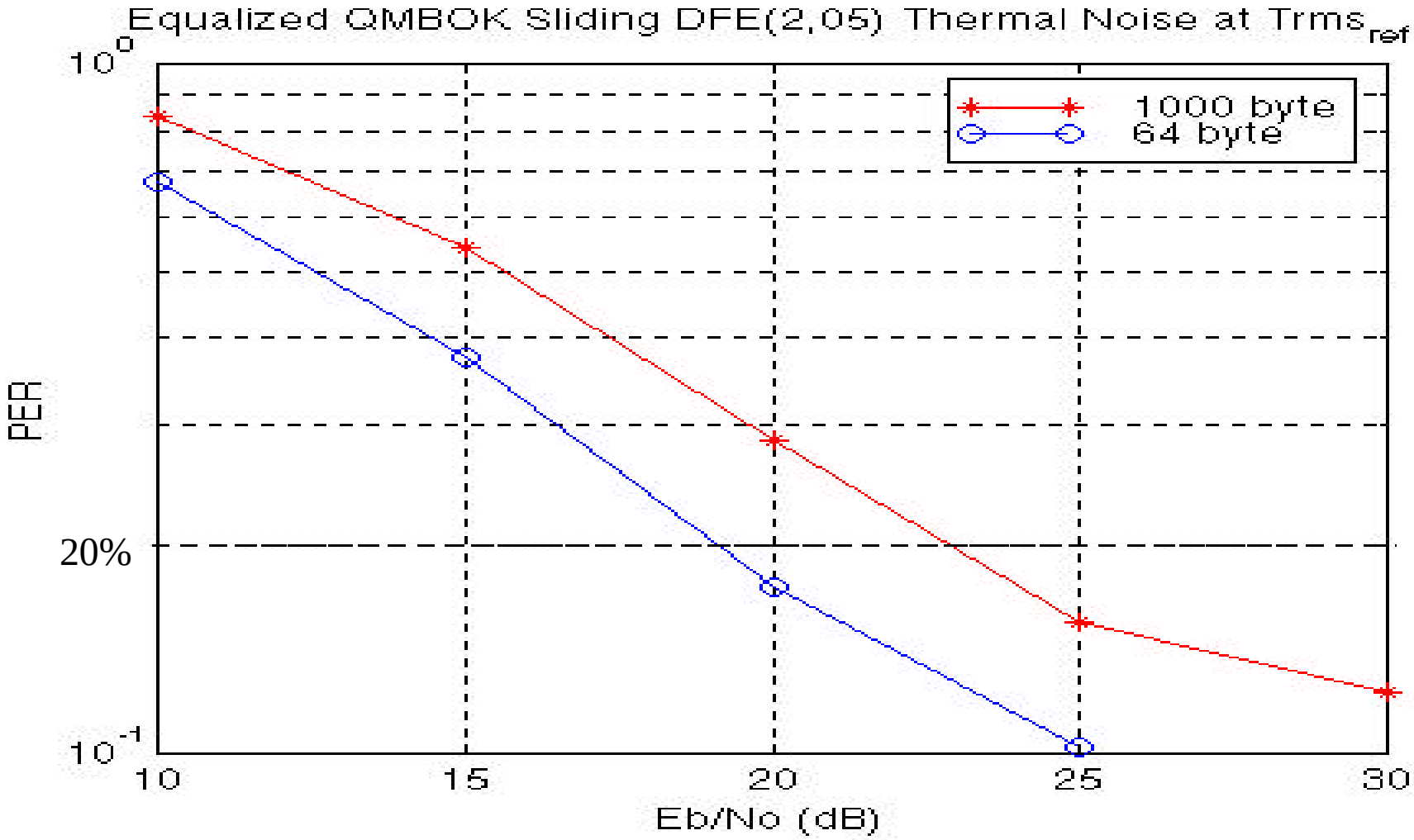
Graph of PER Vs. Thermal Noise (no Multipath).



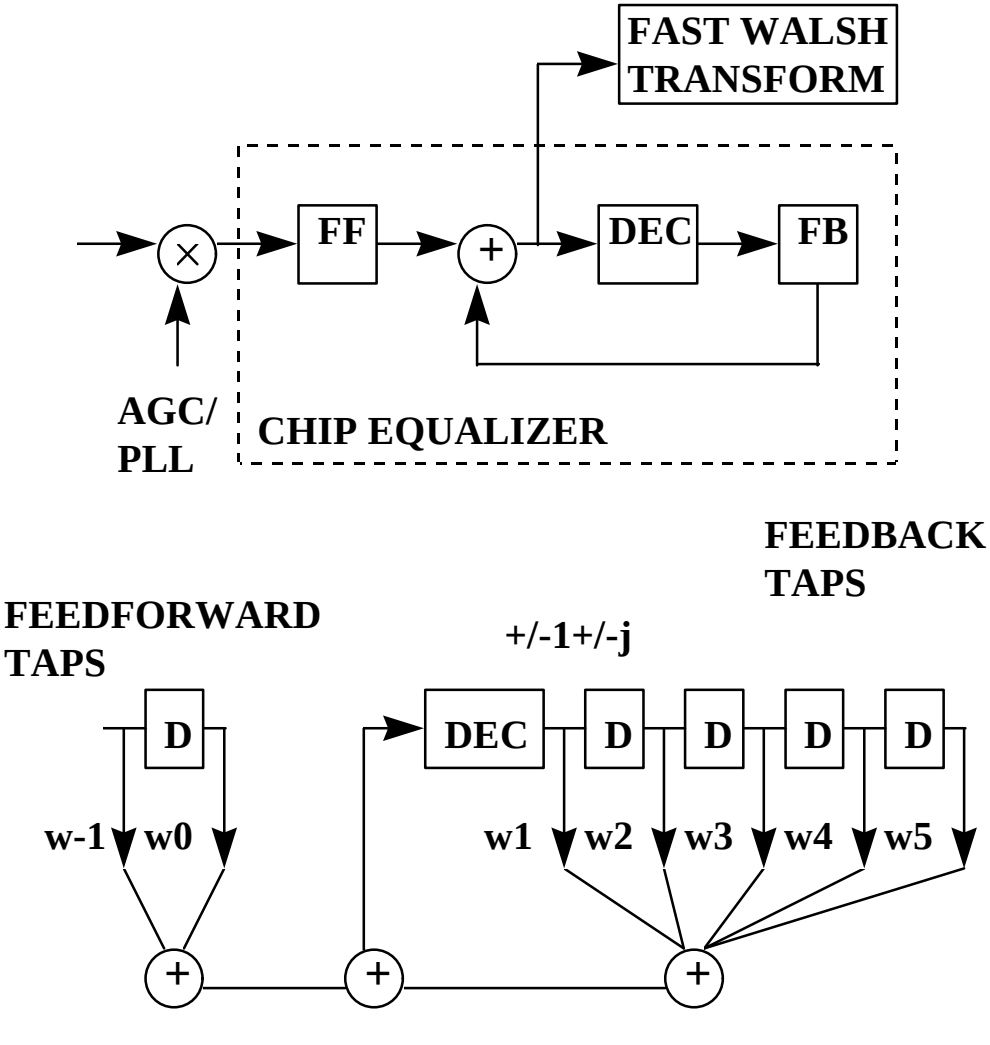
PER Vs. Multipath Only (No Noise).



PER Vs. Thermal Noise with Multipath at 10% PER. Eb/No at 20% PER for 64 and 1000 byte packets.

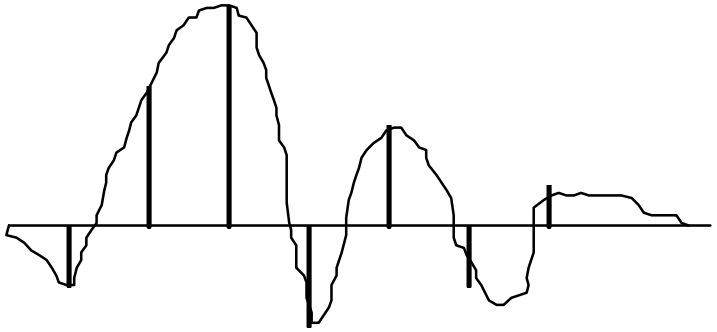


DECISION FEEDBACK EQUALIZER



FEEDFORWARD WEIGHT CALCULATION

CHANNEL IMPULSE RESPONSE



2 FF MATRIX EQUATION

$$\begin{bmatrix} h0 & h-1 \\ h1 & h0 \end{bmatrix} \begin{bmatrix} w-1 \\ w0 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

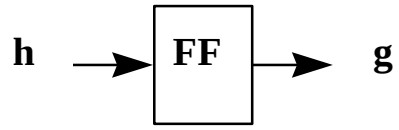
SOLUTION

$$\begin{bmatrix} w-1 \\ w0 \end{bmatrix} = \begin{bmatrix} -h-1 \\ h0 \end{bmatrix}$$

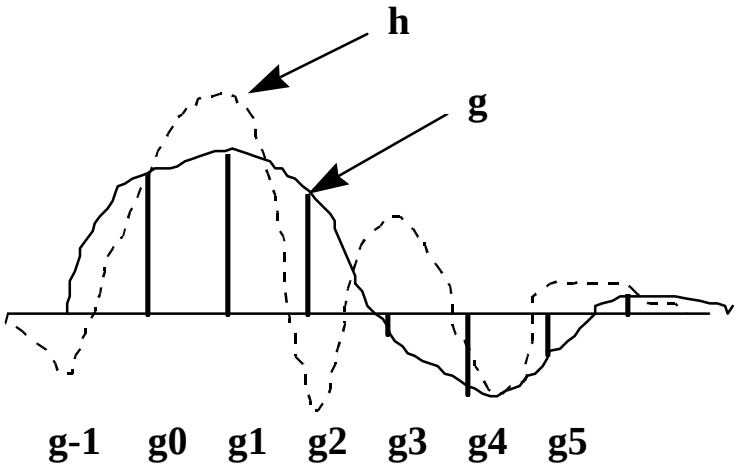
FEEDBACK WEIGHT CALCULATION

CHANNEL IMPULSE RESPONSE

FEEDBACK IMPULSE RESPONSE

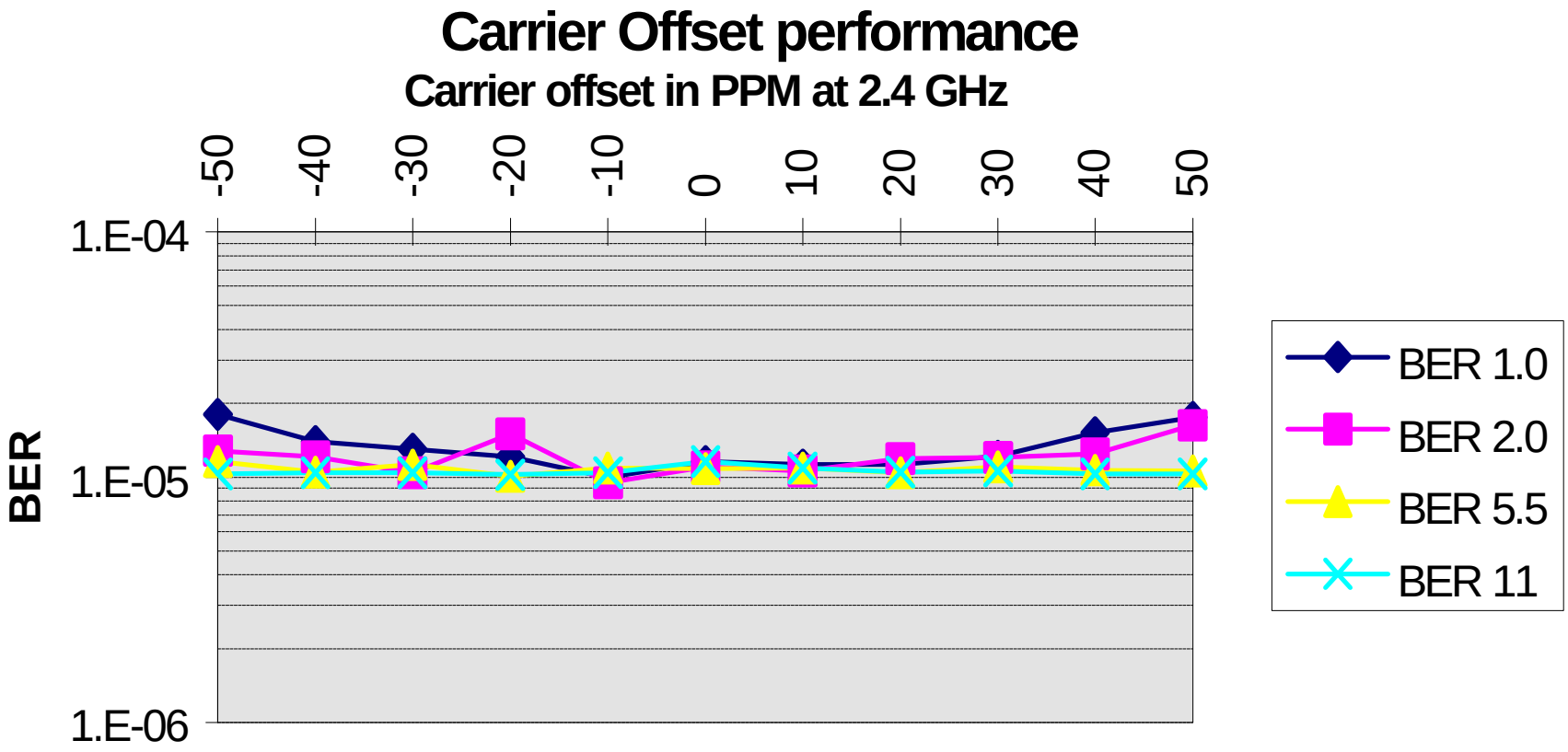


CONVOLVE



$$\begin{bmatrix} w1 \\ w2 \\ w3 \\ w4 \\ w5 \end{bmatrix} = \begin{bmatrix} g1 \\ g2 \\ g3 \\ g4 \\ g5 \end{bmatrix}$$

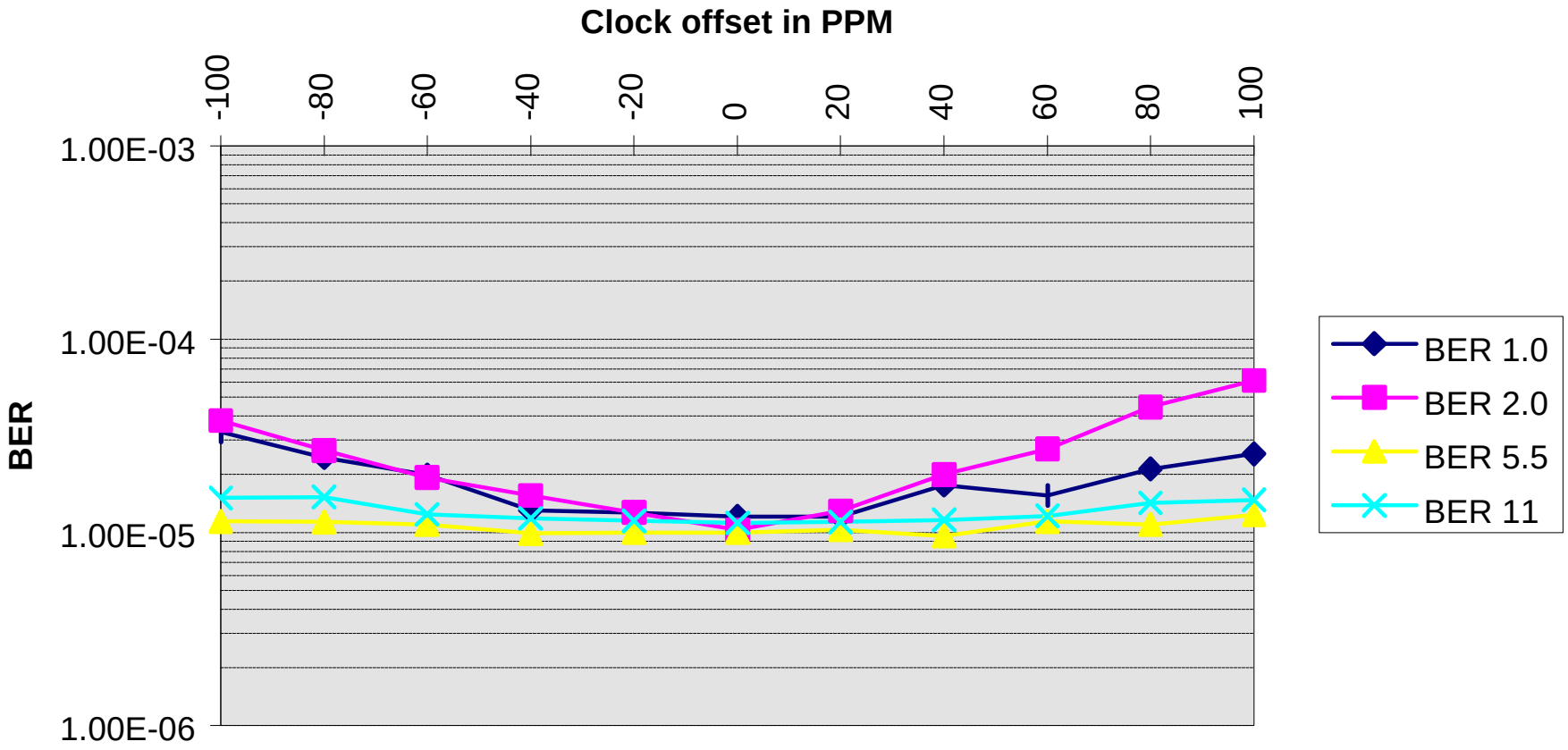
BER versus Carrier Offset Performance of HFA 3860



Required Data Clock Frequency Accuracy

- The new high rate PHY requires the same clock frequency accuracy as the existing low rate PHY or $\pm$ 25 PPM.
- The limitation is that the maximum data clock offset should drift no more than 1/8 th of a chip in 128 us.

BER versus Clock Offset Performance of HFA 3860



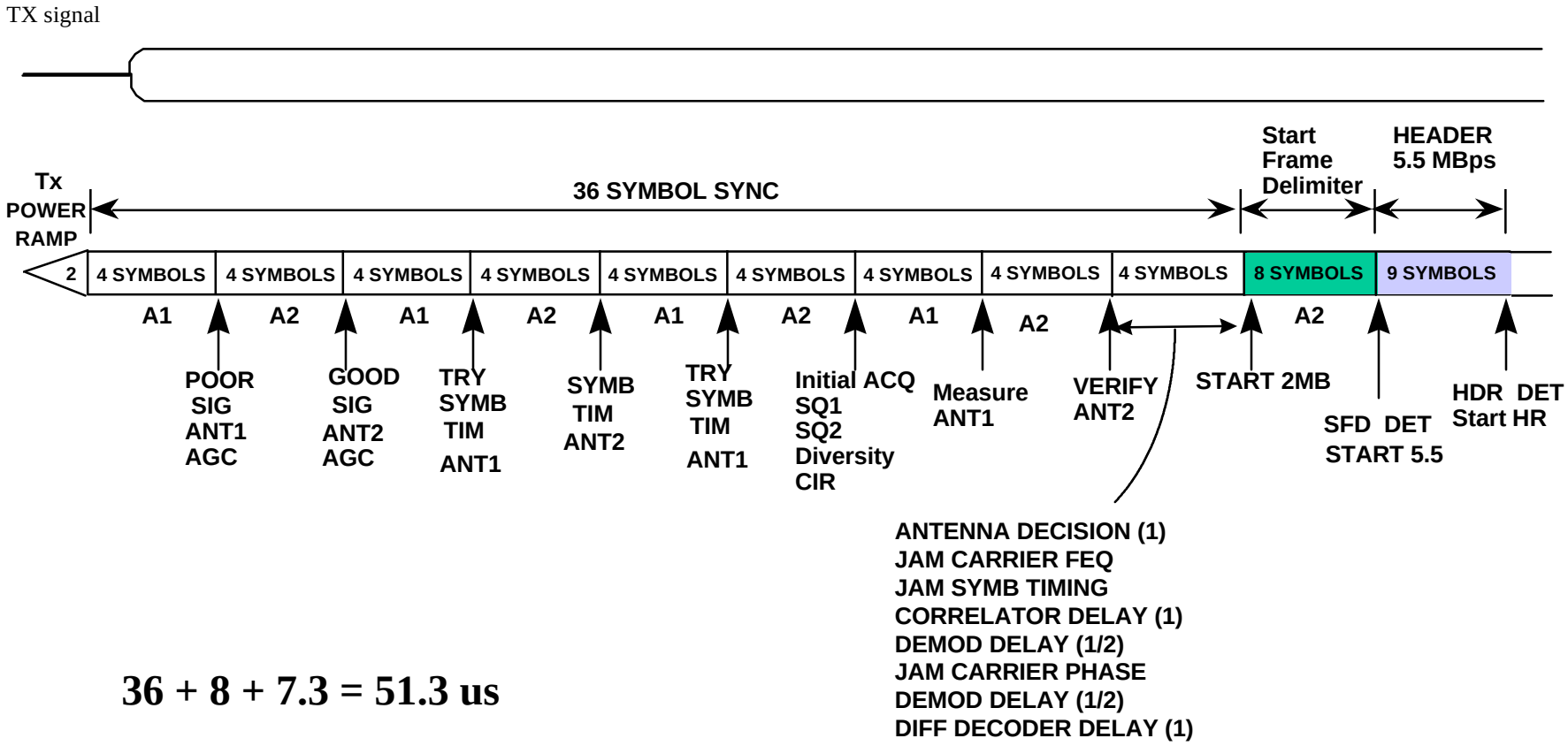
Preamble Length

- Our DS interoperable approach is to include the standard DS or FH 802.11 preamble and header which includes ample time to do diversity and equalization.
- For the cases where interoperability is not an issue, a short (52 us), high rate header is used.
- For FH interoperability, a standard FH preamble and header is followed by the short high rate header.

Short Acquisition

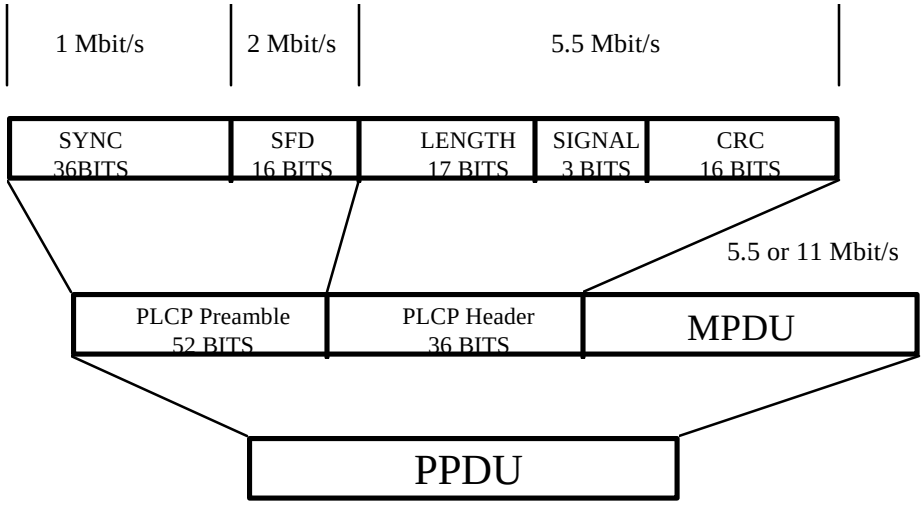
- The preamble and header of the high rate waveforms will be received at a higher signal strength than the case with 1 and 2 Mbit/s, so the acquisition can be quicker. Starting point is 5.5 Mbit/s.
- 13.6 dB Es/N0 in sync detection allows Pd = .999 and Pfa = 10e-7 detection on 4 symbols. Use three for phase roll detection for frequency acquisition.
- 1 symbol is abused for switching and AGC settling
- Use synchronous (FH) scrambler to avoid seeding time.
- Send SFD @ 2 MBps to reduce duration by half
- Send header @ 5.5 MBps and use 1 bit rate field to indicate high or low rate. Switch to 11MBps after header
- Use length field expressed in 0.5 us increments (17 bits).

DUAL ANTENNA ACQUISITION TIMELINE



36 + 8 + 7.3 = 51.3 us

HR preamble and header



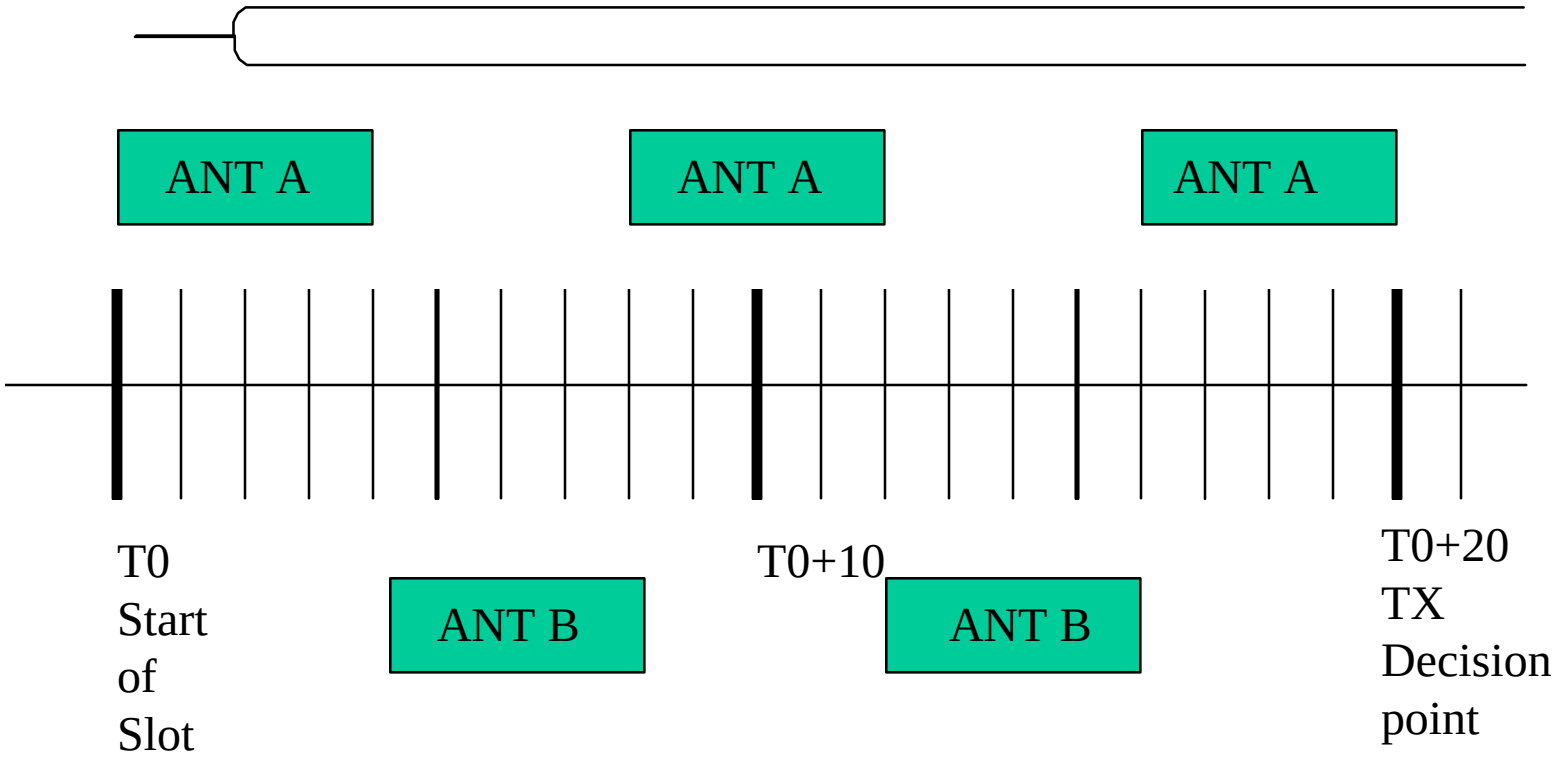
total overhead = 51.3 us

Slot Times

- We propose no change in the DS PHY slot time of 20 us or FH slot time of 50 us.
- For the short header, we have allowed 4 microsecond antenna dwells which divide evenly into the 20 us slot times.
- This allows ample time to detect the signal on both antennas for CCA purposes.

Slot timing and CCA with 4 us dwells

Transmission can start up to 5 us late



CCA mechanism and Co-Channel signal detection time

- We measure the correlated signal energy in the preamble antenna dwells beginning when the receiver is enabled and compare that to a threshold
- FH detection is done on clock energy in similar dwells.

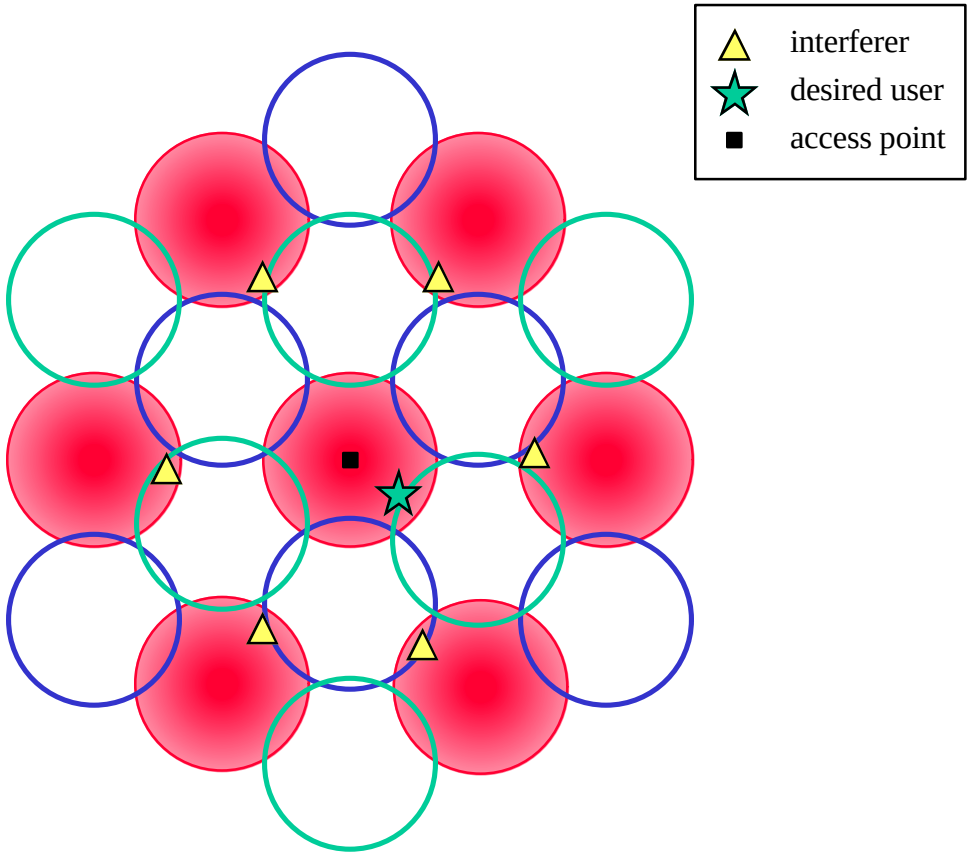
RX/TX turn around time and SIFS

- The transmitter has a 1.3 us processing delay from bits in to bits out the antenna
- The receiver has 3.3 us processing delay from bits in the antenna to bits out
- The RX/TX turn around time is less than 2 us exclusive of the above delays.
- We propose to use the existing 10 us DS SIFS or 28 us FH SIFS.

HR Channelization Scheme

- We propose the existing DS channelization scheme.
- Three non overlapping channels spaced either 25 or 30 MHz in the band
- A choice of 5 MHz channel centers with 11 channels in the ISM band for the US and 13 in Europe.

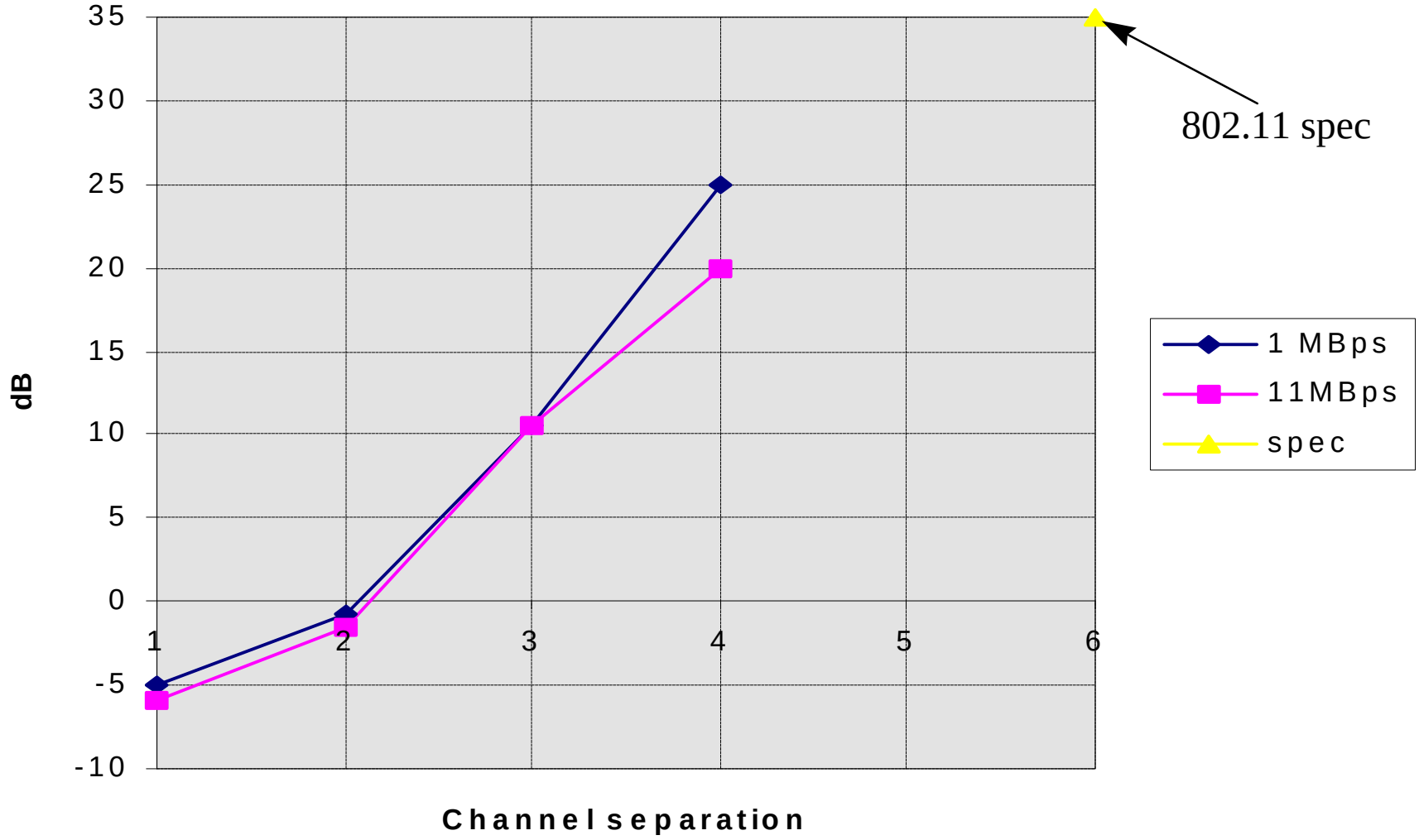
Cell Planning With 3 Frequencies



6 far interferers

Adjacent Channel Interference Rejection

- Only 8 dB more RX filter skirt rejection is needed to achieve the same ACI rejection as the existing low rate DS PHY
- The increase is due to the higher required SNR in the spread bandwidth.


Adjacent Channel Interference Rejection
35
30
25
20
15
10
5
0
-5
-10
dB
1
2
3
4
5
6
Channel separation
802.11 spec
1 MBps
11MBps
spec

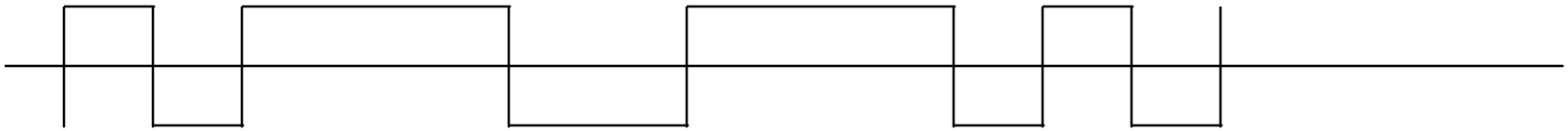
MKK Requirements

- The processing gain requirement for Japan is that the ratio of the 95% power bandwidth to the symbol rate be greater than 10:1
- For rates over 8 MBps, this requires that the 95 % bandwidth be greater than that of the 1 and 2 MBps modes
  - For example, the Harris approach at 11 MBps requires 13.75 MHz
- Proper shaping of the baseband pulse shape can expand the power bandwidth sufficiently
- See paper 98/203 for more details

Bandwidth expansion by pulse shaping

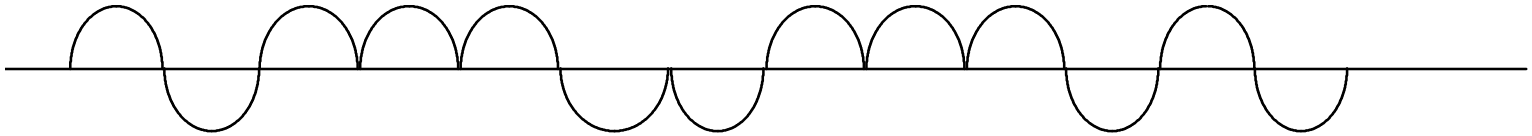
Normal NRZ shaping

95% Spread Factor = 9.3



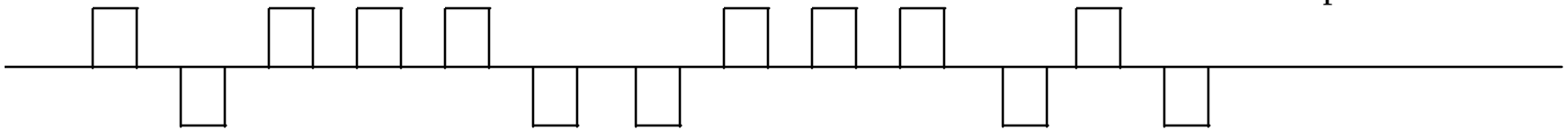
Root Raised Cosine shaping

95% Spread Factor = 10.6



50 % RZ shaping

95% Spread Factor = 10.5



Spectrum Effects

- The narrower pulse shape enhances the high frequency content of the waveform
- The spread factor needs to be > 10.0 in order to meet the MKK requirements
- The spread factor with Tc/2 pulse shape is 10.6 which is overkill, but proves the point.
- To be investigated: 0.75Tc pulse shape, where width is adjusted to just pass the requirement, while being easy to implement.
- This mode can be added to the basic waveform without changing its interoperability over the air
- The Pulse shaping does add amplitude modulation, which is undesirable, but unavoidable.

Co Channel Interference Rejection, DS

- The ability of the modulation to tolerate other networks in the area was tested. The results are S/J in dB that causes 5% PER

Signal → / Jammer ↓	1	2	5.5	11
1	6.2	7.6	6.9	8.7
2	4.2	6.5	4.0	6.7
5.5	0.9	4.9	3.0	7.9
11	0.9	3.1	1.9	6.8

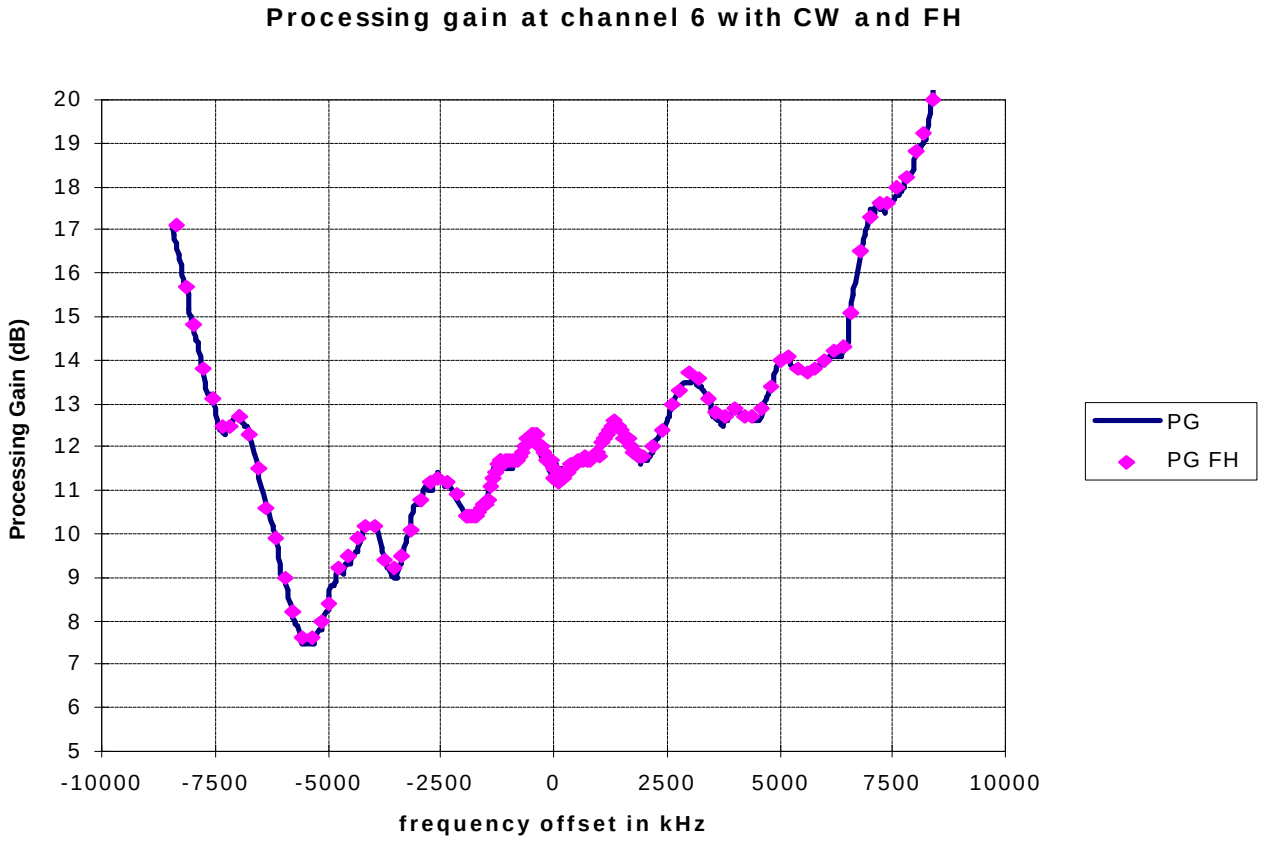
This indicates that the worst case Jammer for 11 MBps is the 1 MBps waveform that spoofs the preamble.

S/J where CW jammer gives 10% PER

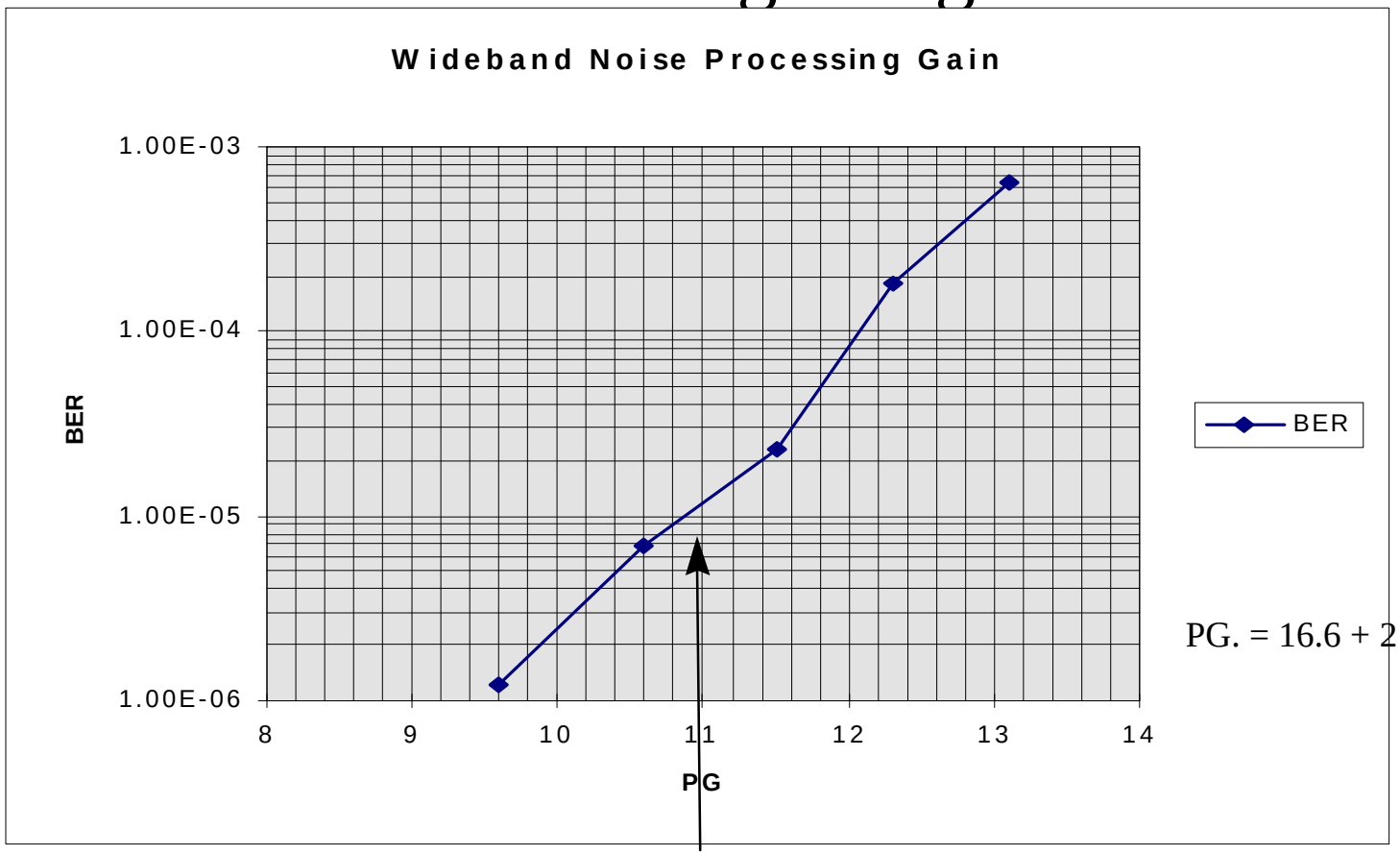
Data shows that the performance is virtually identical with FSK and CW Jamming

Note: channel 1 data is better

The 20% discard point is 10.3 dB



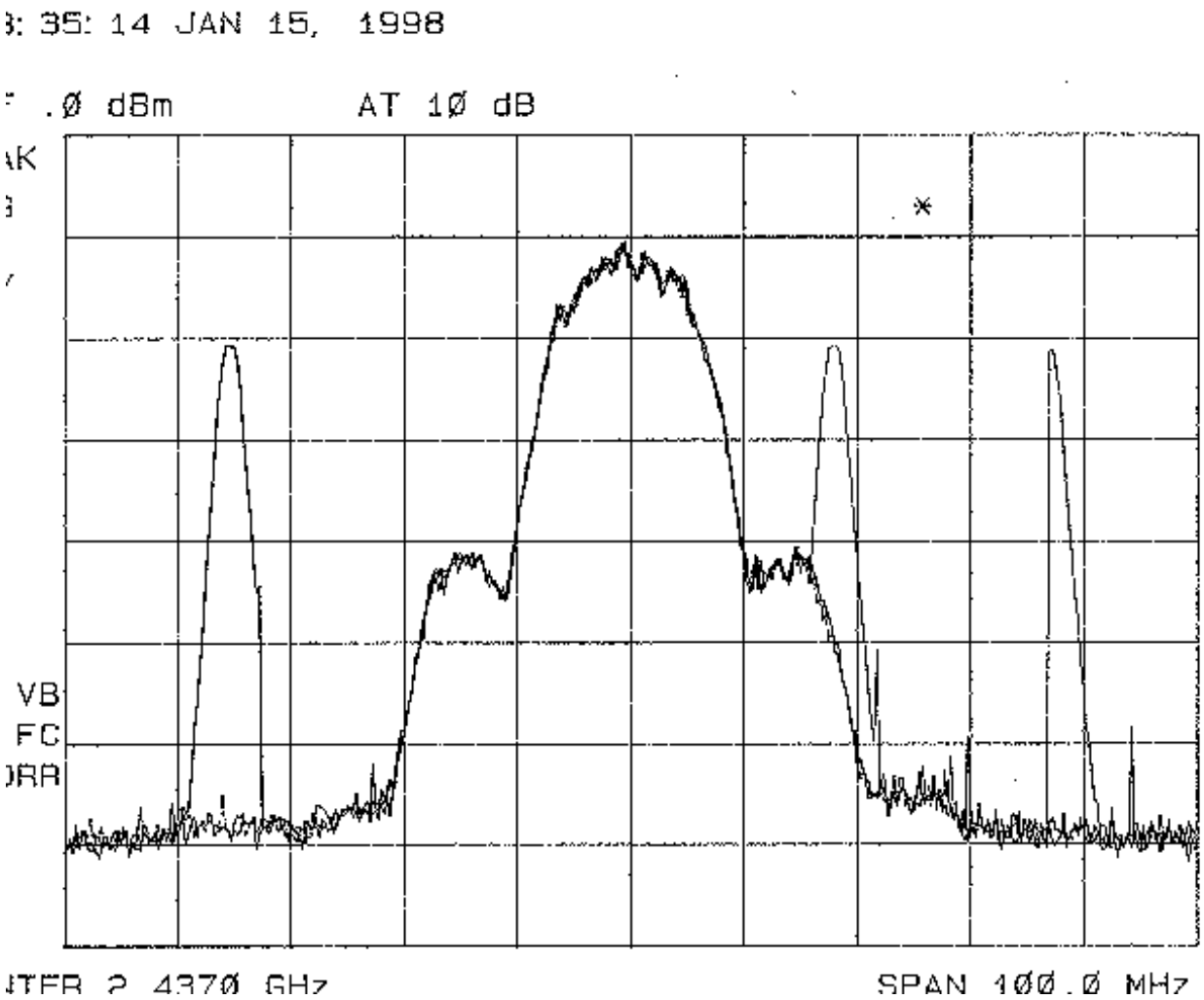
Other Interference Immunity tests, WB Noise Jamming Margin



PG. = 16.6 + 2 - S/J = 10.9dB

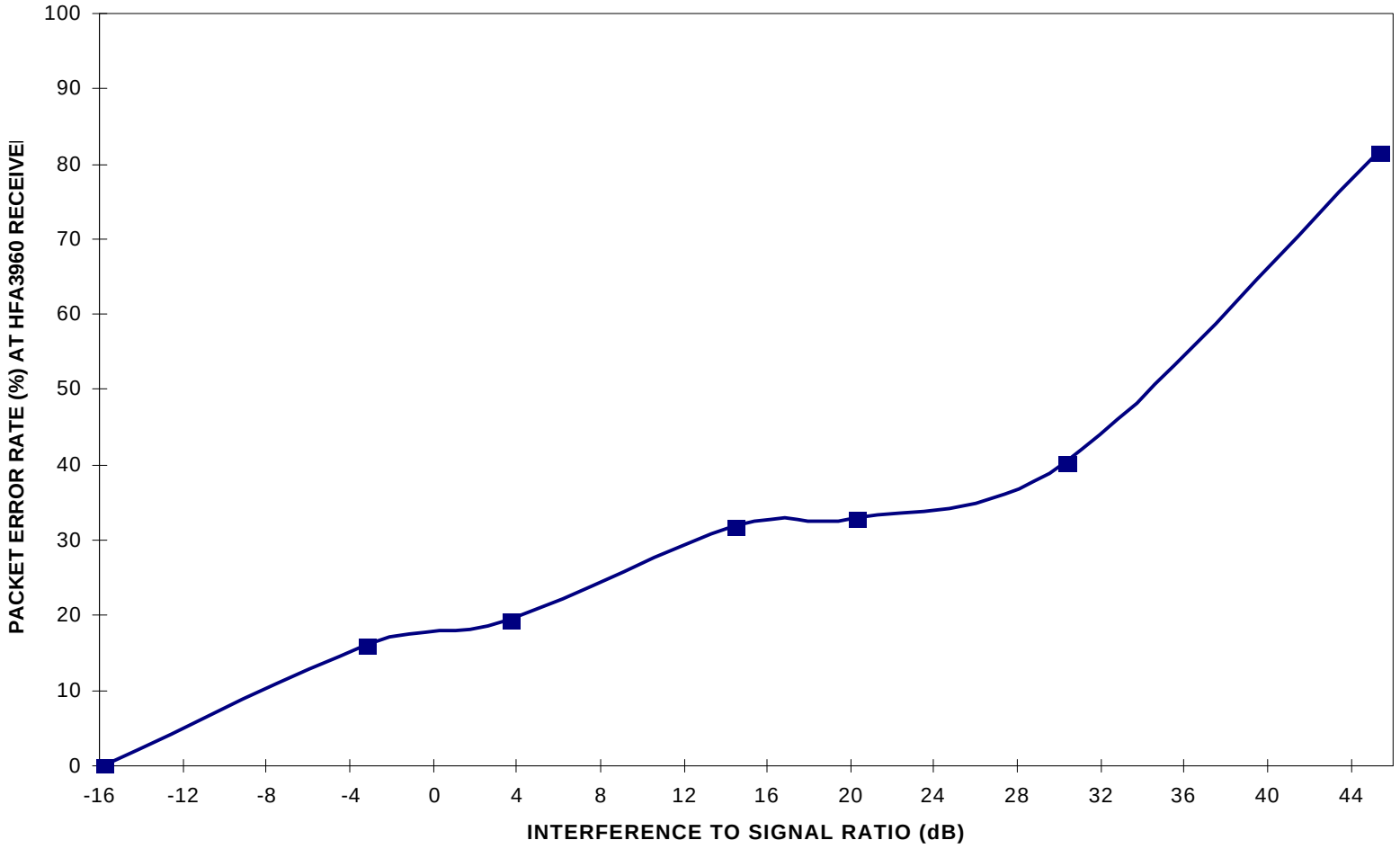
Note: Processing Gain is measured at the 1.0e-5 BER point
S/J is measured in spread rate bandwidth

Other Interference Immunity tests, FH



Other Interference Immunity tests, FH

Figure 6.4.1-2 PER VERSUS FREQUENCY HOPPING INTERFERENCE
Breeze Net FH Transmitter at 3 Mbps Interfering HFA3860 11-Mbps Link on Channel 6



Total Number of Channels in the ISM band

- We propose the existing DS channelization scheme.
- Three non overlapping channels spaced 25 or 30 MHz in the band
- A choice of 5 MHz channel centers with 13 channels available. The highest two are not currently used by the existing standard in the US.

Aggregate Throughput

- The 3 non overlapping channels at 11 Mbps will allow 33 MHz total maximum achievable throughput in the ISM band.
- Link probability tempers this…….

Phase Noise Sensitivity

- There is no particular phase noise sensitivity with the proposed waveform. It performs as well in phase noise as any QPSK scheme.
- The measured phase noise of our receiver's LO which performs well is 2 degrees RMS

RF PA Backoff

- The QMBOK waveform needs about 5 dB of PA backoff to insure low regrowth of spectral sidebands.
- This is the same as the DS BPSK preamble requires.

DC power consumption

- The current, non equalized HFA 3860 QMBOK chip draws 30 mA at 3 VDC.
- This represents about 12% of the radio receive power.
- The equalizer will probably draw more than this.

Power Consumption

- Suggestions have been made to use more a constant amplitude modulation to save TX power
- Some constant amplitude modulations make the equalizer more complex
- If lower backoff in the PA saves 95 mA but costs 5 mA in the receiver the net savings is nil with a 5% TX duty cycle

Patent Submissions

- The Harris position is that we will only patent techniques having to do with our implementation.
- Anything likely to be embodied in the standard will be free of license from Harris.
- The QMBOK waveform is public domain.
- Having a patent does not protect you from other patents which may cover the same or similar techniques.

Interoperability / Co-existence strategy with current low rate PHYs

- Interoperable via use of existing low rate preamble and header, either DS or FH
  - In the case of the FH PHY, the low rate preamble and header must be followed by a short high rate header to re-establish antenna diversity and to train the equalizer
- Will defer or cause deferral via 802.11 mechanisms currently in place.

Is the proposal Interoperable at the data and antenna levels?

- Yes to both, the use of the existing preamble and header insures interoperability and the data format is not changed.

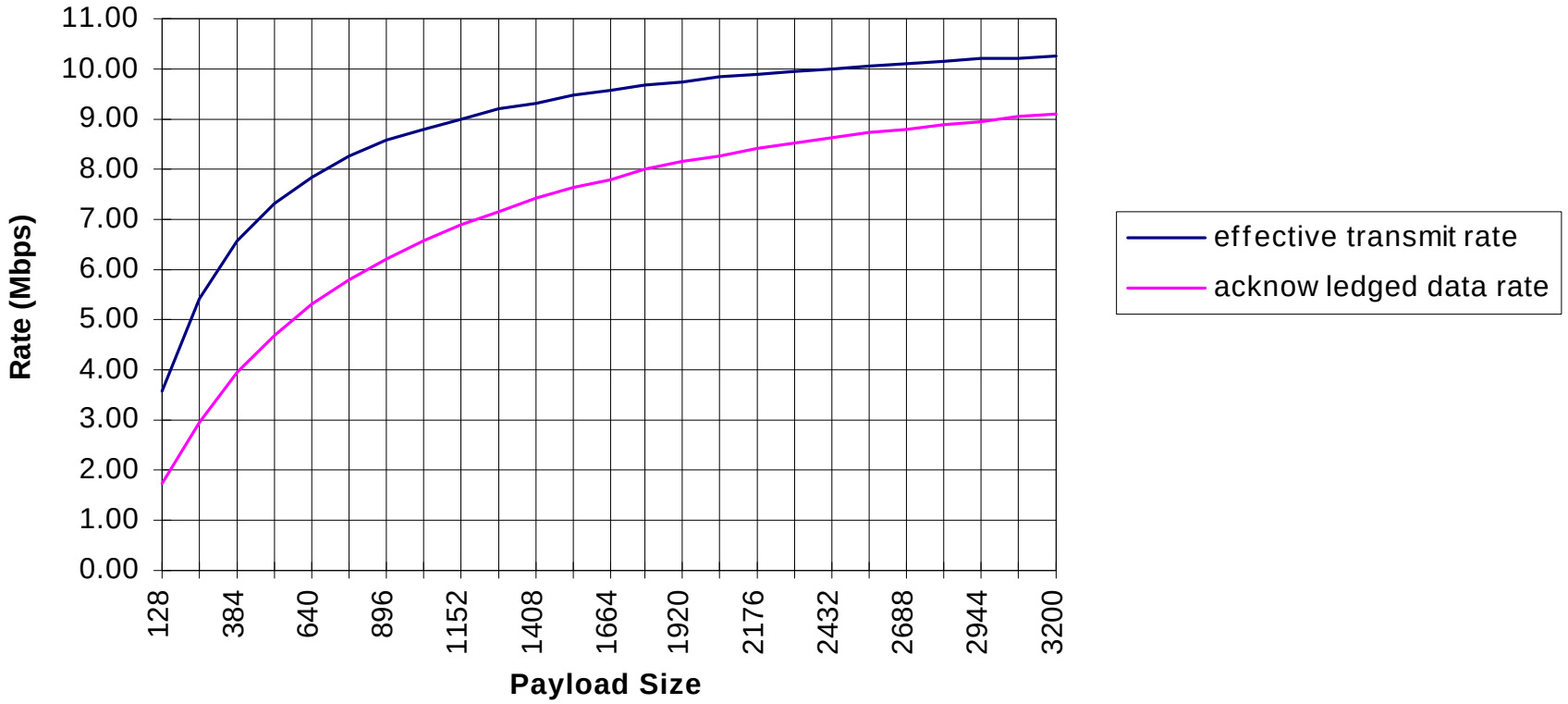
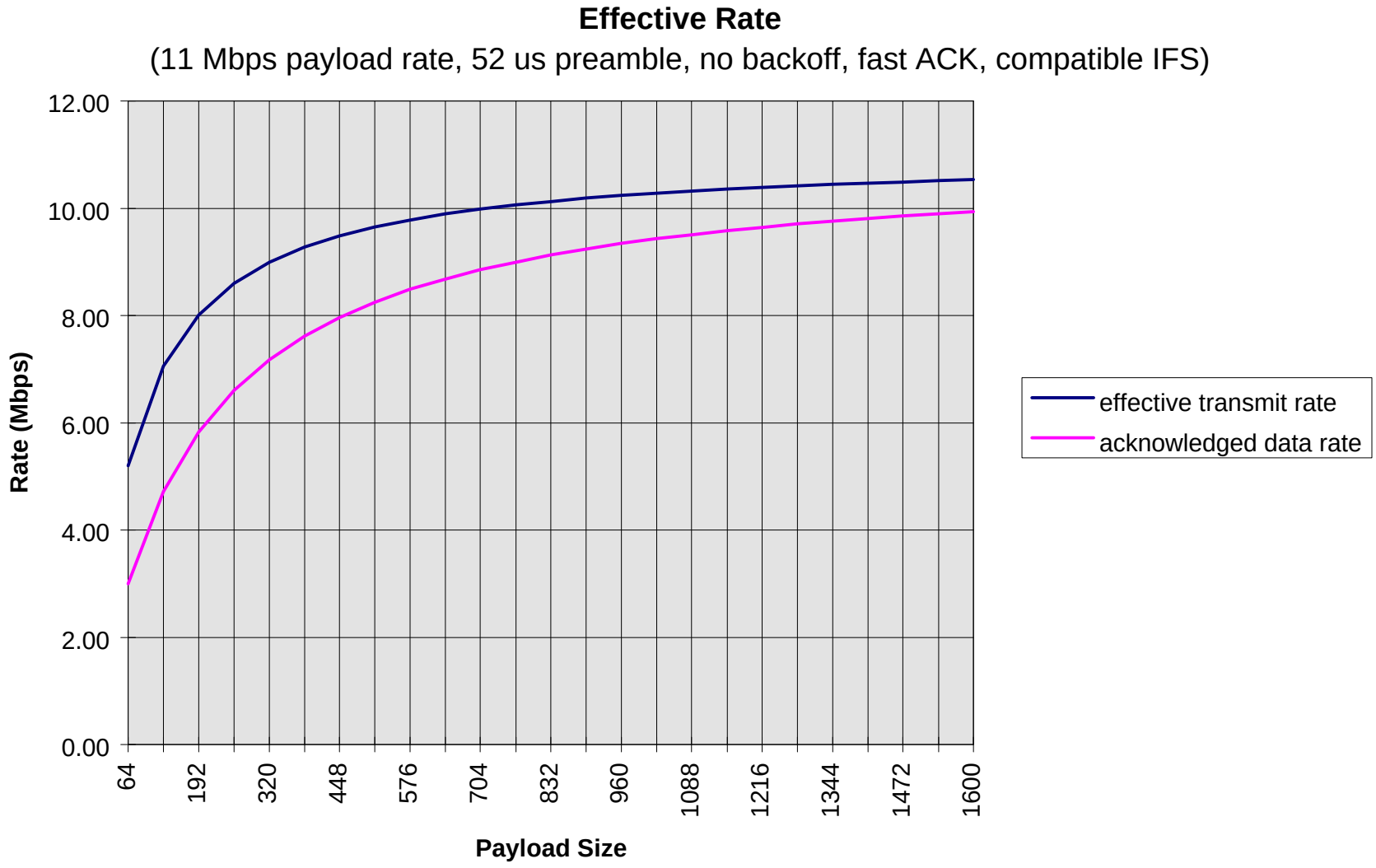
Performance penalty due to Interoperability / Coexistence.

- The DS overhead is 192 us Vs about 50 us without interoperability
- The FH overhead is 128 + 10 + 50 us or about the same
- This amounts to ~20 % on 1K byte packet
- with short preamble it is 5%

Performance penalty due to Interoperability / Coexistence.

Effective Rate

(11 Mbps payload rate, no backoff, ACK at 1 Mbps, compatibility header and IFS)



with 52 us preamble