IEEE P802.11
Wireless LANs

Some Technical details on BreezeCom+NEC proposal

Date: May 1998

Author: Naftali Chayat
BreezeCom
Atidim Tech. Park, Bldg. 1, Tel Aviv 61131, Israel
Phone: +972-3-6456262
Fax: +972-3-6456290
e-Mail: naftalic@breezecom.co.il

Abstract

The BreezeCom+NEC proposal is based on a single-carrier approach. The modulation type is an Offset Quadrature Modulation, meaning that quadrature components are staggered in time with respect to each other. This document illustrates some technical details on the implementation of the proposal. In particular, we shall discuss:

- Reference implementation of a transmitter
- Detection of the header, based on properties of complementary sequences
- Equalizer structure
- Channel estimation and equalizer initialization
- Carrier tracking loop structure
- Timing tracking considerations
- Should the equalizer be adaptive?

Finally, a short comparison with OFDM is conducted.

Transmitter Chain

The transmitter starts with digital generation of waveforms for the I and Q channels. This process starts with symbol generation (12.5 Msymbol/s per quadrature channel), and is followed by digital filter which increases the sampling rate to 25 Msamples/s with the 1 sample stagger between the I and Q channel. After Digital-toAnalog conversion of I and Q channels, antialiasing LPF follows. The two baseband signals are upconverted by a quadrature modulator and followed by a SAW filter. The IF signal is further upconverted to the 5 GHz band, where if undergoes amplification to the final power level.

Figure 1: Typical coherent transmitter block diagram

The digital filter, the antialiasing LPF (low pass filter) and the SAW (Surface Acoustic Wave) bandpass filter all participate in the shaping of the transmitted signal. The accuracy or complexity requirements of one part can be traded for that of the other. The length of the digital filter depends on the implementation accuracy, however it can be rather short (e.g. 4-6 taps) given that the waveshaping process is complemented by an appropriately designed SAW filter which creates a sharp rolloff and supresses the out-of-band components. The D/A accuracy requirements of about 8 bits suffices, though this can be significantly reduced (say, to 4-6 bits) by an appropriate SAW filter design. On the contrary, SAW filter may be avoided if sharper antialiasing filters and more accurate D/A converters are used.

The power amplifier should incorporate means for backoff control. This may be accomplished by a detector for power monitoring and means for gain adjustment, either at the final transmit frequency or at IF. Same variable gain element used for gain adjustment may be used for transmit power control.

Receiver Chain

The receiver starts with LNA and downconverter to an IF frequency, at which the desired signal is separated from the adjacent channels by an appropriate SAW filter. The variable gain amplifier (VGA) scales the signal to a level appropriate for A/D sampling. The variable gain receives control from power detector which may reside in the digital part of the modem.

Figure 2: Typical coherent receiver RF block diagram

A/D considerations

The A/D sampling rate is 25 Msamples/s. The resolution of the A/D takes into account both the quantization noise contribution and the headroom for signal peaks (especially in presense of multipath) and for accuracy of gain control. Accuracy of 6-7 bits is required for the binary mode, and 7-8 bits for the quaternary mode.

Phase noise considerations

The synthesizer resolution of 5 MHz is required at 5 GHz, with 200 MHz coverage. We assume that typical implementation will involve a synthesizer at 2.5 GHz with 2.5 MHz step size and 100 MHz coverage, followed by a doubler. The integrated phase noise requirements of –14 dBc and –20 dBc (for the binary and quaternary modes) should be increased by about 10 dB in order to bring them from 10% PER to small degradation, i.e. to –24 and –30 dBc, respectively. Assuming the f^{-2} phase noise model for the VCO and 50 KHz bandwidth assumption, this translates to

-24 dBc -3 dB –47 dB (50 KHz) = -74 dBc/Hz @ 50 KHz offset or –80 dBc/Hz @ 100 KHz offset,

i.e. –80 or –86 dBc/Hz for the binary or quaternary modes, respectively. Recall now that this phase noise budget is distributed between the transmit and receive side, and also between the IF oscillator and the RF oscillator, which calls for an improvement of 4-5 dB for the RF VCO. Another 6 dB are needed because the VCO is at half of the final frequency. All this translates to a –91 or –97 dBc/Hz at 100 KHz offset for 2.5 GHz VCO (for binary or quaternary mode, correspondingly).

This requirements are stringent but certainly not far-fetched.

Header detection and Channel Estimation

The detection of the header and channel estimation involve both correlation with a binary sequence. We shall illustrate how the mathematical construction of the complementary sequences facilitates a particularly simple construction of a matched filter to such a sequence.

The complementary sequences are formed by a construction

$A_{2n}(z) = A_n(z) + z^n B_n(z)$
$B_{2n}(z) = A_n(z) – z^n B_n(z)$

with $A_0=B_0=1$.

This immediately generates an implementation:

Figure 3: Recursive construction of a filter matched to Golay complementary sequence pair

When we expand this construction we get a telescopic construction:

Figure 4: Telescopic construction of filters matched to Golay complementary sequence pair and subsequences

As we see, the amount of memory elements is still 127, but the number of arithmetic elements (adders and subtractors) dropped from 127 to 12!! Moreover, in this implementation we get for free not only a matched filter to the last sequence, A_{128}, but also to all the preceding subsequences A_1-A_{64} and B_1-B_{64}. In particular, correlation with B_{32} may be used to significantly improve detection performance of the header, as compared with energy detection. Observing the correlator output enables to discriminate the valid header from other random signals.

Another application for the correlations with subsequences A_{32} and B_{32} is initial estimation of frequency offset. Performing dot-product between correlations with subsequences of the header generates a complex variable the phase of which is indicative of a frequency offset.

Equalization and tracking

The receiver utilizes the notion of equivalence between OQM (Offset Quadrature Modulation) at 12.5 Mbaud per quadrature component and PAM (Pulse Amplitude Modulation) at 25 Mbaud. This equivalence is achieved by multiplication of successive samples by j^k (note that this multiplication does not involve arithmetic operations). Therefore the equalization is designed for a PAM signal passing a complex-valued channel.

The Decision Feedback Equalizer (DFE) structure contains Feed-Forward Filter (FFF) and Feed-Back Filter (FBF) parts. The FFF taps involve half of a complex multiplication (two real multiplications), as only real part of the product is required. The taps of the FFF are spaced symbol-spaced (relative to 25 Msymbol/s).

In non-offset modulations fractionally spaced equalizers are typically used to avoid sensitivity to sampling phase. In our case, the use of symbol-spaced equalizer in our case does not introduce such sensitivity, because the aggregate sampling rate in both I and Q channels is 50 Msamples/s, which is more than adequate to represent the 20 MHz signal bandwidth. A back-of-an-envelope calculations show that the complexity here is same as in fractionally spaced equalizer for QPSK (two vs. four multiplications per tap, same number of taps, but twice the number of output samples).

The FBF filter, operating on decisions, consists of low-cost multipliers, as the input data is just couple of bits wide. The computational cost here is also equivalent to QPSK case (one versus four multiplications per tap, but twice the number of taps and twice the number of output samples).

A part which adds to the complexity is the carrier tracking part. Contrary to the QPSK case, where the phase detector is based on same samples that are produced for the decisions, here the phase detection requires additional hardware. That hardware consists of a filter fed by the decisions, which reconstructs the signal at the input (with some delay). The impulse response of the filter is just the channel impulse response, as was estimated from the preamble. Taking the imaginary part of product of appropriately delayed input signal and the reconstructed input signals is the phase detector output which drives the loop filter. The complexity of this part is twice that of the FBF part, however, as mentioned before, this filter operates on 1-2 bit data and therefore the complexity is low.

Equalizer structure is demonstrated in the following drawing:

Figure 5: Digital modem structure – DFE and carrier tracking loop

Let us now address the timing drift. For a 1500 byte frame and 20 ppm drift (10 ppm on each side, opposite directions) the drift at the end of the frame accumulates to 0.25 symbol. This amount is quite significant, and some correction mechanism is desired. The timing tracking is an intricate matter to implement, if the modem is purely digital and there is no control over the sampling process. On the other hand the delay is a filter (with linear phase), so it can be handled through the equalizer adaptation process. Adaptation of the feedforward taps suffices to handle the timing drift.

In addition to the benefit of timing tracking adaptive equalizer also corrects imperfections related to initialization. Imperfect channel estimation, coloured noise, approximate initialization algorithm – all those get improved (if the errors do not kill the reception in the beginning of a packet). Implementation of an adaptive equalizer almost doubles the equalizer complexity, therefore it may be skipped for low-end designs, especially those focusing on binary mode only.

The equalizer initialization algorithm is a complex issue by itself. In an accompanying paper we are showing an algorithm developed by Dr. Dan Raphaeli from Tel-Aviv University, which is highly suited to hardware implementation and making a reuse of hardware already present in an equalizer.

Comparison with OFDM

The OFDM is a good, modern approach to communication over highly dispersive channels. However, we would like to claim that in the context of portable equipment it does not realize its full potential. In the portable equipment the efficiency of the RF power amplifiers is of major importance. In low power equipment the aggregate power consumption is of major importance, but also an instantaneous consumption is of interest. The claim that equalizers for single carrier systems consume several times more MIPS than the FFT machine requires for OFDM reception is correct, however we should pay attention to several details. First is that the machine required for detecting a signal is significantly simpler than the equalizer, therefore in systems with small amount of traffic the power consumption is drastically reduced. In addition, the trend in digital processing is towards smaller gate lengths and smaller power consumption, while in the arena of RF components and especially the efficiency of power amplifiers the progress potential is very limited. The complexity incurred by the equalizer lenghts required for indoor applications are manageable.

OFDM looks as a good choice for Base Station to Mobile Station communications, such as point to multipoint outdoor systems or broadcasting systems (for example, the new Digital Audio Broadcasting standard is based on OFDM), where large PA backoffs are not such a problem, and preprocessing for peak-to-average ratio reduction is cheap. In WLAN scenario, where the mobile stations have to achieve non-negligible power levels, OFDM is a problematic choice.