Submission to
IEEE P802.11
Wireless LANs

Harris/Lucent TGb Compromise CCK (11Mbps) Proposal Selection Criterion

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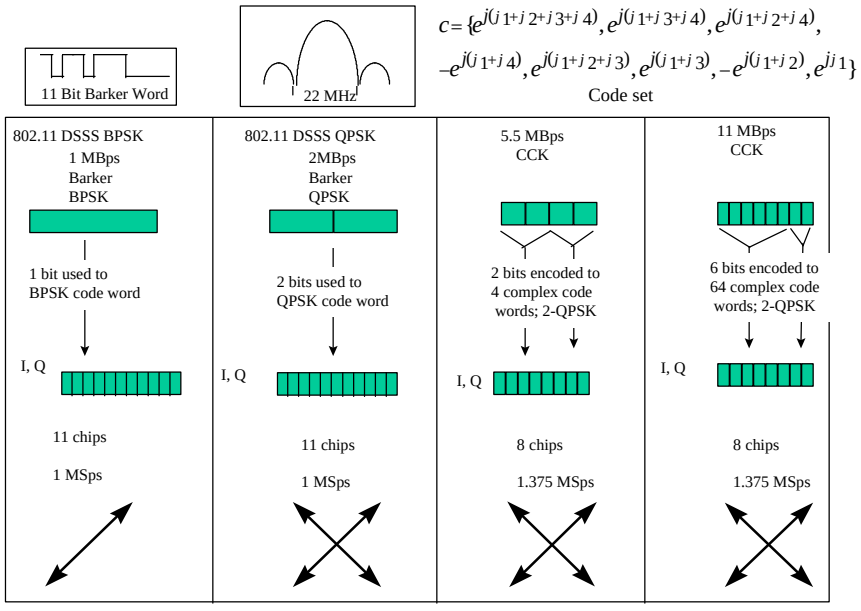
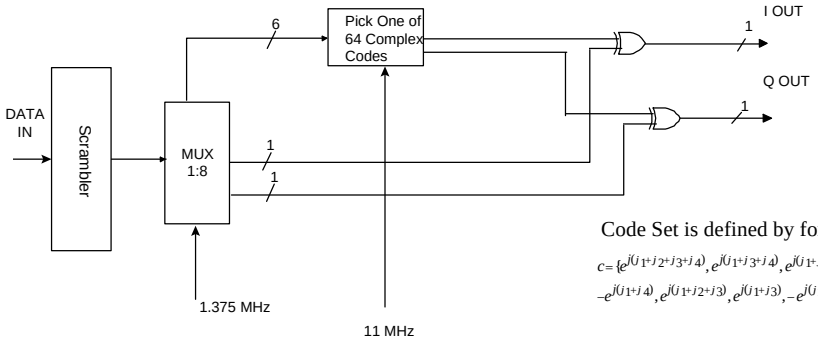
The Evolution of the Waveform

- 1. The Walsh functions used independently on both I and Q channels are subject to cross rail interference.
- 2. By combining the I and Q channel symbols into one complex complementary code symbol, the cross rail interference is mitigated. This new symbol type carries 6 bits and can be QPSK modulated to carry 2 more bits giving 8 bits per symbol as before.

Modulation Technique and Data rates



CCK Modulator Technique for 11 MBps

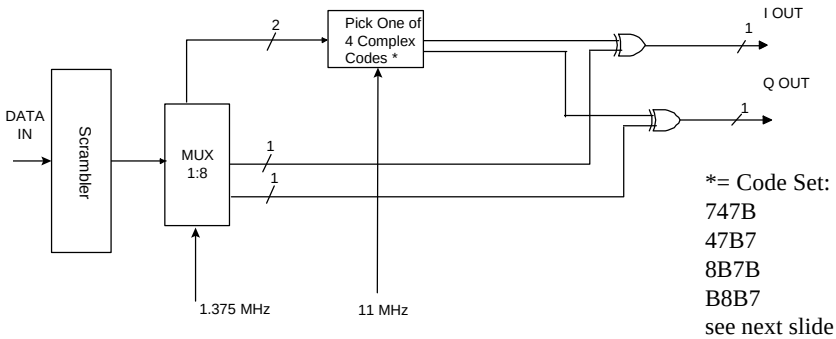


Code Set is defined by formula:

$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\}$

Data Rate = 8 bits/symbol * 1.375 MSps = 11 MBps

CCK Modulator Technique for 5.5 MBps



*= Code Set:
747B
47B7
8B7B
B8B7
see next slide

Data Rate = 4 bits/symbol * 1.375 MSps = 5.5 MBps

Codeword Definitions

The modulator will use I and Q channels to modulate the QPSK and it takes two bits to specify a complex symbol bit, so the hex definition can be:

11h = +1
01h = j
00h = -1
10h = -j

Then the (4) 5.5 Mbit/s base codewords are:

747Bh =	Codeword 1:	$1j$	1	$1j$	-1	$1j$	1	$-1j$	1
8B7Bh =	Codeword 2:	$-1j$	-1	$-1j$	1	$1j$	1	$-1j$	1
B8B7h =	Codeword 3:	$-1j$	1	$-1j$	-1	$-1j$	1	$1j$	1
47B7h =	Codeword 4:	$1j$	-1	$1j$	1	$-1j$	1	$1j$	1

These are QPSK modulated as a symbol to encode two more bits

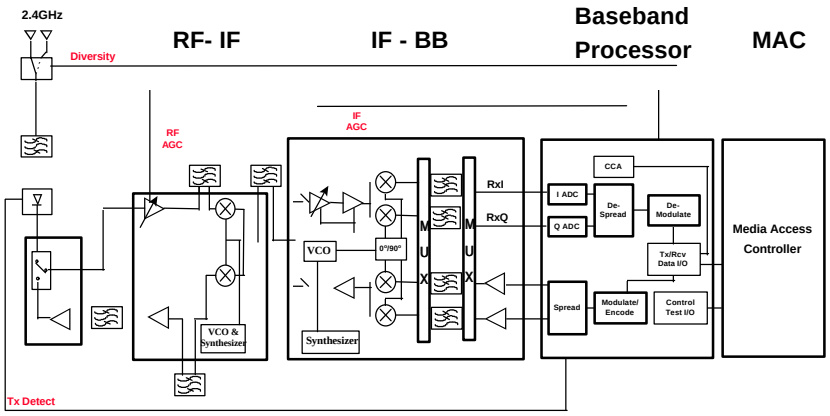
Hardware Impact of CCK vs QMBOK

- The correlators we used to decode QMBOK were two banks of 8 chip serial correlators which required 128 adds per code symbol.
- The 64-ary correlator with the Fast Walsh transform requires 64+32+16 complex adds.

RF/IF Complexity relative to current low rate PHY

- Basically uses same RF and IF as existing 802.11 DS PHY.
- RAKE/ Equalized version replaces the IF limiter with AGC and has more A/D converter bits.
- A combined DS/FH mode uses non optimal wideband IF filters with some loss of performance in a crowded environment.

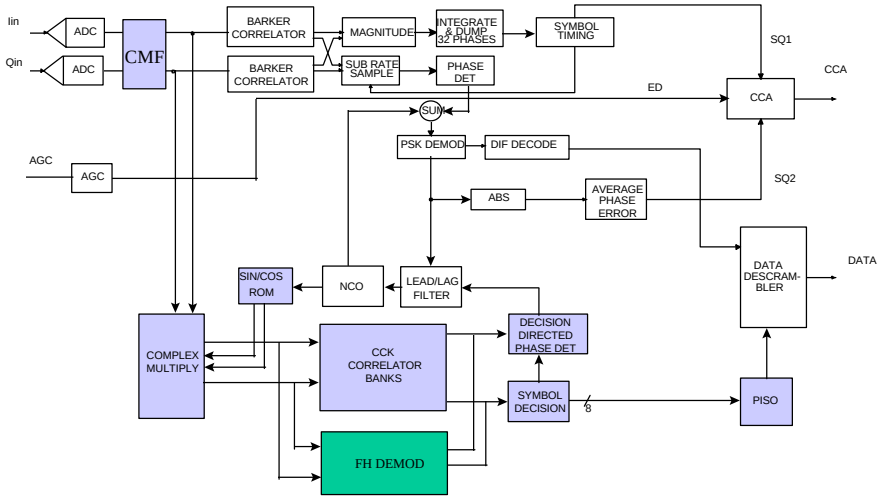
Receiver Implementation



Baseband Processing Complexity relative to current low rate PHYs

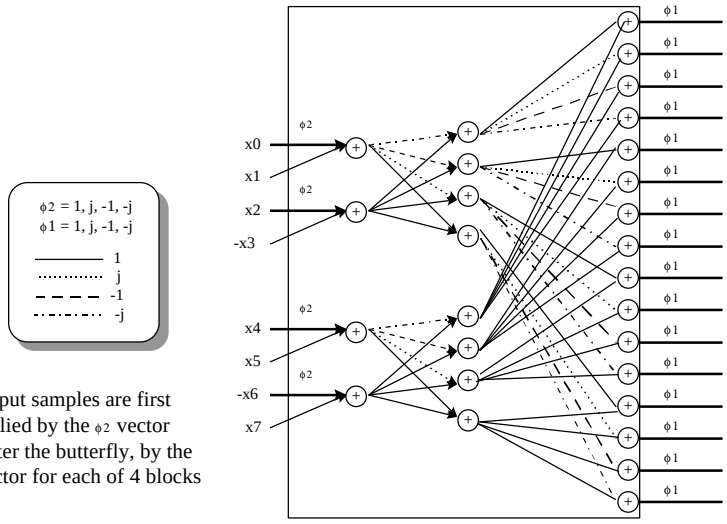
- Addition of high rate with limited receiver increases the DS only baseband processor complexity from 28K gates to 40 K gates.
- Addition of 6 finger RAKE (Channel Matched Filter) to increase delay spread from 40 to 90 ns takes an additional 30 K gates.
- The addition of high rate to FH has not been fully worked out yet.

DEMODULATOR BLOCK DIAGRAM



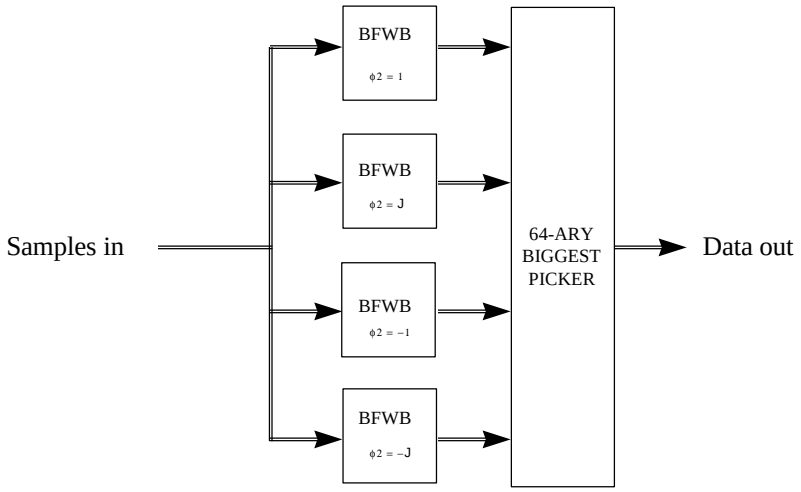
SHADED BLOCK ARE THE ADDITIONS TO DS FOR FH AND HIGH RATES

BASIC FAST WALSH BLOCK (BFWB)



The input samples are first multiplied by the $\phi 2$ vector and after the butterfly, by the $\phi 1$ vector for each of 4 blocks

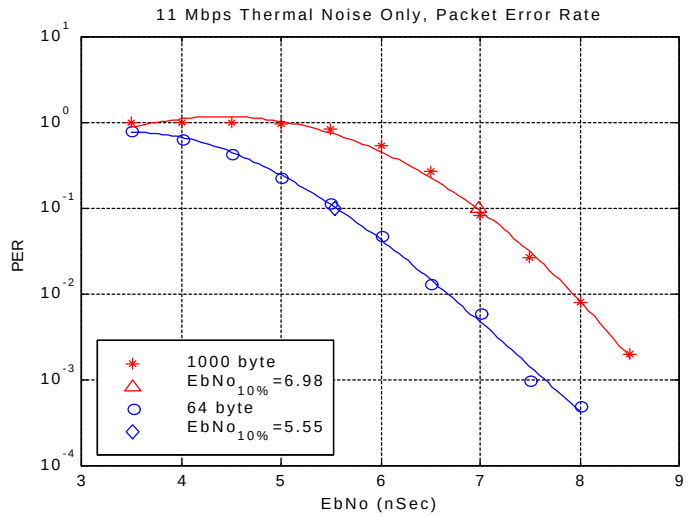
8 CHIP COMPLEMENTARY CODE DECODER



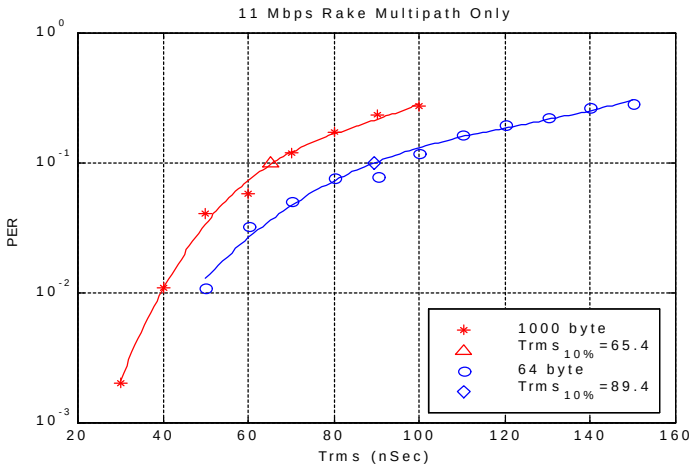
Antenna Diversity and performance impact

- Antenna diversity can improve the performance of the link less costly than an equalizer but not as much.
- The performance impact has shown an improvement of a factor of 8 in PER in field testing.
- The negative impact is to require additional time in the preamble on the order of 16 us (already covered by the 802.11 preamble).

PER Vs. Noise



PER Vs. Multipath Only (No Noise).



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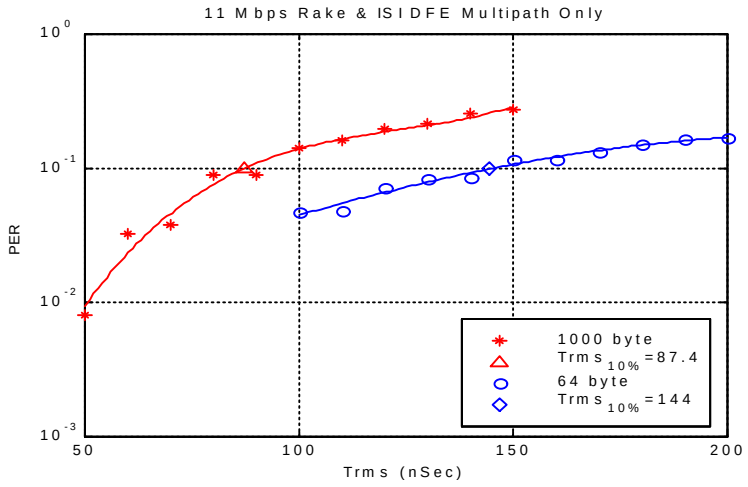

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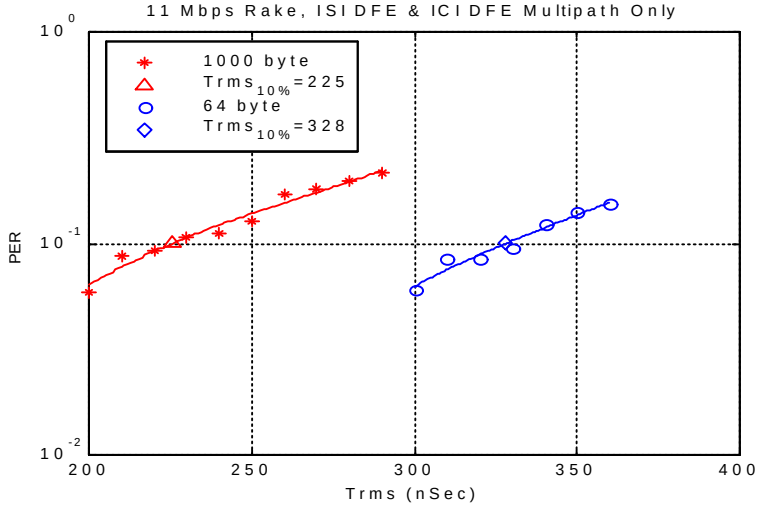

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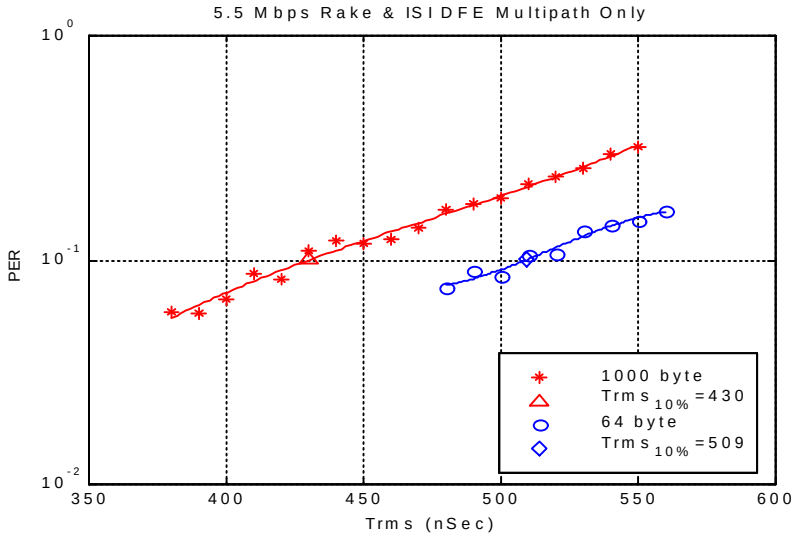
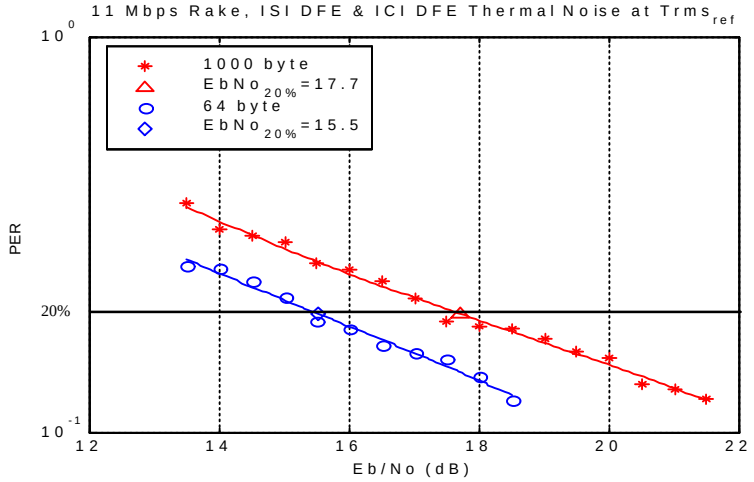


PER Vs. Thermal Noise with Multipath at 10% PER. Eb/No at 20% PER for 64 and 1000 byte packets.



Required Carrier Frequency Accuracy

- The new high rate PHY requires the same carrier frequency accuracy as the existing low rate PHY.
- The DSSS limitation is that the maximum carrier frequency offset should be less than 1/8 th of the symbol rate of the preamble.

Required Data Clock Frequency Accuracy

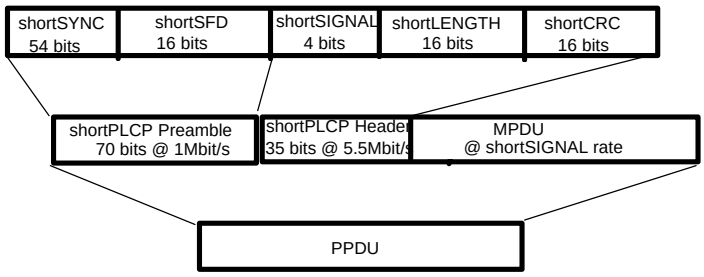
- The new high rate PHY requires the same clock frequency accuracy as the existing low rate PHY.
- We recommend that the data clock be tied to the carrier frequency reference, so that optimizations can be achieved in the symbol tracking circuits.

Preamble Length

- Our basic approach is to include the standard DS or FH 802.11 preamble and header.
- This length includes ample time to do diversity and equalization.
- For the cases where interoperability is not an issue, a short, high rate header can be used.
- Antenna diversity, WEP initialization and equalizer training require a somewhat longer short preamble than the shortest possible.

Interoperability / Coexistence,

short PPDU frame format



ShortSYNC: 54 scrambled all zero's **used for receiver synchronization:**

e.g 30 microsec for CCA @ 20 microsec slottime with or without antenna diversity

shortSFD: bit reverse of original SFD

Slot Times

- We propose no change in the DS PHY slot time of 20 µs or FH slot time of 50 µs.

CCA mechanism and Co-Channel signal detection time

- We measure the correlated signal energy in the preamble over 5 µs dwells beginning when the receiver is enabled and compare that to a threshold.
- The detection time is less than the slot time by enough to include diversity.
- FH detection is done on clock energy in similar dwells.

RX/TX turn around time and SIFS

- The transmitter has a 1.3 µs processing delay from bits in to bits out the antenna.
- The receiver has 3.3 µs processing delay from bits in the antenna to bits out.
- The RX/TX turn around time is less than 2µs exclusive of the above delays.
- We propose the existing DS 10 µs SIFS.

Channelization Scheme

- We propose the existing DS channelization scheme.
- Three non overlapping channels in the band
- A choice of 5 MHz channel centers with 11 channels in the ISM band for the US and 13 in Europe.
- One channel for JAPAN.

Adjacent Channel Interference Rejection

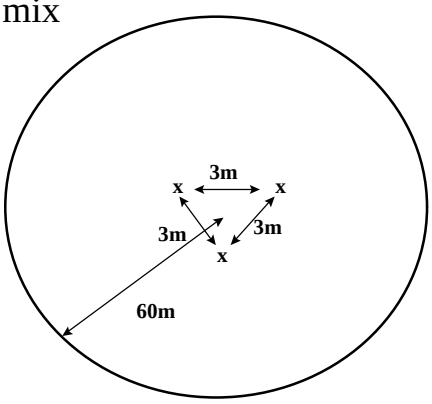
- 6 dB more filter skirt rejection and/or sidelobe attenuation is needed to achieve the same ACI rejection as the existing low rate PHY to account for the difference in SNR required in the spread bandwidth.

Cell planning and ACI

- 3 frequency channels where same frequency of different cells share.
- ACI must be such that a 3 channel solution is possible.
  - interferred devices will fall back in rate
  - system throughput more essential than the ACI figure

Adjacent channel interference

- ACI @ 25 MHz separation: 30 - 35dB
  - makes a 3 frequency channel topology possible at certain distance mix
  - 3 X throughput



Co-channel interference

- CCI is expected to be in the same range as the original Harris proposal.
- Improvement because of better codes.
- Initial simulations show 5-6 dB CCI.

PER VS SNR for CCI

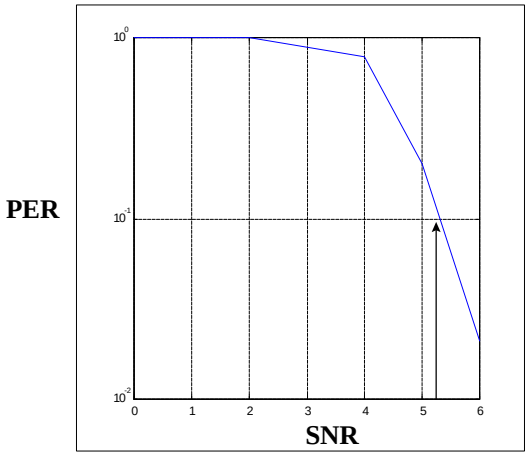


Figure 2: Packet error ratio versus signal-to-interference ratio in dB for CCI.

Interference immunity

- Immunity to CW jamming is expected to be in the same range as original Harris proposal.
- Improvement because of better codes.
- Initial simulation show ~5.5 dB S/J

PER VS SNR for CWI

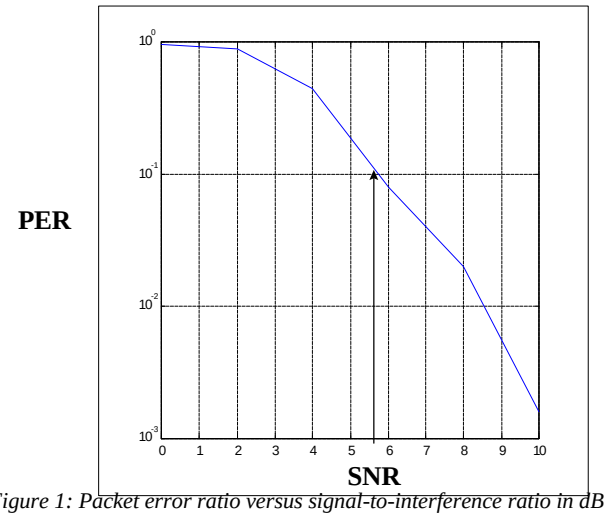


Figure 1: Packet error ratio versus signal-to-interference ratio in dB for CWI.

Phase Noise Sensitivity

- There is no particular phase noise sensitivity with the proposed waveform. It performs as well in phase noise as any QPSK scheme.
- The measured phase noise of our receiver's LO which performs well is 2 degrees RMS.

RF PA Backoff

- The CCK waveform needs about 4 dB of PA backoff to insure low regrowth of spectral sidebands.
- This is the same as the DS BPSK preamble requires.
- Substantially better than BCPM.

DC power consumption

- The current, non equalized HFA 3860 QMBOK chip draws 30 mA at 3 VDC with 0.6 micron technology. This represents about 12% of the radio receiver DC power.
- We do not expect the current consumption of the simplest CCK receiver to differ from this.
- With 0.35 micron technology, the most complex approach will be about the same.

Patent Submissions

- The Harris position is that we will only patent techniques having to do with our chip implementation. (See Harris' patent submission)
- Lucent has not done any patent search and is not aware of any relevant patents.
- Anything likely to be embodied in the standard will be free of license from Harris.
- The CCK waveform is public domain.

Interoperability / Co-existence strategy with current low rate PHYs

- Interoperable via use of existing low rate preamble and header, either DS or FH.
  - In the case of the FH PHY, the low rate preamble and header must be followed by a short high rate header to re-establish antenna diversity and to train the equalizer.
- Will defer or cause deferral via 802.11 mechanisms currently in place.

Is the proposal Interoperable at the data and antenna levels?

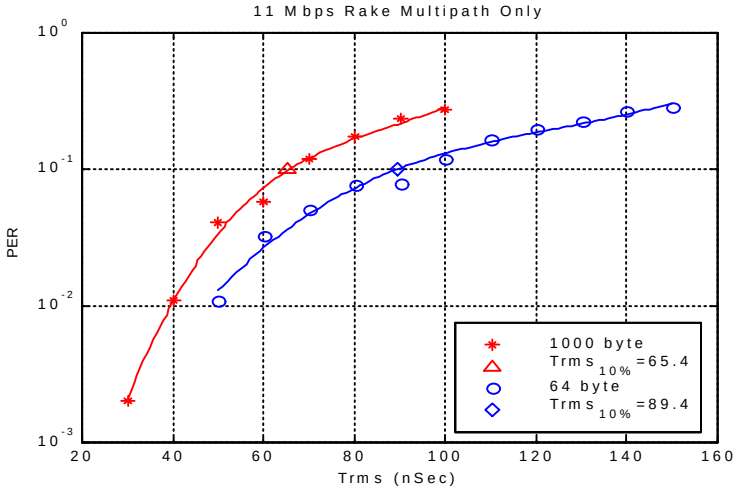
- Yes!

Performance penalty due to Interoperability / Coexistence.

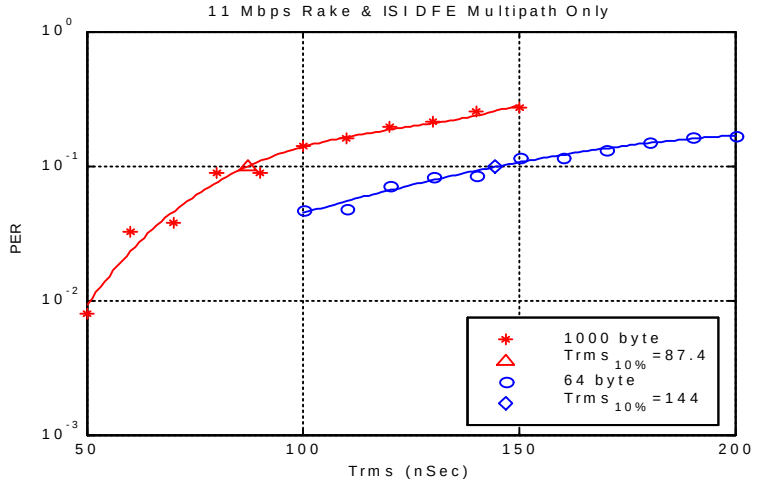
- The DS overhead is 192 µs Vs about 75 µs without interoperability
- The FH overhead is 128 + 10 + 75 µs or about the same
- This amounts to ~20 % on 1K byte packet
- The short preamble and header will be about 75 µs or about 10% overhead on a 1000 byte packet.

Additional simulation data

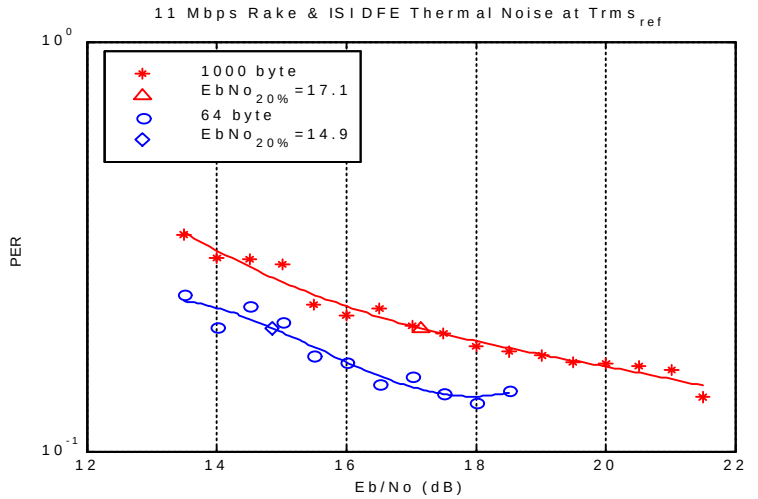
11 MBps RAKE only Multipath only



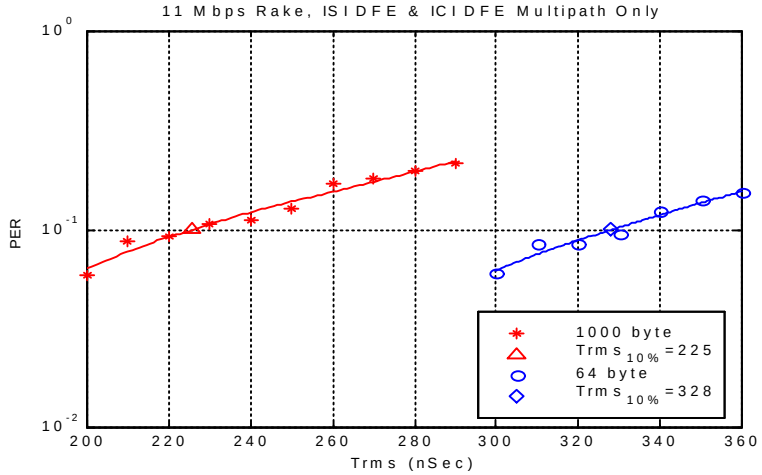
11 MBps RAKE, ISI Multipath only



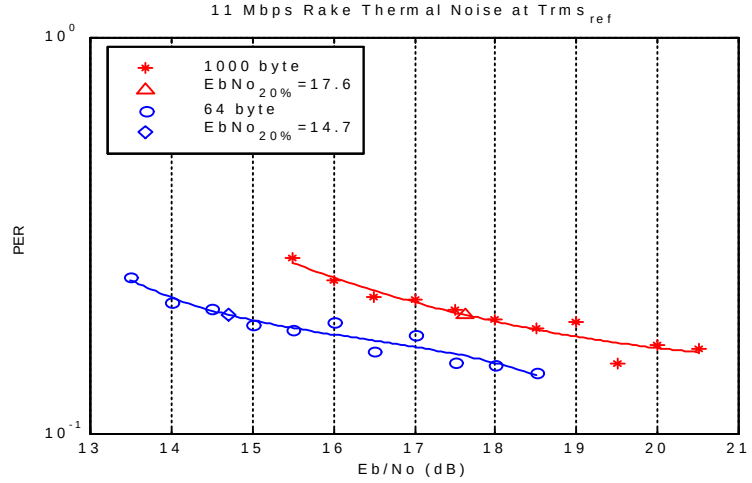
11MBps RAKE & ISI DFE (Noise and Multipath)



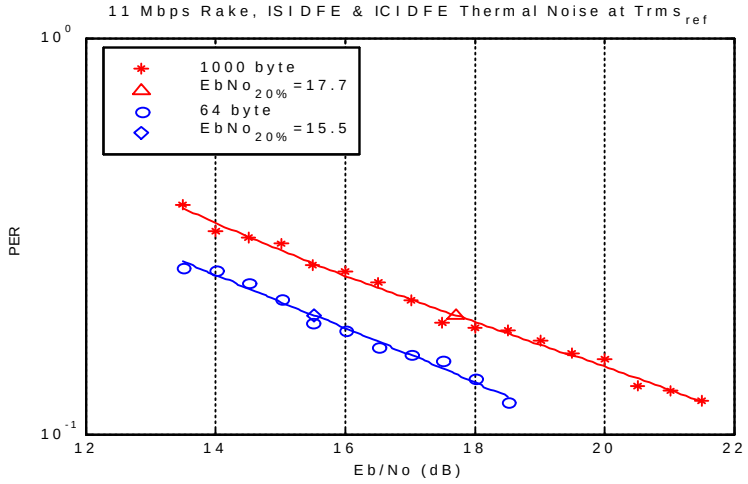
11 MBps RAKE, ISI, ICI Multipath only



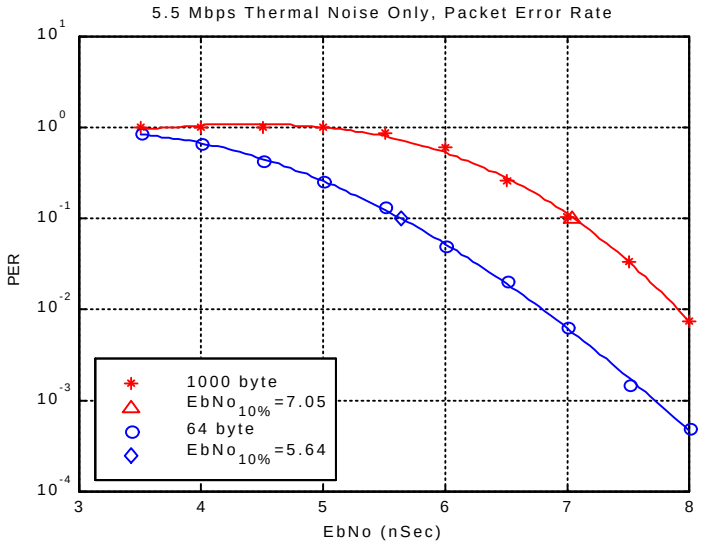
11 MBps RAKE only (Noise and Multipath)



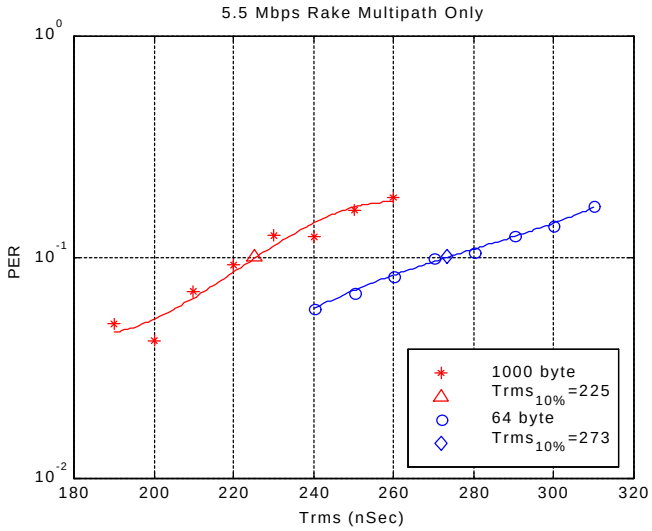
11 MBps RAKE, ISI, ICI (Noise and Multipath)



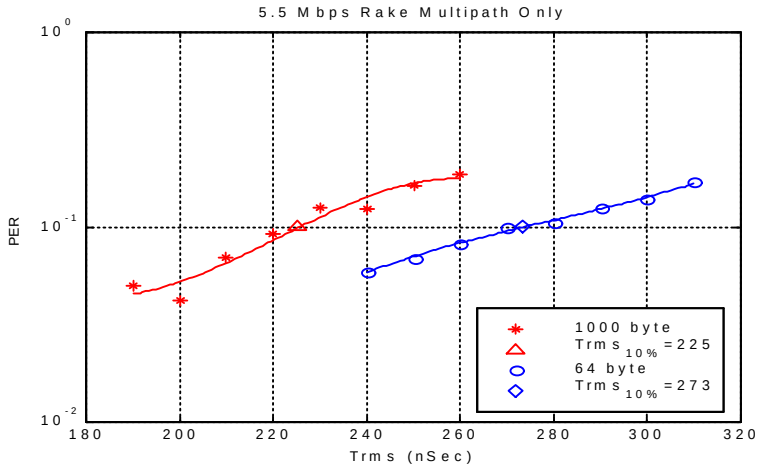
5.5 MBps Noise only



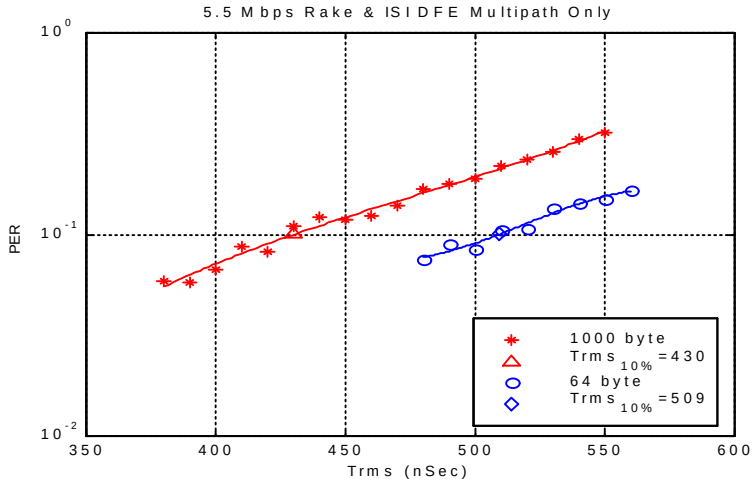
5.5 MBps RAKE, (Multipath only)



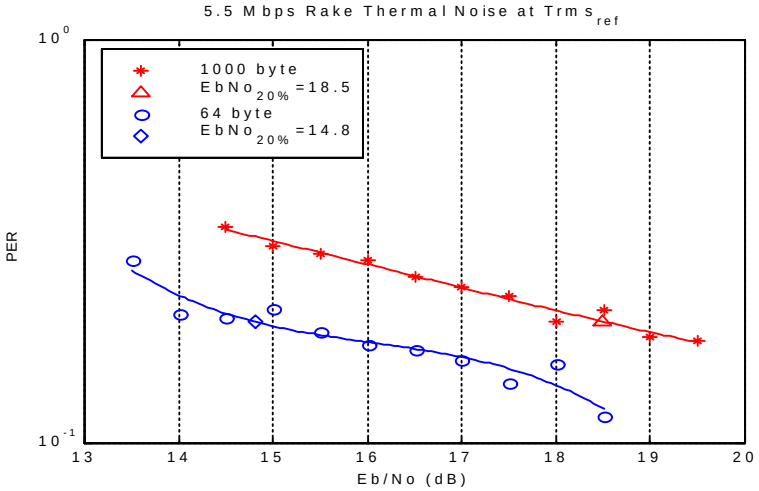
5.5 MBps RAKE only (Multipath only)



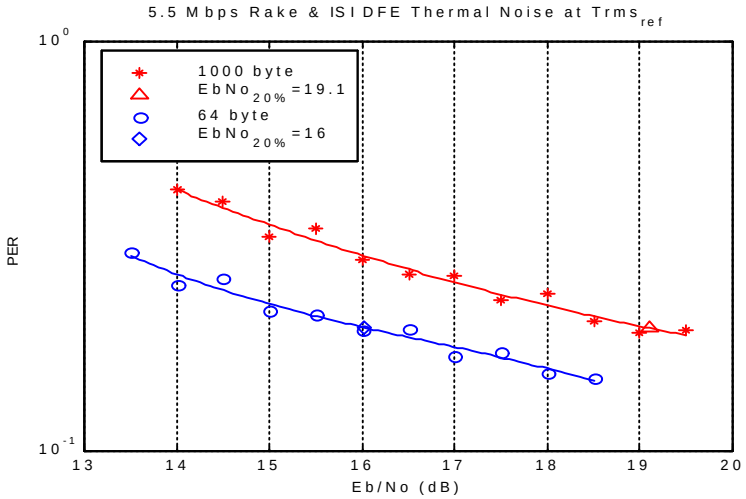
5.5 MBps RAKE, ISI (Multipath only)



5.5 MBps RAKE only (Noise and Multipath)



5.5 MBps RAKE, ISI (Noise and Multipath)



5.5 MBps RAKE, ISI (Noise and Multipath)