Submission to:
IEEE P802.11
Wireless LANS

Title: **Proposal for a High Speed PHY for the 2.4 GHz band**

Date: January 1998

Authors: Mark Webster, Carl Andren, John Fakatselis, Kent Rollins, Victor Lucas, Bob Rood, Bill Hortos
Harris Semiconductor
2401 Palm Bay Road
Palm Bay, Florida
32905
USA
Tel: (407)-724-7000
Fax: (407)-724-7886
email: krollins@harris.com

1. Introduction

Harris is proposing a High Rate PHY extension for the 2.4 GHz band. The basic approach offers a maximum of an 11 Mbps data rate at the PHY level. It can be enhanced with optional features to accommodate various applications and /or operational environments.
Figure 1.0 illustrates a summary of the basic approach as well as the various options that are being proposed by Harris.

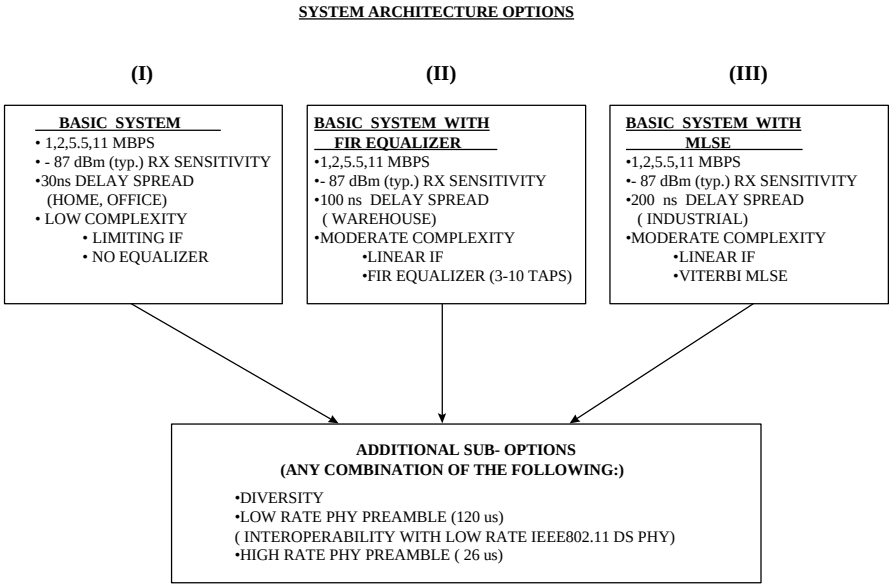


Figure 1.0 Harris High Rate PHY solution summary.

Some of the key aspects of the Harris solution include:

- A maximum data rate of 11MBPS , with the capability to fall back to lower rates of 5.5, 2 or 1 Mbps in demanding environments or when additional range coverage is required.
- Bandwidth utilization per channel equivalent to that of the Low Rate 802.11 DS PHY which can allow a minimum of 3 simultaneous channels within the allocated band.
- Full compliance with the 802.11 MAC as defined in its present form.
- The ability to switch into a high rate preamble improving the system data throughput when interoperability with low rate 802.11 DS PHYs is not required. The system can be backwards interoperable with the 1 and 2 Mbps DS 802.11 PHY .
- The implementation has many similarities to the Low rate DS PHY, mitigating the risk of implementation feasibility. The 11 Mbps solution can essentially be implemented with the same RF and IF front as in the low rate DS PHY.
- The basic approach addresses multipath environments of up to 30 ns delay spread (Home, office applications).Optional enhanced architectures to meet 100 and 200 ns delay spread requirements (warehouse, industrial applications) are also proposed. These enhanced architectures are based on the basic waveform and are fully interoperable with each other.
- Any of the architectures can be used with two antenna receive diversity, the low rate preamble or the high rate preamble for improved system throughput.

Empirical data is available through a prototype developed , by Harris, in PCMCIA form factor. This prototype is an implementation of the basic waveform (lowest level of complexity and performance). The data confirms the performance and the design itself proves implementation feasibility.

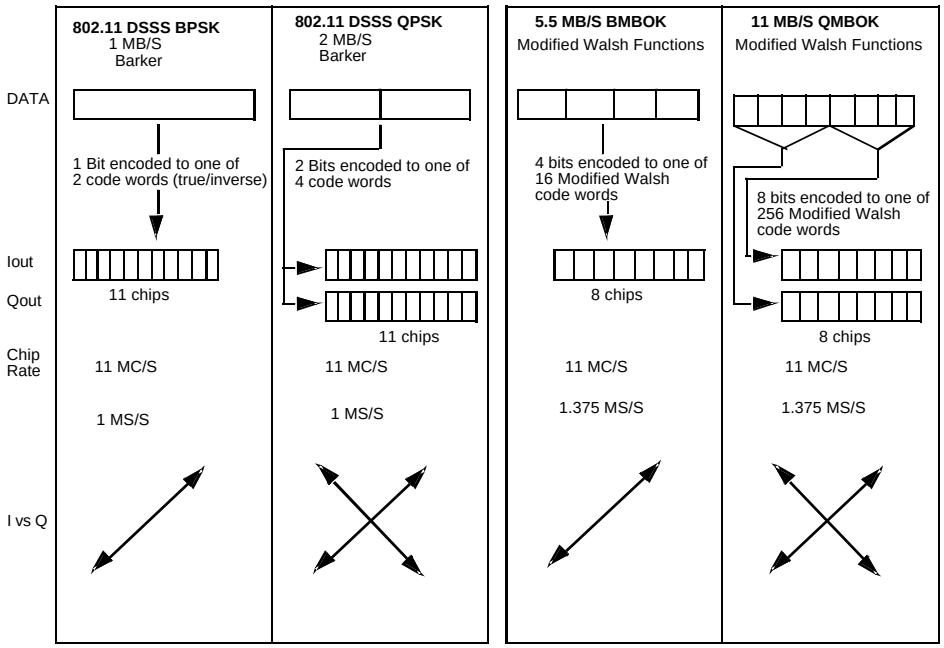
The proposal includes a description of the basic waveform, a system overview, implementation details including schematics and a Bill of Material (BOM).
It continues with an overview of multipath issues and modeling. The enhanced architectures to achieve higher multipath resistance are also described. A FIR equalizer and an MLSE based option is described.
The proposal continues with a description of the receive diversity algorithm and implementation. Spectral efficiency curves are included derived from empirical data from the Harris PCMCIA prototype.
Co-channel and adjacent channel data are attached.

The proposal also addresses interference analysis . The waveform has been tested against CW, narrowband 802.11 FH, and broadband noise.

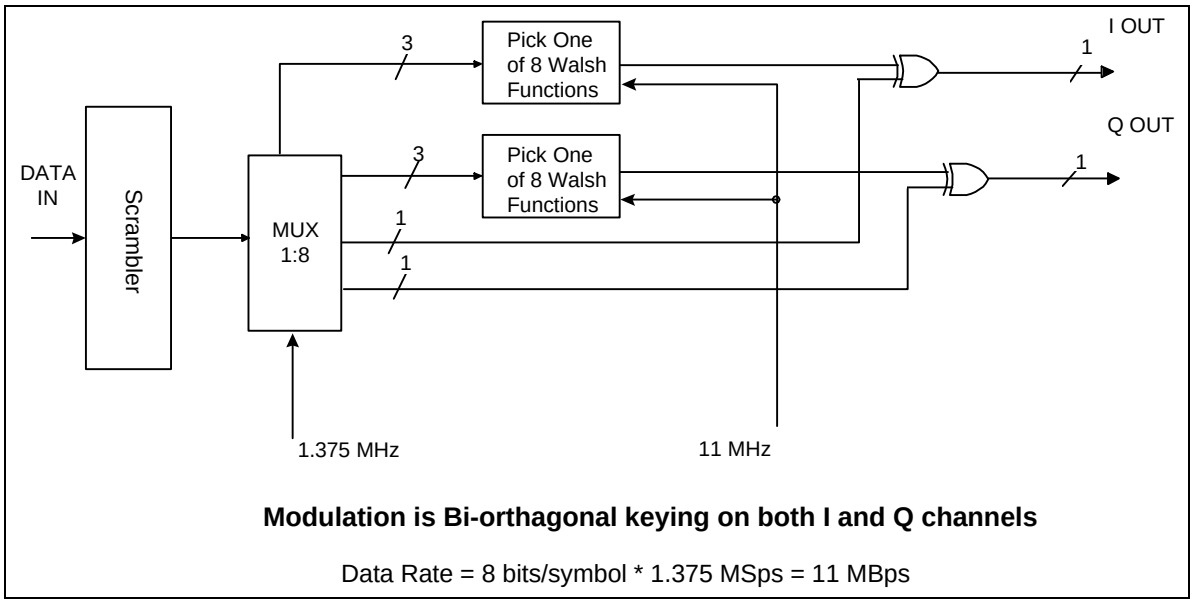
Overall the Harris proposed solution is the result of an exhaustive trade off of alternatives to conclude in what we believe is the best performance vs. complexity solution, with the capability for upgrading to optional interoperable architectures providing enhanced performance capabilities.

2. Overview

Harris Semiconductor proposes a technique for the high rate PHY that uses M-Ary Orthogonal Keying as previously described in IEEE 802.11. 97-144. This technique uses 8 chip symbols where the spread sequences are determined by the data. This allows the waveform to carry up to 8 bits per symbol at a symbol rate of 1.375 MSps for a net data rate of 11 MBps.



This technique has been thoroughly analyzed and also implemented in silicon. A reference radio using the technique has been extensively tested and has also submitted to the FCC for approval of the modulation scheme. Variations to improve its multipath performance where performance can be traded for complexity have been analyzed and are reported here. The technique is capable of two higher rates, 5.5 and 11 Mbps. The analysis is generally performed at the packet size of 1000 bytes or 64 bytes where applicable. The transmitter structure for implementing the waveform is shown below.



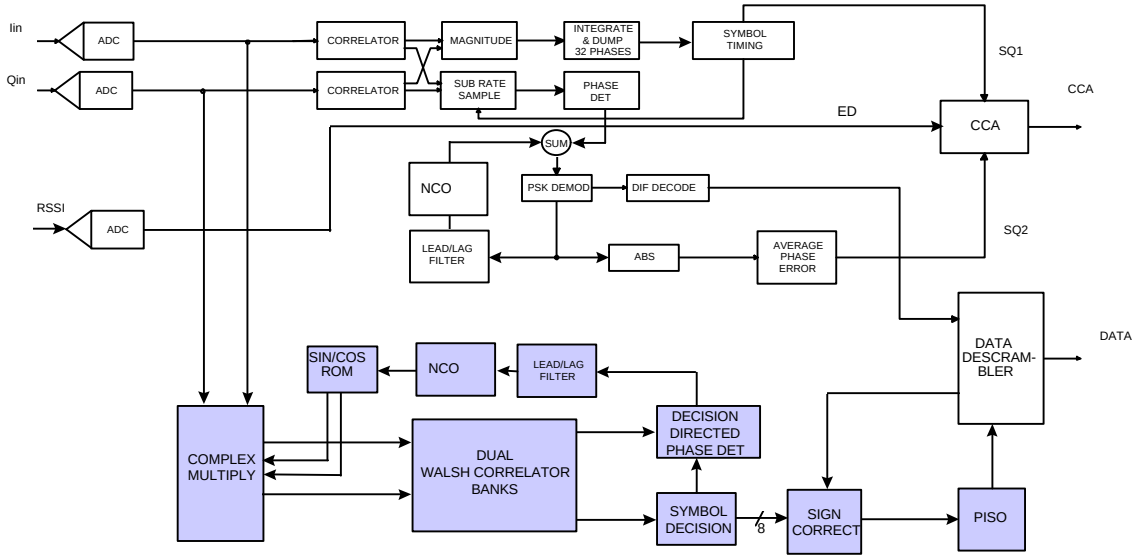
Modulation is Bi-orthagonal keying on both I and Q channels

Data Rate = 8 bits/symbol * 1.375 MSps = 11 MBps

2.1 Receiver structure

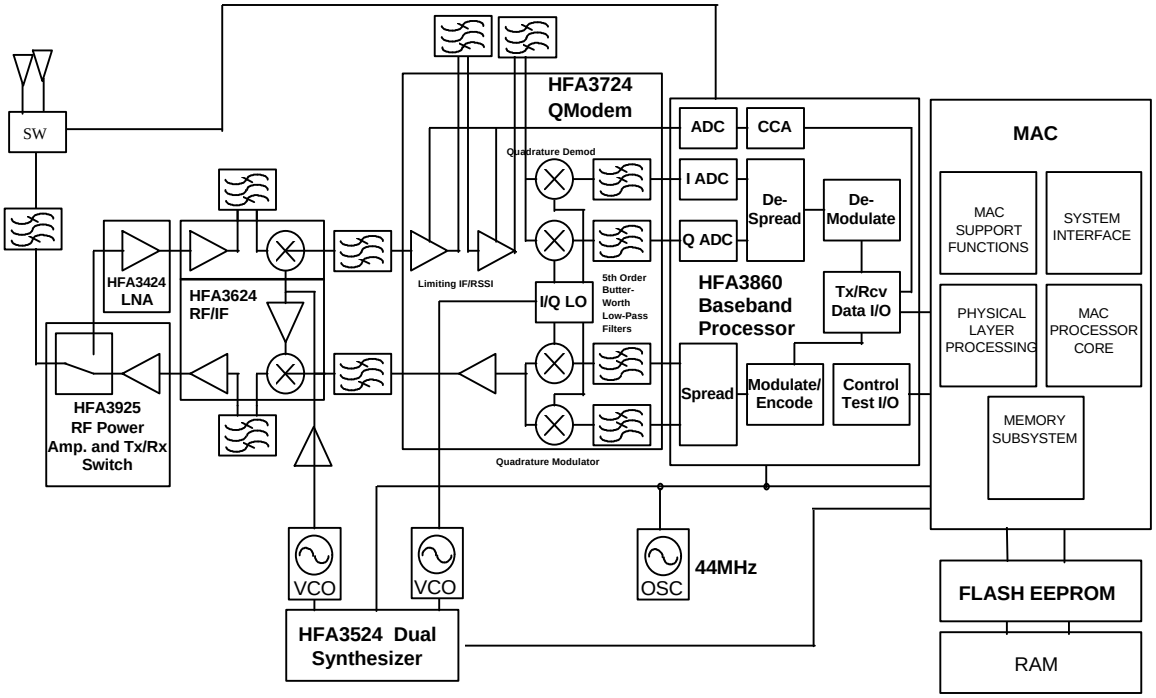
The receiver structure has been previously been described with the exception of the equalizer enhancements for handling higher delay spread requirements than the basic system. A sample of a compatible low rate/ high rate demodulator is shown below.

HFA 3860 DEMODULATOR BLOCK DIAGRAM



SHADED BLOCK ARE THE ADDITIONS FOR HIGH RATES

The radio block diagram shows that the technique being proposed can fit well within the existing radio structures. The primary changes to the radio design going from the basic design to the full complexity design with MLSE equalizer is the change for limited IF to linear IF with AGC.



2.2 Immunity to Multipath and Noise

The Basic technique has been shown to have 30-40 ns of multipath delay spread capability without noise assuming 8% PER. This performance can only be derived from analysis since there is no defined test procedure. When combined with a suitable equalizer, the system can be shown to tolerate 100 ns of delay spread at 8 % PER.

The performance in thermal noise only has been shown on the test hardware to typically be -85 dBm at 11 Mbps and 1.0e-5 BER. The lower 5.5 Mbps rate has a typical performance of -87 dBm at 1.oe-5 BER.

The above performance has been verified using a reference radio constructed to the performance requirements of the existing standard. This includes the channel spectral mask, the oscillator accuracy, and the synchronization preamble and header. The existing header, backoff mechanism, and slot times have been retained for backwards compatibility and interoperability. The rates are easily described by the existing rate change mechanism in the current header. The co and adjacent channel performance has been measured and is similar to the existing standard with allowance for the about 8 dB higher SNR required. The radios have been subjected to the FCC's CW jamming test. In addition simulated FSK FH signals and broad band noise. The radios have passed these all of tests.

2.3 Critical Points

The new baseband processor chip uses 30 mA from 3.3 volts at the 11 Mbps rate. The power consumption of the new chip developed is essentially the same as the chip developed for the existing standard because we eliminated some features for flexibility that were not needed to meet the standard. It is felt that when the implementation uses power saving techniques where the high or low rate sections are turned off as needed, the power consumption will be the same. When an equalizer is added, this may double the baseband processor power consumption.

There is no extreme sensitivity to phase noise or PA backoff. The waveform is the same as the existing standard with respect to amplitude components of the waveform, so the PA backoff needs to be in the 5 dB range. The enabling technologies are standard CMOS processes.

2.4 IP Position

The IP position of Harris Semiconductor is that we have developed a technique that is essentially textbook and all features that would likely be embodied in the standard would not be Harris IP. What we have patented is the detailed implementation of the chip and would consider licensing arrangements for this design if desired.

2.5 Alternative Approaches

There are alternatives that can be considered (80207r1.doc) that slightly modify the basic technique. The first of these is offset QPSK for the basic waveform. This will allow a lower backoff in the power amplifier and also allow the waveform to be described in terms of 22 MCps spread rate.

3. MULTIPATH ANALYSIS AND ARCHITECTURES

The following section provides an overview of the multipath problem, the model and assumptions. It concludes with the proposed architectures that work with the basic Harris waveform to combat multipath using cost effective implementations.
The analysis of the Harris proposed waveform without equalization has also been included. This low complexity basic approach is practical for applications were multipath requirements are not demanding.

3.1 INTRODUCTION TO MULTIPATH MITIGATION

HARRIS is pleased to propose high-performing, low-complexity techniques for mitigating multipath at the high data rates of 5.5 and 11 Mbps. The explanation of HARRIS'S proposal will center on 11 Mbps. The modifications needed to down-scale to 5.5 Mbps are straight-forward.

Only the multipath performance results will be presented. Insufficient time was available to finalize the performance in thermal noise and thermal noise with multipath. HARRIS should shortly be able to provide these results, establishing a comprehensive performance description.

HARRIS'S signal processing techniques provide theoretical performance of less than 10% packet-error-rates at multipath spreads up to 200 nsec RMS.

HARRIS'S proposal is unique in exploiting a certain characteristic of the multipath channel other proposals ignore. Statistically, the predominate channel-impulse-response energy follows the impulse response peak. Also, HARRIS avoids the data-rate capacity loss which naturally occurs when the signal is burdened with other constraining waveform properties.

These strategies are shown to be smart when trying to achieve a high bits/Hz spectral efficiency at low complexity.

HARRIS' technique works with the existing preamble or with a new short preamble. Only an accurate channel impulse response estimate is needed to configure the demodulator for data-mode tracking.

HARRIS'S multipath analysis was performed at 8 samples per chip, using realistic modulator/demodulator filters.

3.2 LINEAR CHANNEL DISTORTION

This section describes the amount and types of linear distortion that the receiver must cope with. For good performance the distortion must be compensated. The compensation techniques can increase complexity. The source of the linear distortions is shown in Fig. 3.2-1.

Figure 3.2-1 The key system components inducing end-to-end linear distortion.

3.2.1 MODEM FILTER EFFECTS

Fig. 3.2.1-1 shows the modulator/demodulator filters used in the HARRIS design. The transmit filters must meet a spectral mask. Limiting bandwidth consumption is important for multi-user occupancy. The receive filters limit noise, interference and control frequency translation distortion. HARRIS has selected cost effective filters. HARRIS is using models of these filters in all the performance analysis.

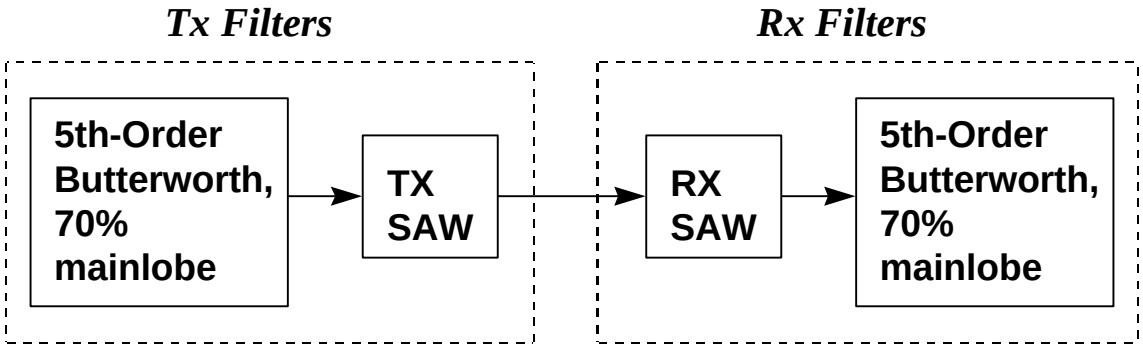
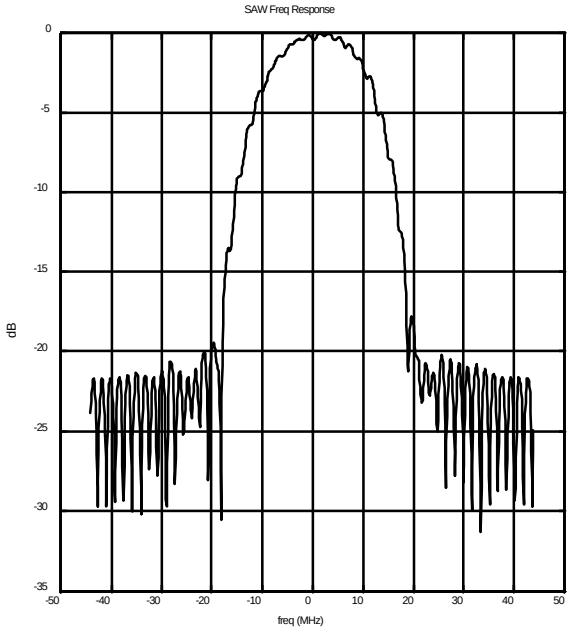
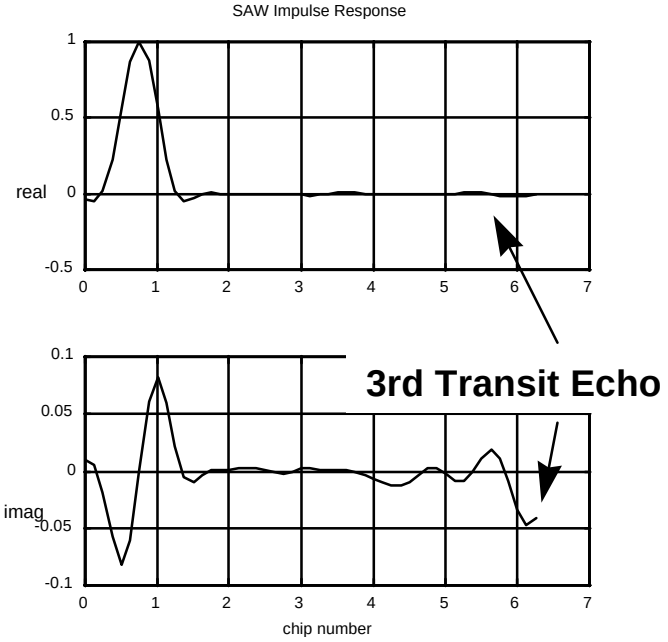


Figure 3.2.1-1 Linear distortions under the designer's control.

Fig. 3.2.1-2 shows the lab-measured characteristics of the SAW filters. Note the presence of the 3rd transit echo. This is a characteristic of SAW filters.



(a)



(b)

Figure 3.2.1-2 Real SAW filter characteristics. (a) Frequency response. (b) Impulse response.

The resulting modulator/demodulator impulse response is shown in Fig. 3.2.1-3. The filters cause multiple-chip-duration distortion. This distortion must be included for realistic analysis. The modem filter's impulse response is convolved with the multipath channel fingers. This causes a significant smearing of the channel fingers.

Notice that the filters cause a non-trivial amount of eye closure in the scatter plot. Techniques which combat multipath help also mitigate the distortion caused by the modem filters.

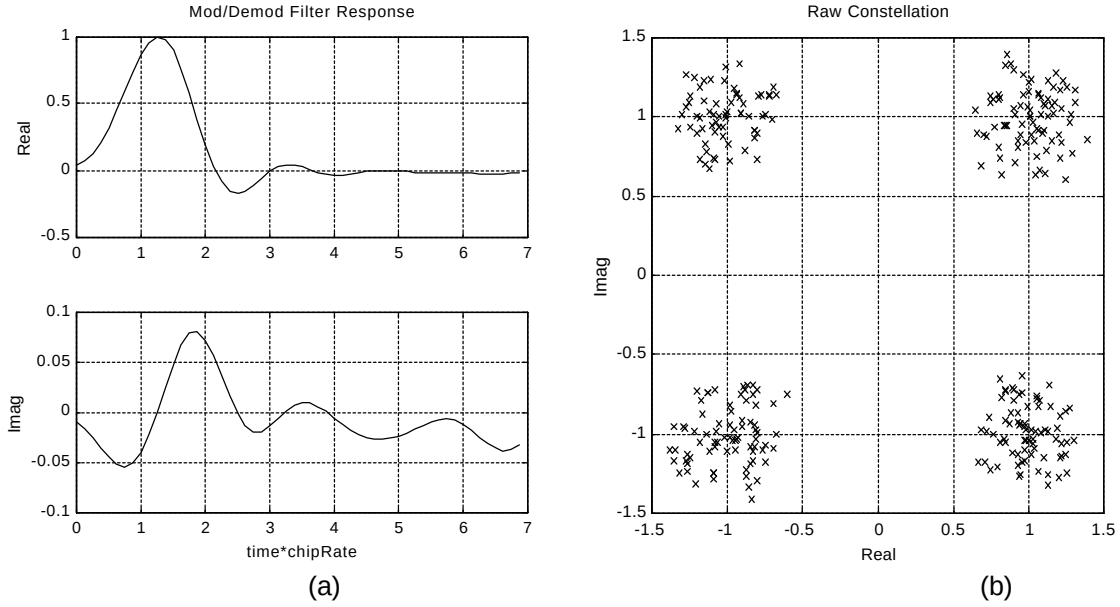


Figure 3.2.1-3 End-to-end modem filter response.

3.2.2 MULTIPATH CHANNEL EFFECTS

This section examines the exponentially-decaying Rayleigh fading multipath model being used to estimate performance. Fig. 3.2.2-1 shows the characteristic. This model uses many multipath components. They are finely spaced. HARRIS retained all energy until the tails contained only energy more than 30 dB down.

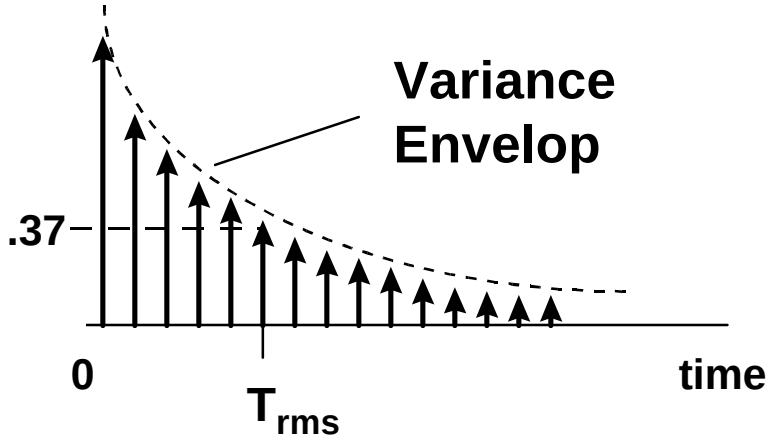


Figure 3.2.2-1 Discrete exponentially-decaying Rayleigh fading channel model. A stochastic realization consists of complex Gaussian RV's at each discrete instance.

A stochastic realization for 100 nsec RMS multipath is shown in Fig. 3.2.2-2. HARRIS used 8 samples per chip. The chip rate is 11 MHz. The impulse response typically spans 6 to 8 chips for the 100 nsec RMS spread channel. It appears the coherent bandwidth is about 0.5 MHz.

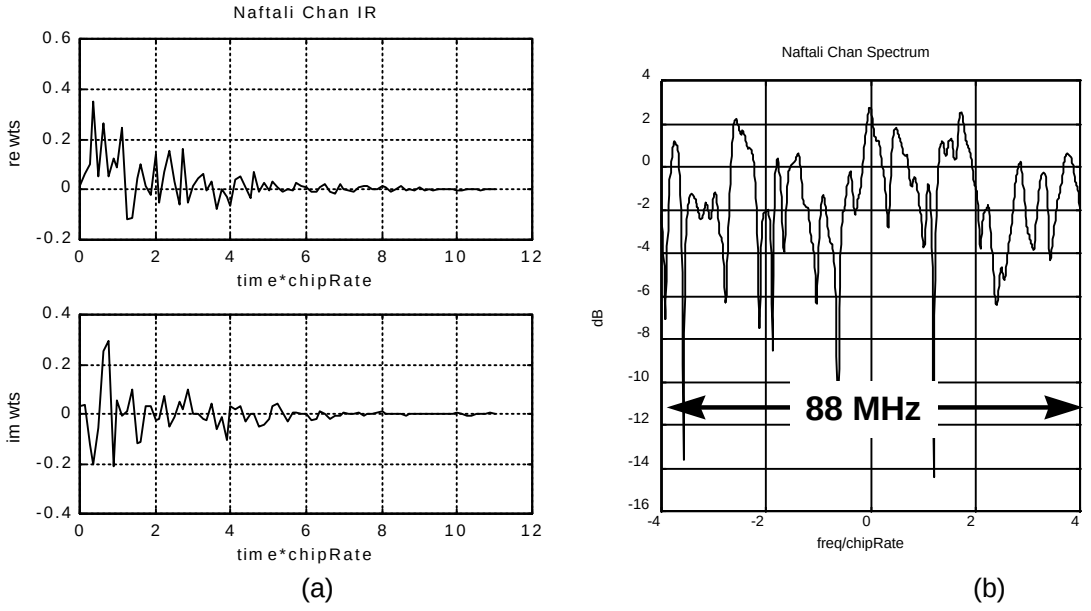
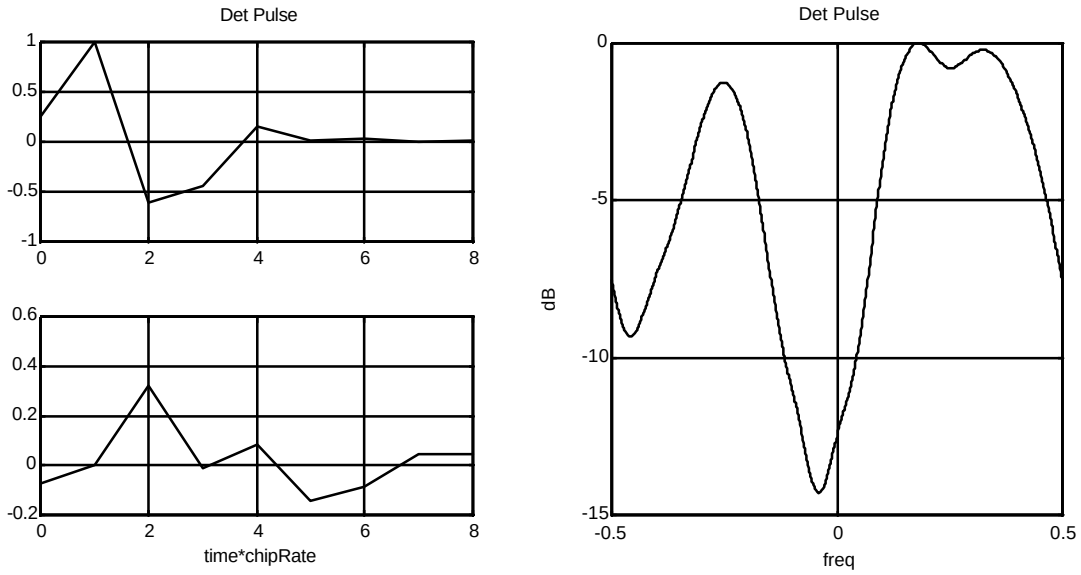


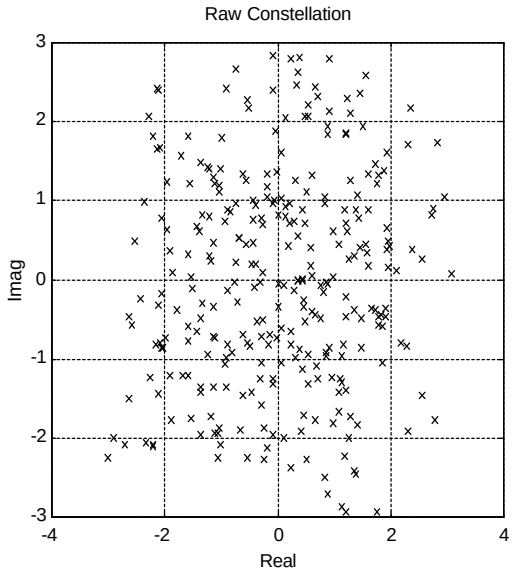
Figure 3.2.2-2 Exponential decaying fading example. A stochastic realization for the 100 nsec RMS delay-spread case is shown.

3.2.3 END-TO-END EFFECTS

This section examines the linear filtering effects extending end-to-end. Fig. 3.2.3-1 shows a stochastic realization for the 100 nsec RMS multipath spread case. The signal has been decimated to 1 sample/chip about the impulse response peak. The 100 nsec RMS delay channel typically spreads energy across 6-8 chips.



(a) (b)



(c)

Figure 3.2.3-1 Modem/channel cascade example. A stochastic realization for the 100 nsec RMS delay spread case is shown. (a) Impulse response. (b) Frequency response in Nyquist bandwidth. (c) Corresponding constellation.

Fig. 3.2.3-2 shows a stochastic realization for the 200 nsec RMS multipath spread case. Here the energy is typically spread across 12-16 chips. The Barker word is limited in its ability to estimate channel impulse responses this long.

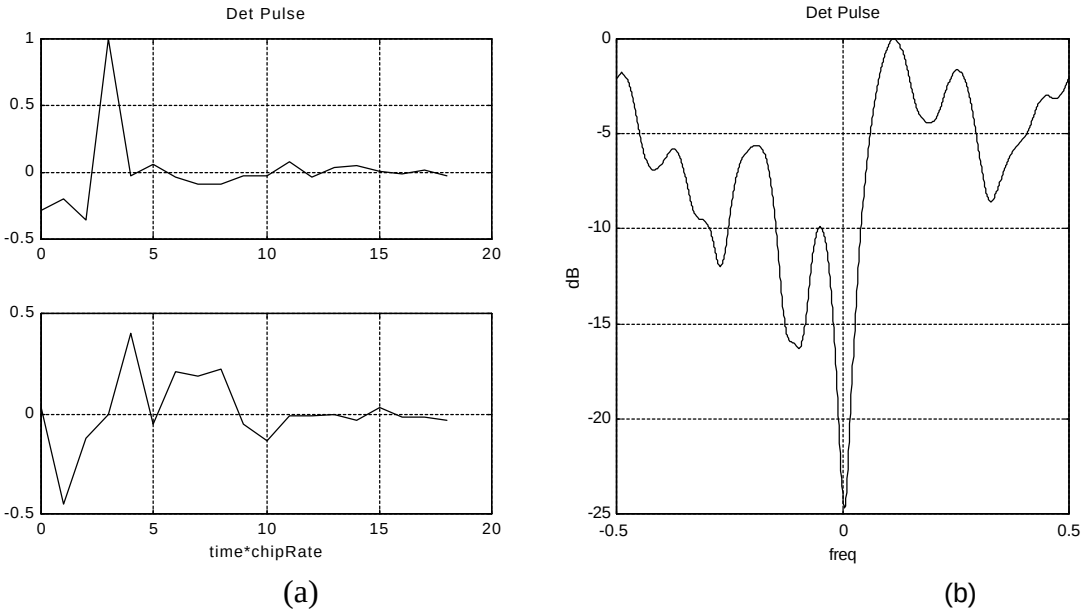


Figure 3.2.3-2 Modem/channel cascade example. A stochastic realization for the 200 nsec RMS delay spread case is shown. (a) Impulse response. (b) Frequency response in Nyquist bandwidth.

Conclusions can now be drawn as shown in Fig. 3.2.4-1.

First, the end-to-end energy spans about 6X the RMS delay spread. The receiver complexity is driven by this effect.

Second, typically the channel is has a small amount of precursor energy leading the impulse response peak and a lot of post-cursor energy following the peak.

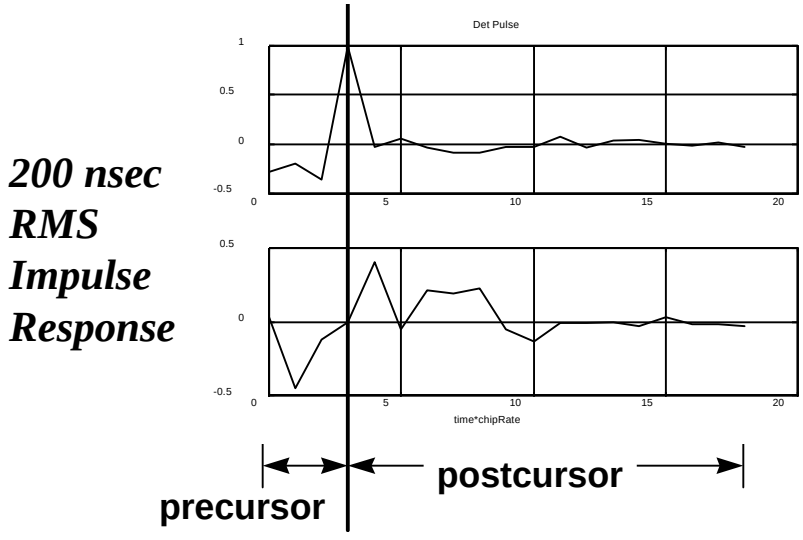


Figure 3.2.4-1 Post cursor component is the dominate channel characteristic.

3.3 THERMAL NOISE FLOOR

Thermal noise is another important issue. Thermal noise is predominately generated in the receiver front-end and is measured by the noise figure. Propagation loss defines where the signal lies relative to the noise floor. Some environments are $1/r^3$ while others are $1/r^4$, where r is the TX/RX separation.

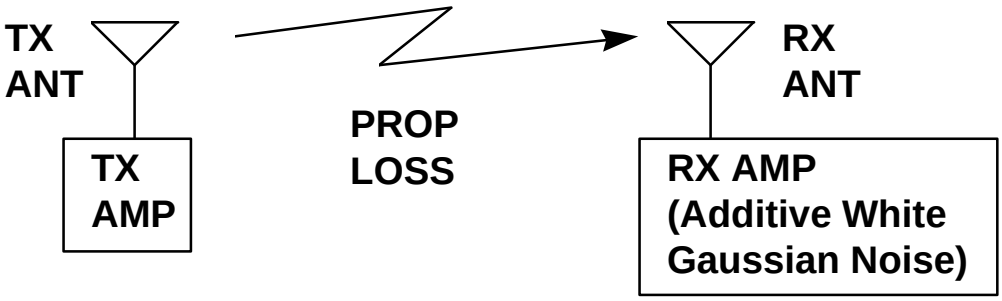


Figure 3.3-1 Signal power in the receiver is influenced by the link.

For linear processing, AGC set-up is an important issue as shown in Fig. 3.3-2.

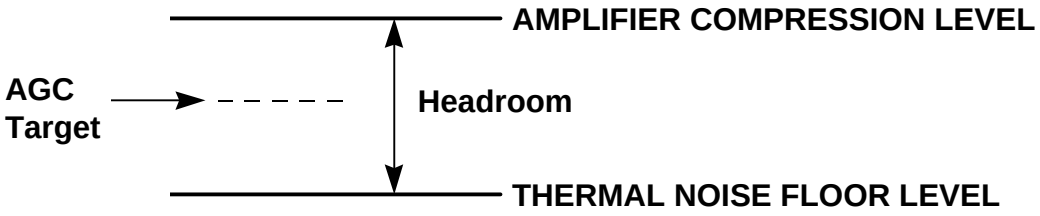


Figure 3.3-2 Ideal AGC set-up position.

An important issue is evaluating to what degree noise is important versus multipath effects. Some designs may be more noise robust but less multipath robust. Other designs may be more multipath robust but less noise robust. What importance weighting is needed for performance in real-world situations?

3.4 SIGNAL DESIGN CONCEPTS

This section will detail the signal design concepts which must be understood to select a waveform for high data rate WLAN transmissions. The following will show that a crystal-clear picture does not exists for selecting a waveform. However, broad conclusions can be drawn. Engineering intuition will need to be used to make the ultimate selection, possibility based upon cost and extensibility issues. HARRIS feels that narrowband-equalized signaling has not been previously analyzed sufficiently to uncovered strong merits in its favor. This section will reveal some of those merits.

3.4.1 BANDWIDTH-LIMITED VERSUS POWER-LIMITED

This section describes two extreme approaches for maximizing multi-user capacity in the bands of interest. It will be reasoned why HARRIS leans toward approaches which conserve single-user bandwidth.

The two traditional communication paradigms have been the bandwidth-limited and the power-limited scenarios. This is illustrated in Fig. 3.4.1-1. Using the capacity equations for signaling in additive white Gaussian Noise (AWGN), general conclusions can be drawn. Unfortunately, the present situation is complicated by other factors. Multipath is a major performance-limiting impairment along with the AWGN. Also, it is desirable to have a high multi-user capacity within the bands of interest (2.4 GHz and 5 GHz), since these are shared spectral resources. These additional factors lead to an erosion of the normal rules of thumb.

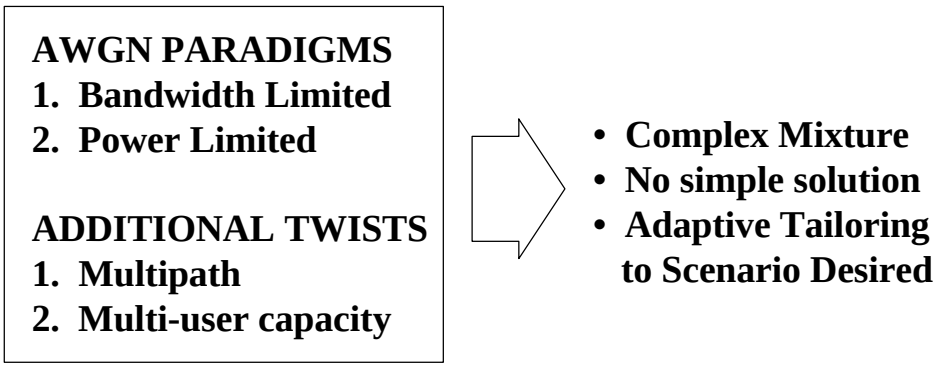


Figure 3.4.1-1 The dominate high-rate 802.11 signaling viewpoints.

Nevertheless, the democratic majority seeks to push higher data rates through the medium. A single-user does not care how the data rate is increased, just as long as his performance is good. For a single, isolated TX/RX modem pair, high data rates with good symbol error rate performance can be obtained by either conserving power or conserving bandwidth. This is depicted in Fig. 3.4.1-2. The signals (QPSK, 8 PSK, 16 QAM) which maintain bandwidth must be provided increasing Eb/No to successfully communicate. The signals which conserve TX power by operating at low Eb/No's must necessarily consume bandwidth. The waveforms proposed to the 802.11 committee fall within these regions. RAKE based techniques tend to fall in the bandwidth consuming camp, while the equalizer-based techniques tend to fall within the power consuming camp. By looking at the BITS/HZ axis, it is obvious the equalizer based communications conserve bandwidth at the single user level.

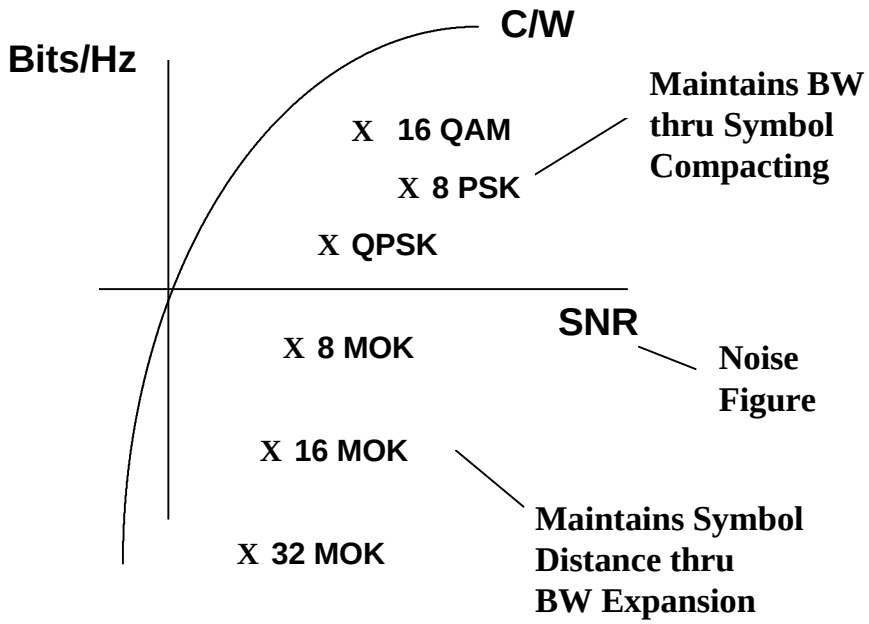


Figure 3.4.1-2 Digital modulations capacity comparisons at 10^5 symbol error rate.

A system designer must look at all the issues, since he is interested in the joint performance of all users. Most communications today occur in scarce spectral resources allocated by governments, such as the FCC in the U.S. Multiple users must be able to operate well concurrently. Consequently, the system designer is interested in the joint capacity of the spectral band. Here, the BITS/HZ metric includes all users.

To optimize band capacity, there are two lines of attack. One, conserve bandwidth at the single user level, so many single users can be packed concurrently within a band in a non-interfering fashion. Two, consume bandwidth letting users interfere frequently, and use processing gain to reject interference, improving the detection signal-to-interference (SIR) ratio. For second interfering system to work well, adaptive power control has been shown to be crucial. These two viewpoints are being played-out in the cellular/PCS worlds as shown in Fig. 3.4.1-3.

Standard	Bandwidth	Processing
TDMA **IS-54/IS-136** **GSM**	**Narrowband** **(SNR > 10 dB)**	**DFE or Viterbi Equalizer**
CDMA **IS-95**	**Wideband** **(SIR low)**	**RAKE**

Figure 3.4.1-3 Cellular/PCS signaling paradigms.

HARRIS has a preference for the narrowband band-capacity-optimization approach, primarily because it is more difficult to maximize band-capacity by coordinating users in the wideband approach. With the wideband approach, the users spread whether or not it is needed. The CDMA spreading codes in the 802.11 band are too low to provide adequate processing gain. Adaptive power control needed to realize multiple access is difficult. The WLAN systems tend to be more uncoordinated than the Cellular/PCS systems for obvious reasons.

Note that the narrowband Cellular/PCS systems tend to use equalizers, while the wideband systems use the RAKE. In like fashion, HARRIS proposes using a equalizer to combat multipath distortion while conserving bandwidth.

3.4.2 CAPACITY LOSS THROUGH WAVEFORM-FEATURES OVERHEAD

This section demonstrates that certain proposed waveforms carry bandwidth consuming, data-rate limiting features which tend to limit capacity. HARRIS proposes a waveform freed from these constraints, maximizing single-user and multi-user capacity.

3.4.3 MINIMIZING ISI THROUGH SYMBOL STRETCHING

Many proposals before the committee describe waveforms which contain certain features beyond simple information bit loading. The first waveform feature described limits intersymbol interference. This is evident in the both OFDM and RAKE (correlation based processing). In both these systems, conventionally signaling symbols must be much longer in duration than the multipath spread. The motive for this is shown in Fig. 3.4.2.1-1.

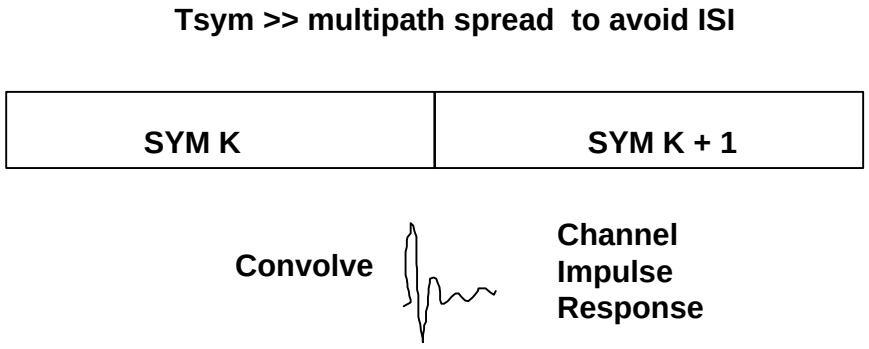


Figure 3.4.2.1-1 Minimizing ISI by increasing symbol duration so the convolution smear is a small percentage of the symbol.

The channel multipath spread smears adjacent symbols into one another. This intersymbol interference (ISI) can be significant, requiring equalization to mitigate the performance loss. OFDM systems use a slow IFFT/FFT signaling rate with waveform cyclic extensions (buffering) to minimize the effect. RAKE receivers traditionally have a many chips/symbol, with long duration symbols for the same reason.

Unfortunately, as shown in earlier sections, the multipath spread is very long compared to practical RAKE symbol durations. Hence, under non-trivial multipath spreads, the 802.11 proposed RAKE techniques suffer significant loss from ISI. This is true even if the RAKE symbols have fairly good correlation properties.

3.4.4 GOOD CORRELATION PROPERTIES

The second waveform feature frequently sought is good correlation properties. RAKE receivers have the best performance if the symbols are designed to have impulsive autocorrelation properties and near-zero cross-correlation properties. The motive involves symbol detection through RAKE combining. The RAKE combiner does not work well unless the RAKE-preceding correlation stage generates correlation outputs which equal the channel impulse response, independent of the specific transmission symbol. If this feature is not true, symbol distance erosion occurs.

The drawback to this approach is the design of symbols with good correlation properties consumes bandwidth as shown in Fig. 3.4.2.2-2. A much broader bandwidth is necessary. This is not a problem if the waveform already consumes a lot of bandwidth for either CDMA purposes or for diversity enhancement through bandwidth spreading beyond the coherent BW. This again is compatible with the power-limited design concept.

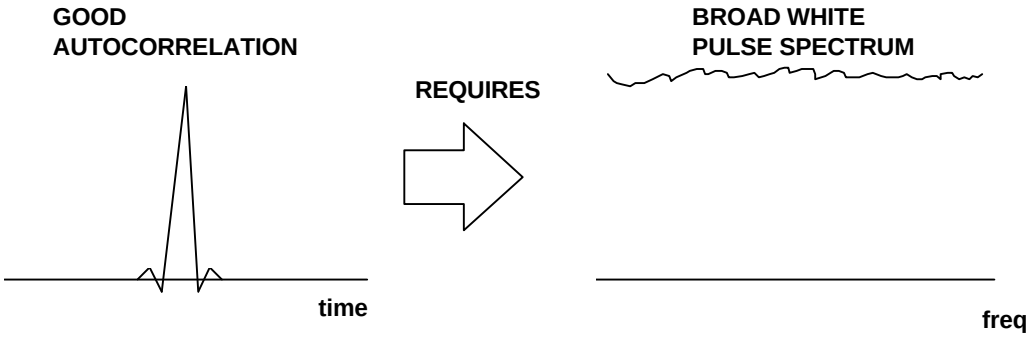


Figure 3.4.2.2-2 Good correlation properties consume bandwidth which limits the bits/Hz data-rate capacity.

Consuming bandwidth to purchase correlation properties means the bandwidth cannot be spent sending information bits. This limits the capacity of the single user, thereby limiting multi-user capacity within a band.

3.4.5 EXTENSIBILITY TO HIGHER RATES

After the development of the 1 and 2 Mbps standard, 802.11 has been faced with upgrading to higher data rates up to 10 Mbps. If history follows its usual pattern, once a 10 Mbps standard exists, motivation for a new standard will rise for 20 Mbps or 30 Mbps. Most of the proposals presented are fundamentally limited in data. However, HARRIS proposes a waveform which is extensible to 20 or 30 Mbps, similar to the way microwave links and voiceband modems have pushed higher data rates while maintaining a fixed bandwidth. This feature may provide greatly enhanced user acceptance and proliferation, since infrastructure does not need to radically change for the higher rates.

3.5 HARRIS'S PROPOSED TECHNIQUE FOR COMBATING MULTIPATH

This section provides an overview of the approach taken by HARRIS to mitigate the effects of multipath. The next section will describe architectural variations which trade complexity for performance. In short, HARRIS recommends the use of equalization. The complexity of the equalization is minimized by exploiting the predominately minimum-phase characteristic of the channel.

A summary of the motivations is shown in Fig. 3.5-1. The proposal avoids many of the problems highlighted above for other waveforms. As will be shown in the following sections, this opens the door for low-complexity, high-performance architectures.

- **If SNR is good enough, chip-level equalization is potent (TDMA standards, microwave links)**
- **Does not waste bandwidth trying to achieve good correlation properties**
- **Eliminates ISI, so symbol duration is freed from multipath-spread considerations**
- **Processing can be simpler**

Figure 3.5-1 Key advantages of HARRIS proposed technique.

The chief question which needs to be asked, "Is the chip level SNR sufficiently high to allow chip-level processing, or is the processing gain of the many-chip symbol needed to realize adequate performance?" To answer this question examine Fig. 3.5-2. This figure shows the symbol-error-rate (SER) performance of QMBOK with 8-chip symbols versus the QPSK chip error rate. Note that there is less than 2 dB SNR performance difference at 10^{-5}. This results from attempting to pack a high number of information bits on a few chips. This data packing results from trying to push a lot of data bits through a limited bandwidth. As shown earlier in the power-limited and bandwidth-limited capacity curves, achieving high bits/Hz forces higher Eb/No's to be used.

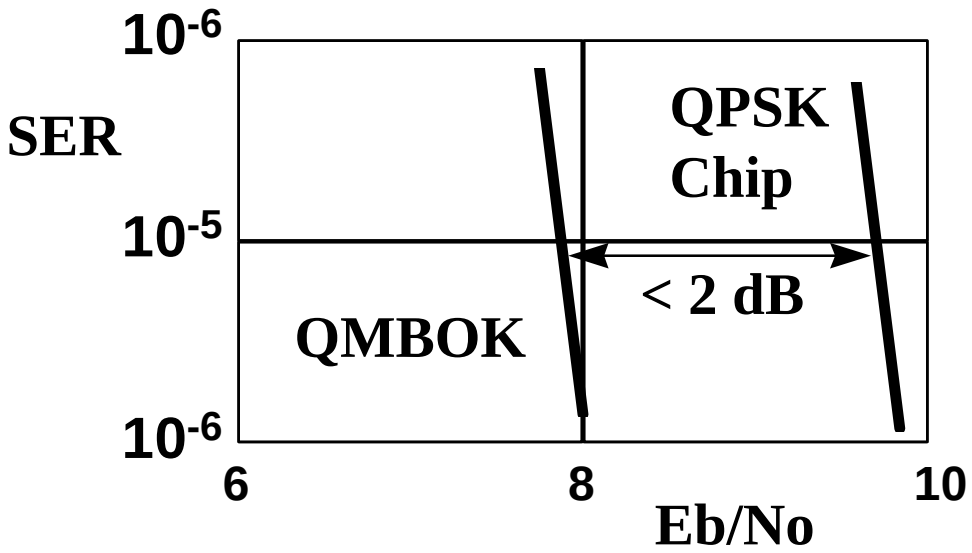


Figure 3.5-2 A comparison of symbol error rate for symbol level versus chip level processing.

Similar analysis could be shown for the PPM waveform. Here, many bits are packed on the 11-bit Barker word through position. So much distance is lost, that performance would be nearly as good if the QSPK chips were converted to QPSK symbols and the information bits sent directly on the QPSK.

Equalization does not mean that M-ary orthogonal waveforms cannot be used. M-ary orthogonal waveforms can still be used to provide orthogonal processing gain in thermal noise. Alternatively, PPM waveforms could be used with chip level equalization also. Eliminating chip level ISI means the receive processing architecture becomes much easier.

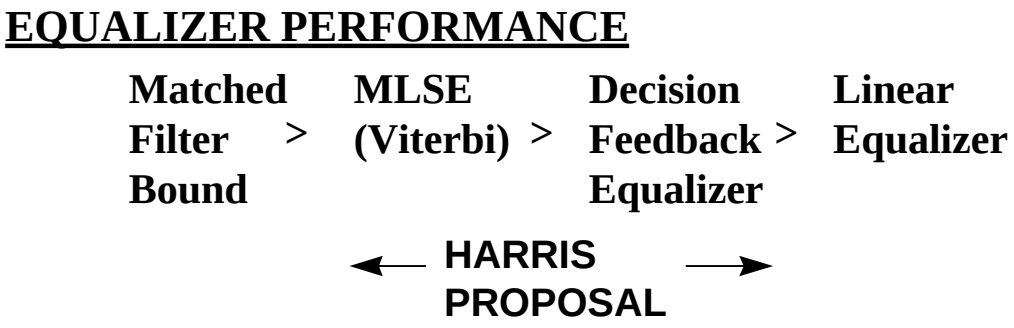


Figure 3.5-3 Equalizer performance comparisons.

Since a variety of equalizer techniques exist, one must consider which one to use. Fig. 3.5-3 shows the performance ranking of the most common techniques. The matched filter bound is not an equalization technique, but rather a benchmark against which all can be compared. HARRIS proposes using a combination of the MLSE and DFE equalizer to satisfy the needs of the receiver.

The gut level reaction is that an equalizer should not be used because it is too hard to train. HARRIS'S description will show how training is not a significant hurdle for 802.11. DFE and MLSE training is not a big hurdle for Cellular/PCS TDMA systems in the same way.

3.5.1 HARRIS'S KEY FEATURES

HARRIS believes their proposal presents the simplest proposed tracking architecture for high bits/Hz efficiency. The reason for this simplicity is HARRIS exploits a channel characteristic most proposals ignore. The channel is predominately minimum phase. The minimum phase distortion can be eliminated with only adds and subtracts using the feedback taps in a decision feedback equalizer.

HARRIS'S proposal provides high-resolution architecture scalability. The design implementation can be highly tailored to meet performance or power-draw needs. The designer is not forced to use one specific architecture for all scenarios. A suite of designs could be potentially made, optimizing particular features, all with the same waveform. The lowest complexity is provided in benign environments. Medium complexity is provided in moderate multipath environments. The highest complexity is reserved for the severe multipath environments.

HARRIS'S proposed waveform is unfettered by RAKE waveform constraints.

HARRIS'S waveform's distance properties are equivalent to other's who are pushing the same bits/Hz spectral efficiency.

The signal is applicable to both 2.4 GHz and 5 GHz.

Short preambles can be accommodated, since equalizer acquisition only requires an estimate of the channel impulse response.

Easy extensions provide data rates up to 20 or 30 Mbps.

3.5.2 HARRIS ARCHITECTURES

This section presents three canonical architectures. All these architectures work with the same transmit modulation. For 11 Mbps the modulation is QMBOK. QMBOK consists of quadrature M-ary biorthogonal keying. Eight bits are assigned to a symbol. Four bits select a sign on 1-of-8 Walsh symbols for each the I channel and the Q channel. The Walsh symbol can be viewed as having 8 chips. The quadrature signaling forms a QPSK chip. The following discussion will center on the 11 Mbps QMBOK waveform with QPSK chips. Fallback to 5.5 Mbps will accomplished using standard MBOK on the I-channel only, so the Walsh chip is BPSK.

The HARRIS chip rate is 11 MHz.

3.5.3 NO EQUALIZATION

The simplest architecture targets the low-cost, benign multipath environment. This architecture works for 30 nsec delay spreads or less. No equalization is used. A low-cost, nonlinear, limiting IF can be used.

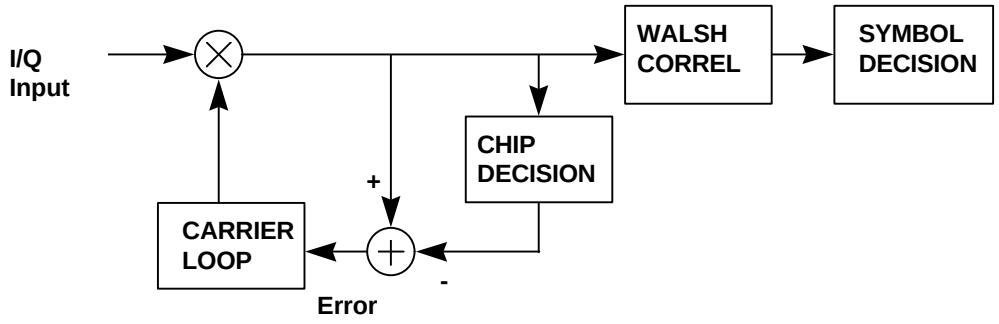


Figure 3.7.1-1 Architecture for the no-equalizer canonical form.

A plot of simulated multipath performance is shown in Fig. 3.7.1-2.

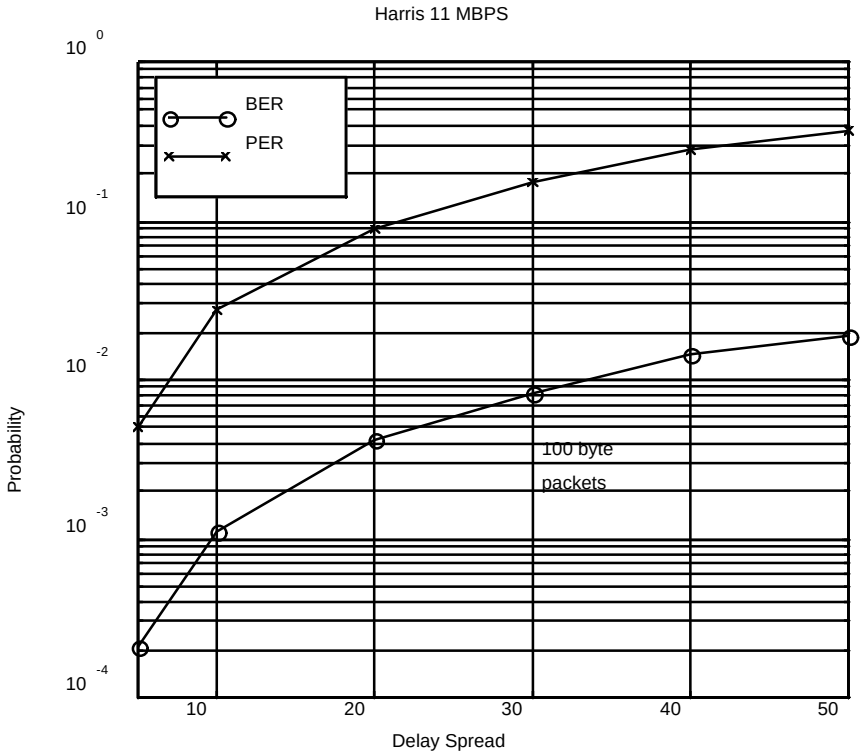


Figure 3.7.1-2 Multipath performance for the architecture shown in Fig. 3.7.1-1.

3.5.4 DECISION FEEDBACK EQUALIZATION

This section describes HARRIS'S form employing a decision feedback equalizer. As shown later, this architecture can be further subdivided into 3 types, with increasing performance-complexity characteristics. Here the 10% packet-error-rate (PER) multipath performance can theoretically exceed 100 nsec RMS delay spreads. Instantaneous equalizer training is achieved using only an estimate of the channel impulse response. It is assumed the impulse response estimate exists with 2 samples/chip, so a preferred decimation phase can be selected. This minimizes noise amplification by feed-forward taps in the DFE.

3.5.5 DFE STRUCTURE

A decision feedback equalizer is shown in Fig. 3.7.2.1-1. In multipath environments, the DFE and Viterbi equalizer are commonly used, since they usually output perform a linear equalizer. The DFE performance is provided by the absence of noise amplification in the feedback stage.

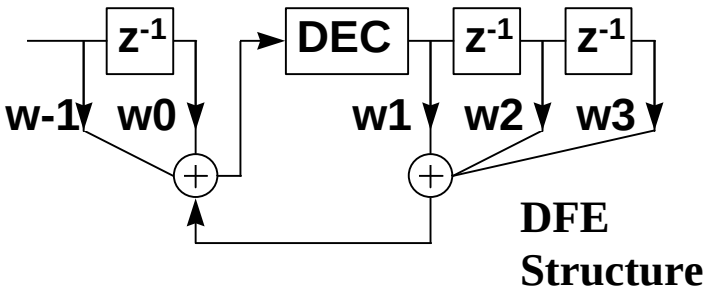


Figure 3.7.2.1-1 The structure of a decision feedback equalizer. The front end is the feed-forward section, and the back-end is the feedback section.

Theoretically, the DFE processes two types of channel information differently. The minimum phase channel components are processed by the feedback (FB) stage. The maximum phase channel components are processed by the feed-forward (FF) section . A typical impulse response for 100 nsec delay spread is shown in Fig. 3.7.2.1-2. The peak of the impulse response usually defines a partition between the minimum-phase and maximum-phase channel components. The energy in front of the peak (precursor) is maximum phase, while the energy following the peak (postcursor) is minimum phase.

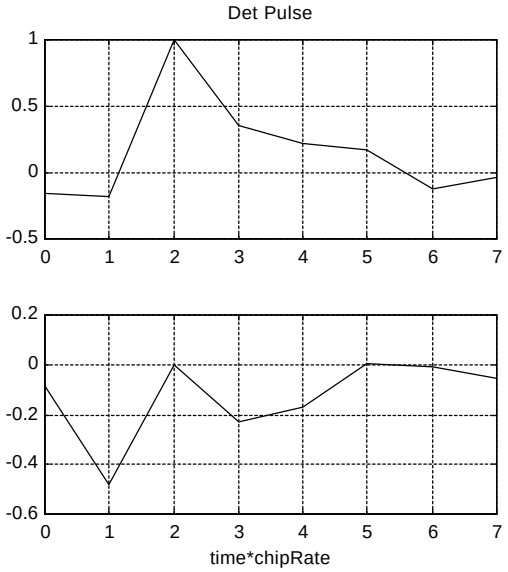


Figure 3.7.2.1-2 Typical end-to-end impulse response at 100 nsec RMS delay.

For an FIR channel, the minimum-phase zeros fall inside the unit circle in the Z-plane. The maximum-phase zeros fall outside the unit circle. This is demonstrated for the zeros-plot shown in Fig. 3.7.2.1-3 for the channel shown in Fig. 3.7.2.1-2. Note the two zeros outside the unit circle correspond to the two precursor taps shown in Fig. 3.7.2.1-2. A zero falling directly on the unit circle is handled by the feedback taps.

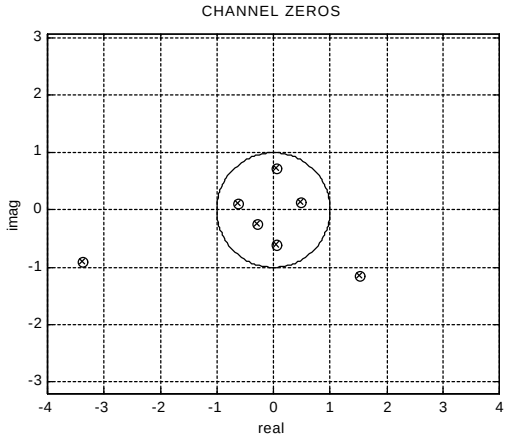


Figure 3.7.2.1-3 Channel zeros for the impulse response shown in Fig. 3.7.2-2.

3.5.6 INSTANTANEOUS DFE ACQUISITION

Decision feedback equalizers are usually trained using either a zero-forcing metric (ZF) or a minimum-mean-squared-error metric (MMSE). Most textbooks describe the use of a training sequence with either a slow recursive algorithm (LMS) or a fast recursive algorithm (RLS). Alternatively, for the wireless world techniques have been developed for instant training using a estimate of the channel impulse response. A preamble (IS-54) or a midamble (GSM) is used with impulsive autocorrelation properties for performing the channel estimation. The channel impulse response can be used to calculate the DFE taps.

Most commonly the 802.11 multipath appears as shown in the two examples of Fig. 3.7.2.2-1. In the first example, no precursor (maximum-phase) components are present. Here the ideal equalizer weights contain only feedback (FB) taps and no feedforward (FF) taps. The FB taps are set equal to the channel impulse response (1 sample/chip).

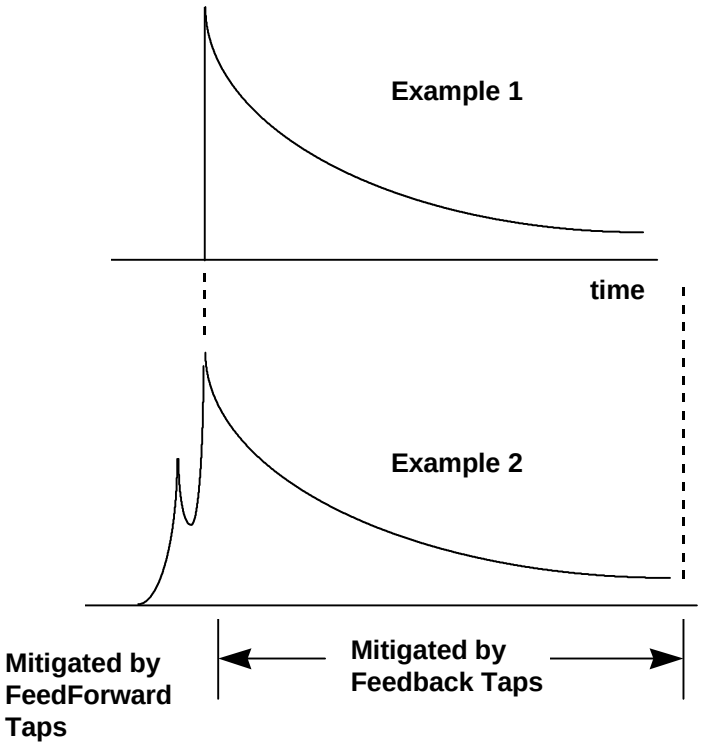


Figure 3.7.2.2-1 Channel diagram emphasizing typical characteristics.

Example 2 of Fig. 3.7.2.2 requires FF weight calculation before the FB weights can be computed. Using the zero-forcing (ZF) criterion, two FF weights can be solved using the matrix shown in Fig. 3.7.2.2-2. Once the channel impulse response is known, the coefficient matrix is known. Simple inversion gives the result. For two FF weights the w_{-1} and w_0 solution is simply h_{-1} and h_0 scaled by the same complex constant. Solving for 3 FF taps is similar.

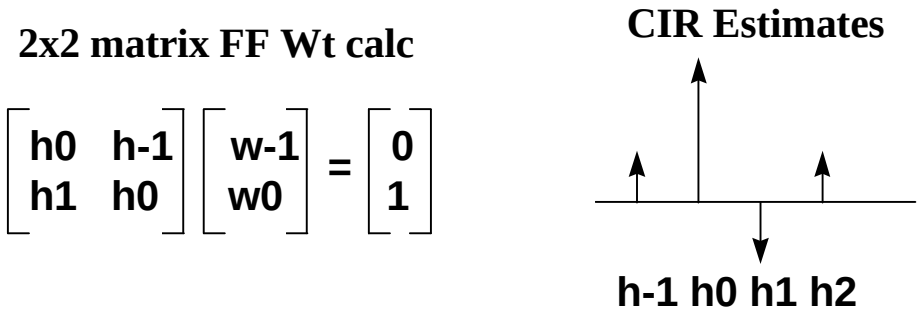


Figure 3.7.2.2-2 Two tap feed-forward DFE ZF weight calculation.

Once the FF weights have been calculated, the FB taps are derived by convolving the channel impulse response with the FF weights. The trailing taps in the output convolution become the FB taps.

To vary complexity, the developer simply decides how many taps are needed to obtain a certain level of performance. These options are illustrated by using only FB taps, using only 2 FF taps, and using 3 FF taps. The number of FB taps is varied in each case.

3.5.7 DFE WITH FB TAPS ONLY

This section examines the architecture and performance for a DFE which uses only FB taps. For a QPSK signaling element, the FB FIR output computation is very simple because no multiplications are required, only additions and subtractions. The QPSK element decision is ±1±j.

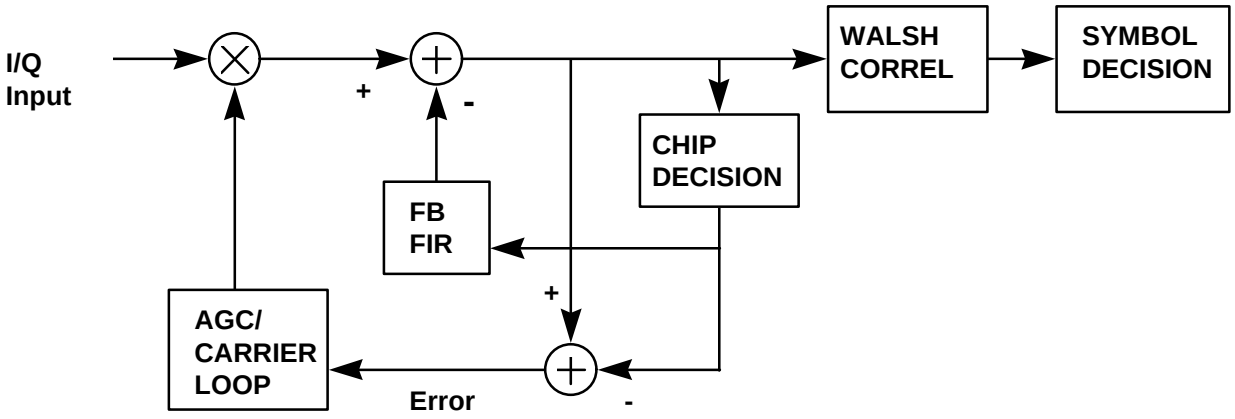


Figure 3.7.2.3-1 FB taps only demodulation architecture.

The associated multipath performance has been conservatively estimated by HARRIS. A packet error is assumed whenever a stochastic channel realization has a closed-eye at the QPSK chip level. This is conservative (worst-case bound) because the correlation gain of the fast Walsh transform is ignored. Note, differentiation between 64 byte and 1000 byte packets is not made. This is conservative because the data pattern needed to realize an eye closure may be a small probability event.

The performance in multipath is shown in Fig. 3.7.2.3-2. The number of FB taps is varied from 0, 1, 2, 4, 6, 8 and 10.

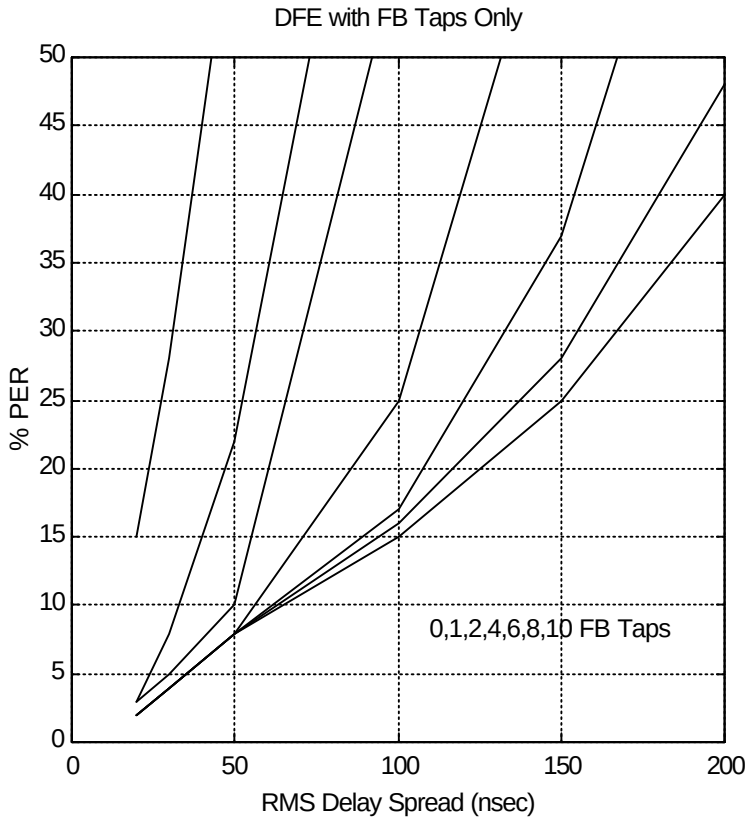


Figure 3.7.2.3-2 Packet error rate performance in multipath for various FB tap quantities. This data was calculated using a worst-case bound—chip eye closure.

Only 6 FB taps provides <10 % packet errors out to 60 nsec and <20% packet errors out to 110 nsec of RMS multipath. The is very good performance given the simplicity. For this case, only 6 complex adds (or subtracts) are required per chip. This architecture may be good enough for many target environments.

3.5.8 DFE WITH TWO FF TAPS

Since the FB-taps-only case makes no attempt to combat precursor multipath components, this section adds a little more complexity by using two FF taps.

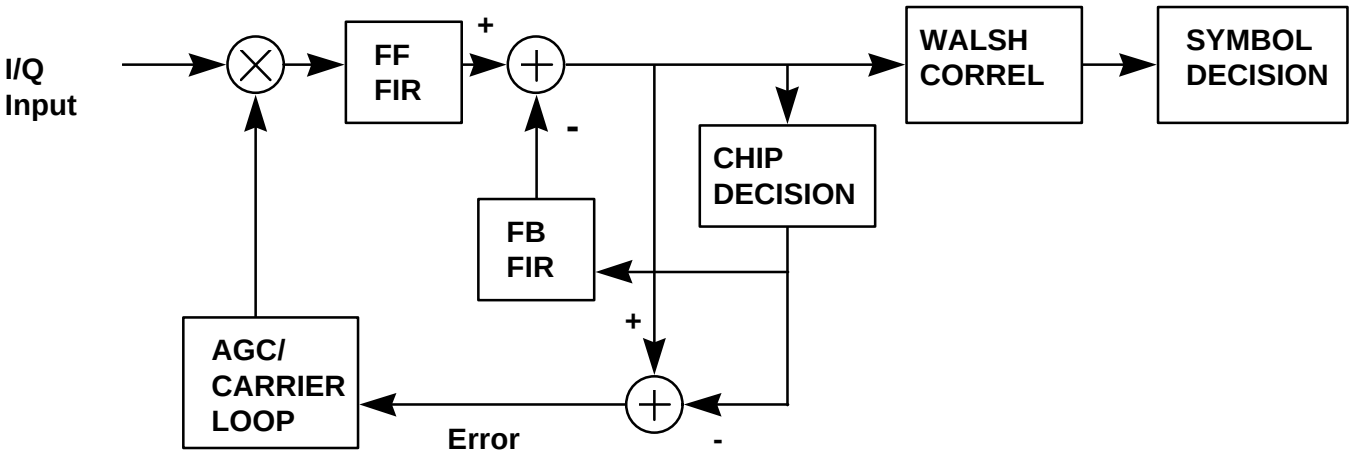


Figure 3.7.2.4-1 Architecture including feedforward DFE taps.

The associated multipath performance has been conservatively estimated by HARRIS. A packet error is assumed whenever a stochastic channel realization has a closed-eye at the QPSK chip level. This is conservative (worst-case bound) because the correlation gain of the fast Walsh transform is ignored. Note, differentiation between 64 byte and 1000 byte packets is not made. This is conservative because the data pattern needed to realize an eye closure may be a small probability event.

The performance in multipath is shown in Fig. 3.7.2.4-2. The number of FB taps is varied from 1, 2, 4, 6, 8 and 10.

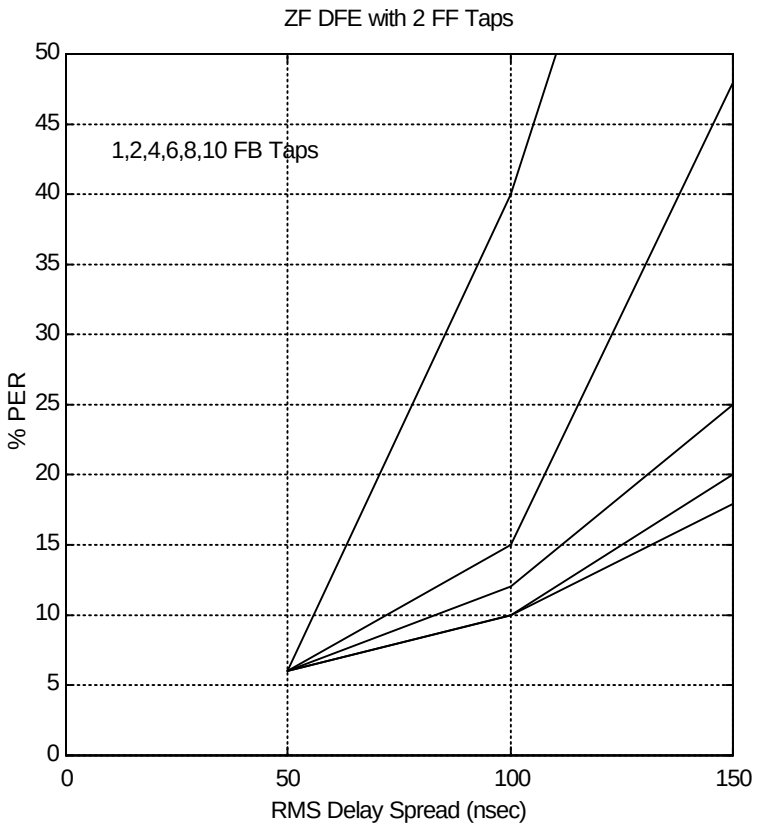


Figure 3.7.2.4-2 Packet error rate performance in multipath for 2 FF taps and various FB taps quantities. This data was calculated using a worst-case bound—chip eye closure.

Here only 2 FF taps and 6 FB taps provides <10 % packet errors out to 80 nsec and <20% packet errors out to 120 nsec of RMS multipath. The is very good performance given the simplicity. An extra multiply is required per chip.

3.5.9 DFE WITH THREE FF TAPS

This section examines the performance using 3 FF taps. The architecture remains that shown in Fig. 3.7.2.4-1.

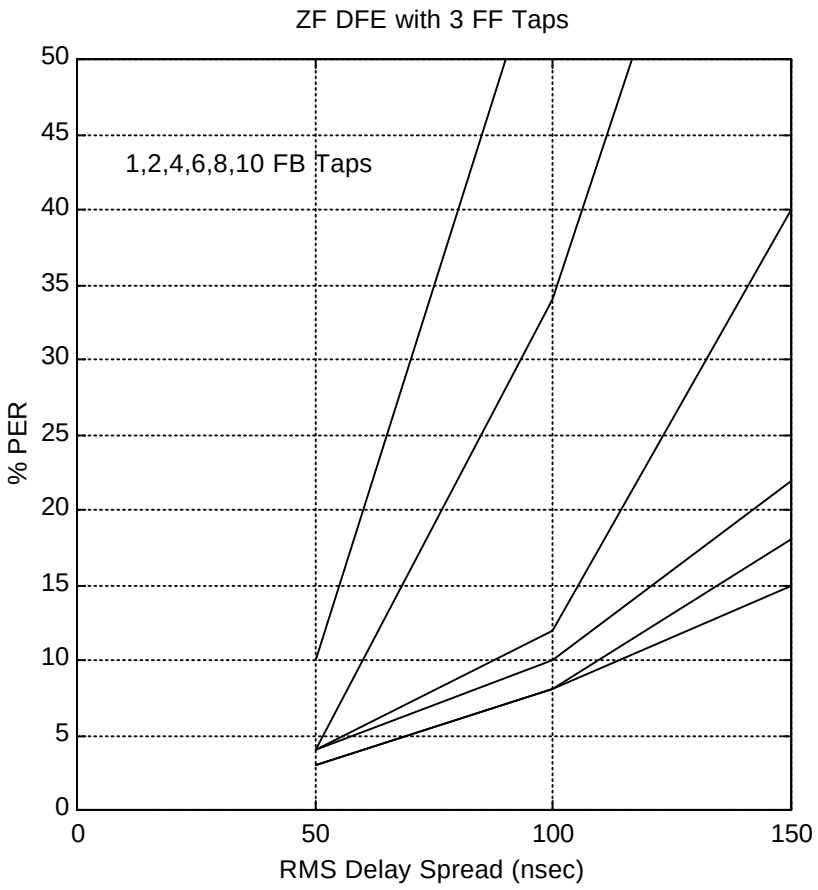


Figure 3.7.2.5-1 Packet error rate performance in multipath for 3 FF taps and various FB taps quantities. This data was calculated using a worst-case bound—chip eye closure.

Here only 3 FF taps and 6 FB taps provides <10 % packet errors out to 100 nsec and <20% packet errors out to 140 nsec of RMS multipath. The is very good performance given the simplicity. Two extra multiplies is required per chip.

3.5.10 VITERBI-DFE EQUALIZATION

This section describes HARRIS'S canonical form employing a Viterbi/decision-feedback equalizer. As shown later, this architecture can be varied with increasing performance-complexity characteristics.

The key motive for using the Viterbi-DFE is to strongly combat the precursor distortion in the multipath channel. The feed-forward taps in a DFE are limited in their capability.

Here the 10% packet-error-rate (PER) multipath performance can theoretically reach 200 nsec RMS delay spreads. Instantaneous equalizer training is achieved using only an estimate of the channel impulse response.

3.5.11 VITERBI-DFE OVERVIEW

In an additive-white-Gaussian-noise, intersymbol-interference environment, the optimum receiver is the maximum likelihood receiver. This receiver can be implemented using the complexity limiting Viterbi algorithm for performing maximum likelihood sequence estimation (MLSE). The Viterbi MLSE receiver is employed in GSM cellular phones. Unfortunately, applying MLSE is too complex for the 802.11 high data rate receiver.

However, the complexity of the Viterbi-based MLSE receiver can be greatly reduced, while maintaining good performance by employing decision feedback techniques. The idea is to use MSLE estimation on the precursor portion of the channel and feedback equalization on the post-cursor portion of the channel.

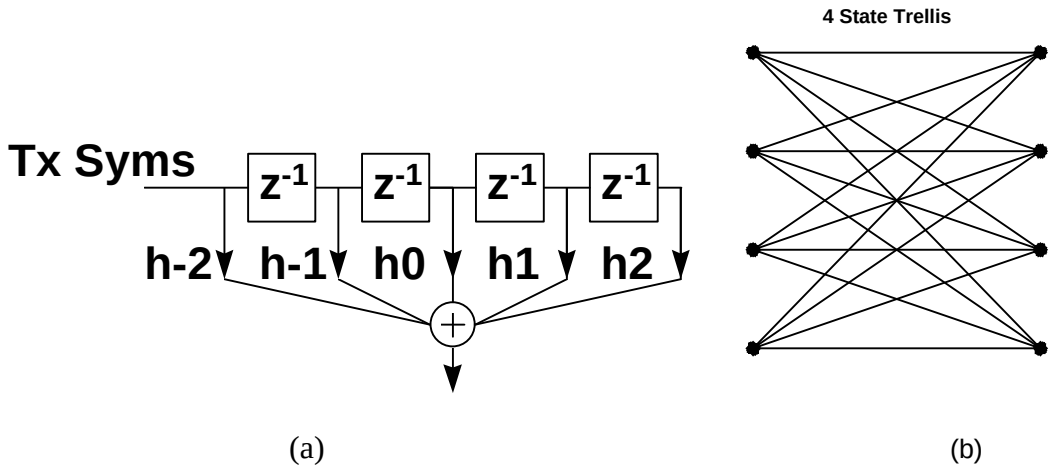


Figure 3.7.3.1-1 Finite state machine channel viewpoint. (a) The channel impulse response forms FSM. (b) A representative trellis.

The channel forms a finite state machine (FSM) as shown in Fig. 3.7.3.1-1. The symbols in the delay elements form the state. The input of a new symbol causes a state transition. The state transitions can be represented by a trellis. The received signal therefore contains memory. An optimal detector can compare the distance between the received signal and the known possible transmit transitions. The minimum distance sequence is the optimum received signal estimate.

The number of states in the trellis is equal to M^{L-1}, for an M-ary modulation with a L-tap channel. For QSPK chips, M is 4. For a 100 nsec RMS delay spread channel, L can range to 8. This establishes 16K states. This degree of complexity cannot be handled. For QPSK elements, 4 branches enter and exit each state in the trellis.

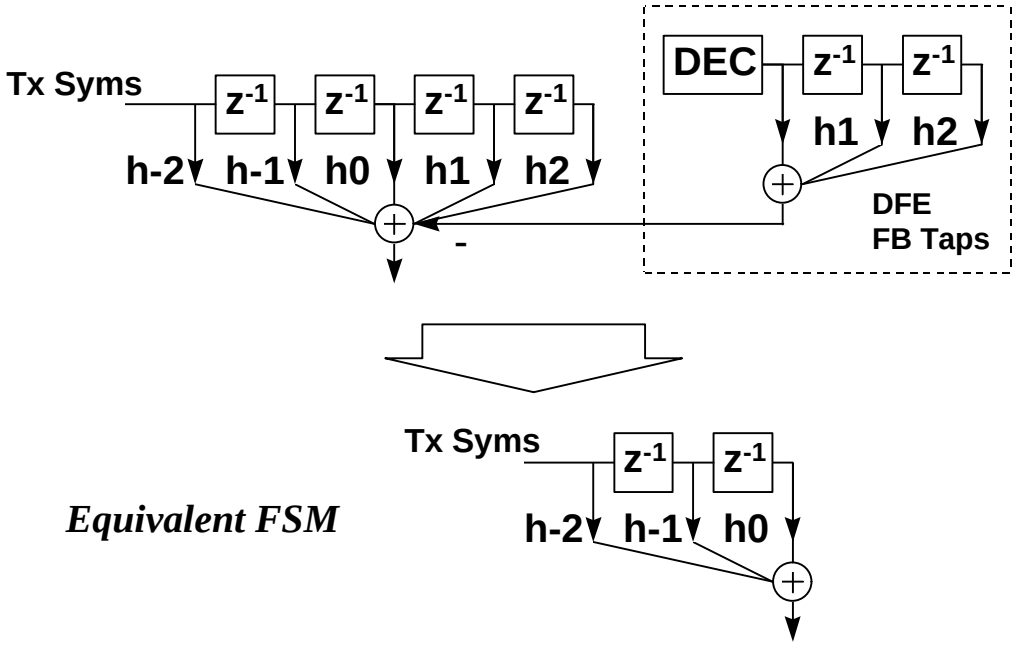


Figure 3.7.3.1-2 Reducing the complexity of the finite-state-machine through decision feedback.

Figure 7.3.1-2 demonstrates how decision feedback can reduce complexity to an acceptable level. If the channel FSM were cascaded with a decision feedback stage, the overall complexity would be reduced to only the complexity of the precursor taps. This is the trick employed in the receiver.

Where do the decisions come from in the receiver for the feedback stage? From a partial traceback of the trellis as shown in Fig. 3.7.3.1-3. A full traceback is used to make the data decision, but the partial traceback fed to the FB taps is often a good estimate of the transmit symbol. Each step in a traceback is equivalent to stepping back one extra memory in the transmit symbol queue. The reliability of the estimate increases with each traceback step.

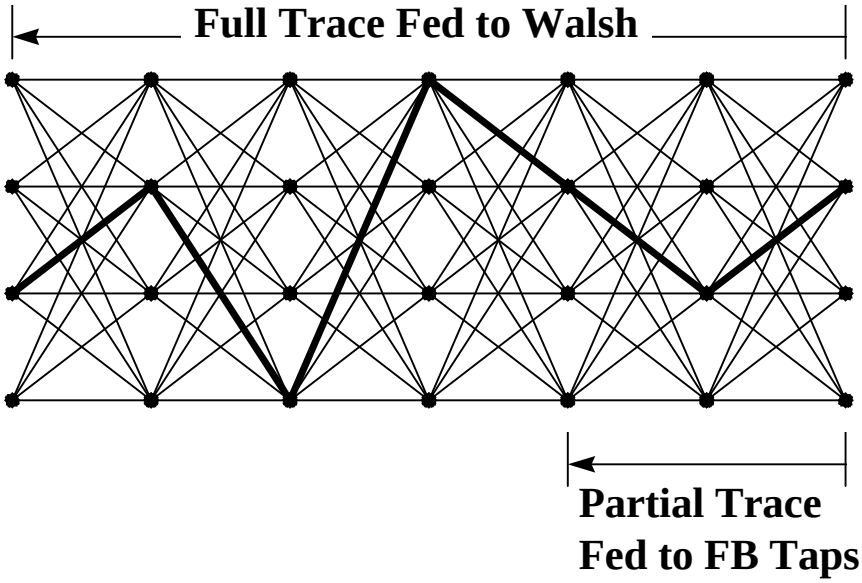


Figure 3.7.3.1-3 A partial traceback is used to feed the decision feedback stage.

The reliability increase is illustrated in Fig. 3.7.3.1-4. The drawback of the reliability increase is the number of states in the trellis increases by a factor of M-ary for each extra delay.

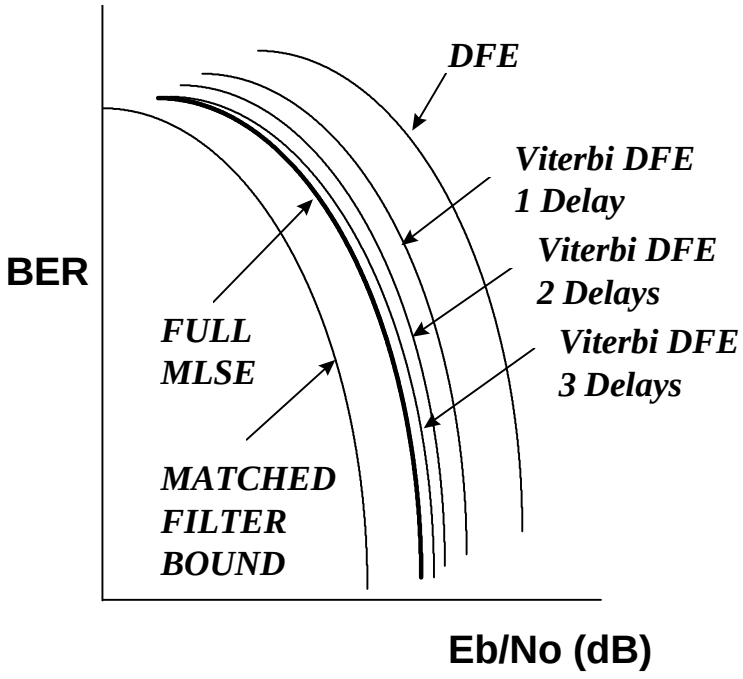


Figure 3.7.3.1-4 Viterbi DFE performance variation with increasing partial traceback delays.

The complexity in the Viterbi algorithm comes from computing the branch metrics, determining the branch survivors, identifying the best state, and performing the traceback. Memory can be traded against real-time operations.

3.5.12 FOUR-STATE VITERBI-DFE

The architecture for the Viterbi-DFE is shown in Fig. 3.7.3.2-1. The diagram shows the qualitative details.

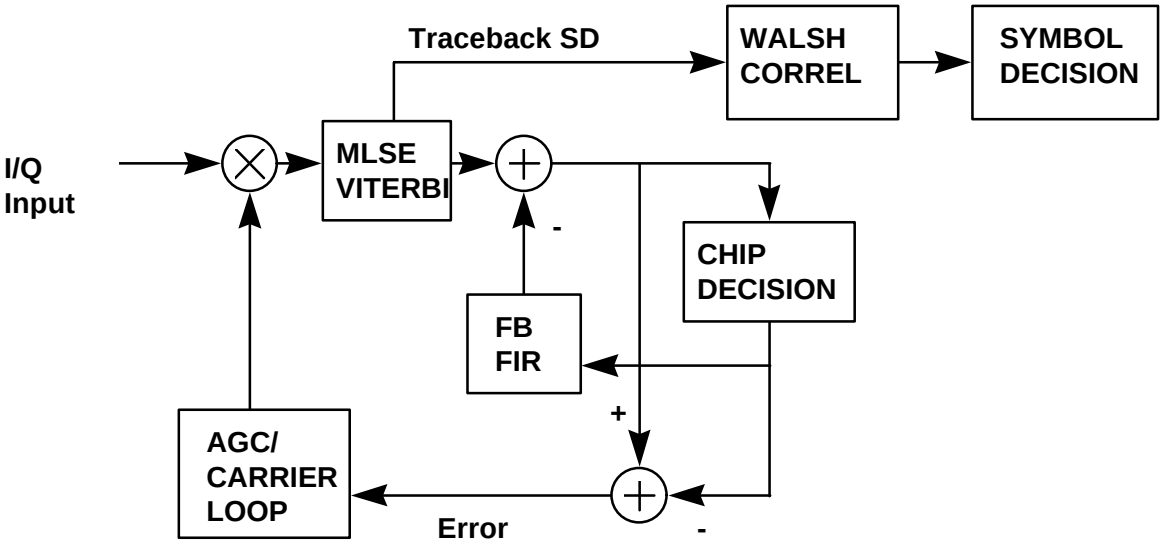


Figure 3.7.3.2-1 Architecture for the Viterbi-DFE.

The performance of a 4-state trellis Viterbi-DFE is shown in Fig. 3.7.3.2-2. This curves were generated using a conservative bounding technique similar to that used for the DFE. An eye closure metric was measured given the joint operation of the MLSE/DFE. Actually, the Viterbi would often resolve the instantaneous eye closure through the traceback.

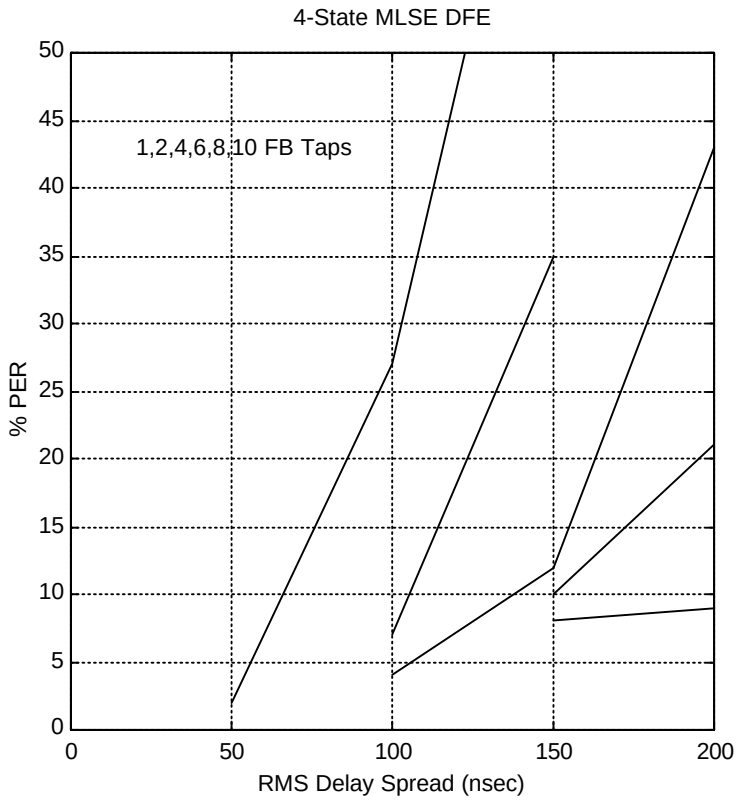


Figure 3.7.3.2-2 Multipath-spread performance curves for the 4 state Viterbi-DFE.

3.5.13 SIXTEEN-STATE VITERBI-DFE

The performance for a 16-state trellis Viterbi-DFE is shown in Fig. 3.7.3.3-1. These curves were generated using a conservative bounding technique similar to that used for the DFE. An eye closure metric was measured given the joint operation of the MLSE/DFE. Actually, the Viterbi would often resolve the instantaneous eye closure through the traceback.

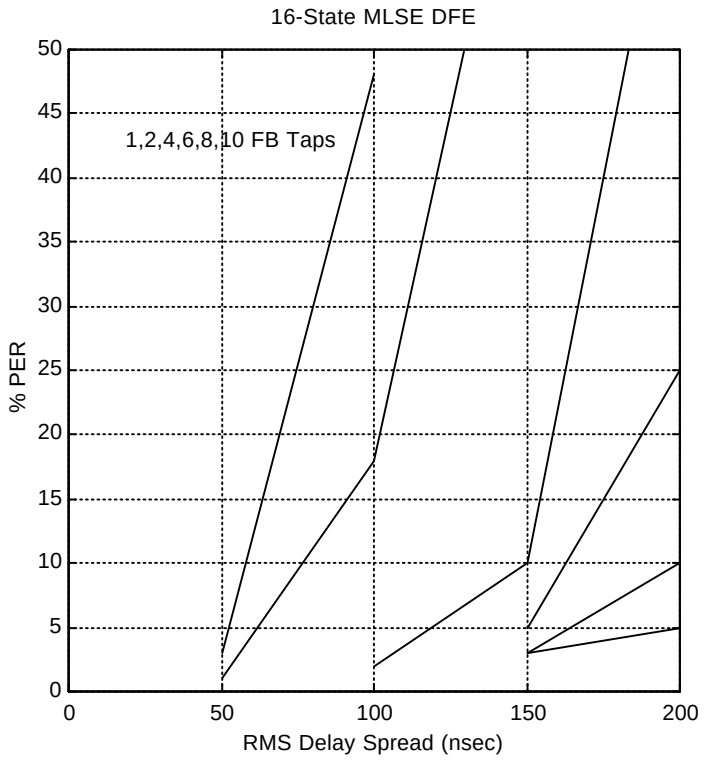


Figure 3.7.3.3-1 Multipath-spread performance curves for the 16 state Viterbi-DFE.

3.5.14 PERFORMANCE SUMMARY

Describing HARRIS'S performance in multipath is not an easy task, since such a wide range of options are possible—trading complexity for performance. An attempted performance summary is shown in Table 3.8-1. Multipath performance is presented in 25 nsec RMS increments, ranging from 25 nsec up to 200 nsec. The minimum architecture complexity needed to achieve a 10% packet error rate is shown.

In many instances one may be very satisfied with 20% packet errors in a very severe environment. If this is acceptable, the ZF DFE with no FF Taps and FB Taps only can be used up to 75 nsec. The ZF DFE with 2 feedforward taps can be used all the way up to 150 nsec RMS spread. Also, the 4 state Viterbi-DFE can reach as far 175 and 200 nsec RMS spreads. This greatly reduces cost and power draw by allowing the preferred packet error rate of 10% to softly degrade to 20% when conditions are severe.

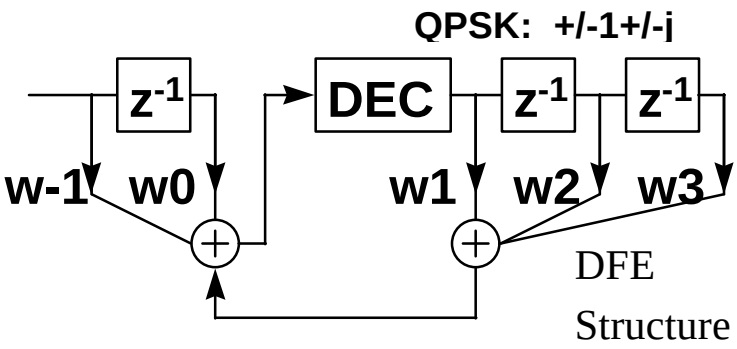
Table 3.8-1 Packet error rate performance.

RMS Multipath Spread	10% PER	20% PER
25	ZF DFE, 1 FB Tap	
50	ZF DFE, 2 FB Taps	
75	ZF DFE, 2 FF and 4 FB Taps	ZF DFE, 4 FB Taps
100	ZF DFE, 3 FF and 6 FB Taps or 4 state Viterbi-DFE, 4 FB Taps	ZF DFE, 2 FF and 4 FB Taps
125	4 state Viterbi-DFE, 6 FB Taps	ZF DFE, 2 FF and 6 FB Taps
150	4 state Viterbi-DFE, 8 FB Taps or 16 state Viterbi-DFE, 4 FB Taps	ZF DFE, 2 FF and 8 FB Taps
175	16 state Viterbi-DFE, 7 FB Taps	4 state Viterbi-DFE, 7 FB Taps
200	16 state Viterbi-DFE, 8 FB Taps	4 state Viterbi-DFE, 8 FB Taps

3.5.15 COMPLEXITY SUMMARY

The complexity of only the DFE will be described. Insufficient time was available for estimating the complexity of the Viterbi-DFE, although it is felt the 4 state architecture will be quite reasonable.

The DFE complexity is shown in Fig. 3.7-1. The FF taps require a complex multiply each. A complex multiply is 4 real multiplies and 2 real adds. The FB taps operate with only adds/subtracts because the decisions are QPSK.



nFF: # of complex FF Taps
nFB: # of complex FB Taps

# of real mults: 4 nFF/chip
# of real adds: (2 nFF + 6 nFB)/chip
# of compares: 2/chip

Figure 3.7-1 The basic DFE structure with math operations/chip.

For 2 FF taps and 6 FB taps, a gate estimate is 10K gates for the DFE tracking structure, 20K for the weights training calculation and 5K for the channel impulse response estimate. These are gate deltas over the 1 and 2 Mbps silicon. Probably 6 bit A/D's will be required. This will tend to dominate.

Table 3.7-1 Gate count complexity for 2 FF taps and 6 FB taps DFE.

Function	**Gate Count**
DFE tracking structure	10K
DFE weight calculation	20K
CIR estimation	5K
TOTAL	**35K**

3.5.16 PREAMBLE PROCESSING

Mitigation of multipath requires an estimate of the channel impulse response as shown in Fig. 3.8-1. HARRIS is on equal footing in this requirement with all the other proposals.

HARRIS can use a short preamble if the channel impulse response estimate is sufficiently accurate.

The 11 bit Barker may not be sufficiently accurate for large multipath spreads.

AGC settling is an important issue to examine.

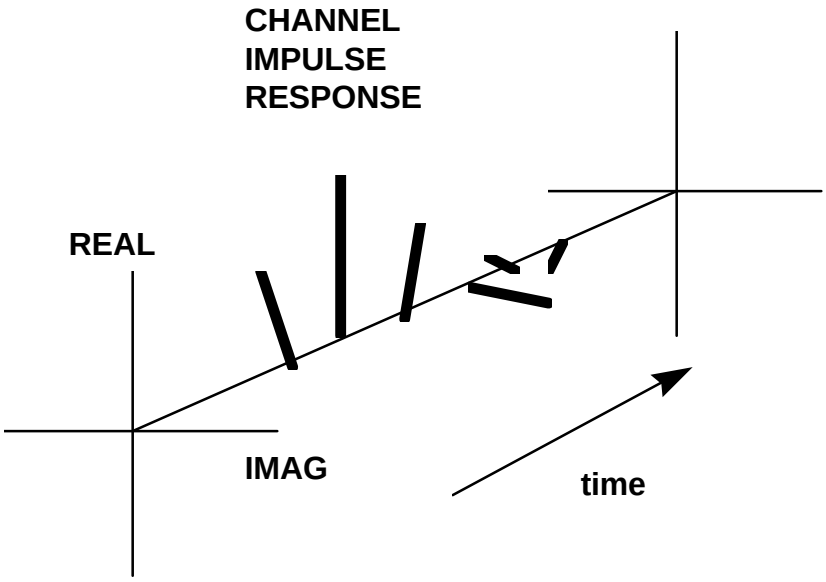


Figure 3.8-1 A channel impulse response showing amplitude and phase information.

3.5.17 FUTURE PERFORMANCE EXTENSIONS

This section demonstrates how the receiver architecture can basically remain unchanged, while supporting higher data rates. The 11 Mbps chip rate is 11 Mcps. By converting chips to symbols, eliminating the Walsh symbol structure, QPSK data can be sent directly as shown in Fig. 3.9-1. In this case, 22 Mbps can be exchanged, all without changing the clock rates. Also, 33 Mbps can be exchanged by using 8 PSK symbols. With 8 PSK the DFE FB taps would have to become multipliers instead of simple add/subtracts.

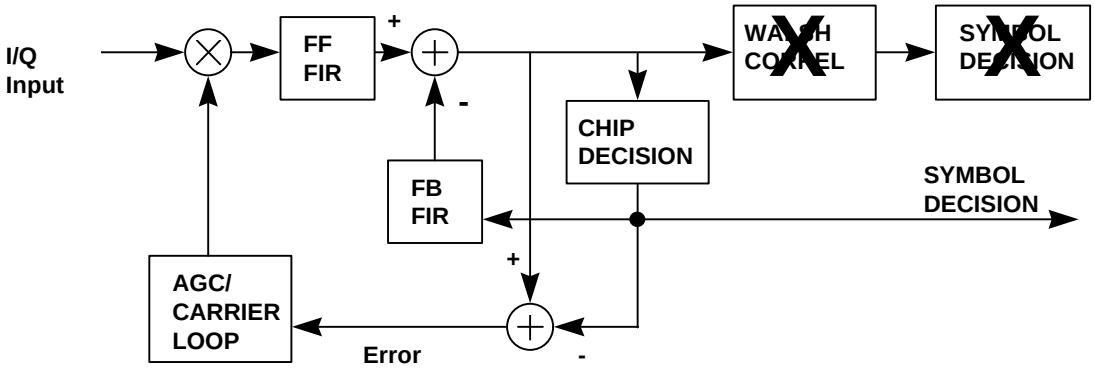


Figure 3.9-1 Modified architecture for handling higher data rates.

4. Introduction to Antenna Diversity

The advantages of antenna diversity are derived from the fact that two sufficiently physically separated antennas usually result in non completely correlated channels. The dimensions of a laptop (12") provides sufficient physical separation for significant antenna diversity performance gain, although for most near term applications only the access point and perhaps desktop PCs will have diversity to minimize cost. The coming integration of wireless network hardware into laptops will isolate the user from antenna wiring.

The actual performance gain achieved is highly dependent upon the details of the operational environment. In the limit, if the channels are uncorrelated, and the best antenna accurately chosen, the missed message rate can be raised to the power of the number of independent paths. For example a 50% missed message rate could, with dual receive diversity, theoretically be reduced to 25% and with dual transmit & receive diversity to 6.25%. Antenna diversity also reduces the probability of 'dead spots,' which are very annoying to users.

4.1 Antenna Diversity Concepts

Antenna diversity complexity and performance should track the performance of the rest of the modem. Providing various interoperable cost/performance options extends the breadth of feasible users (home, office, industrial & custom products) and reduces cost by increasing production qualities. Examples include a low cost non-diverse IF limited receiver to which antenna diversity, equalizer and additional processing could be added, depending upon the price sensitivity of the user. Following this concept both receive and simplified transmit antenna diversity schemes will be presented.

Starting at the low end, the current antenna diversity metric, which optimizes signal to noise ratio (1 & 2 Mbps specification) with an IF limited signal, can be easily modified to optimize multipath performance for useful IF limited delay spreads. Accurate performance of the metric at very large delay spreads, far beyond the useful range of a limited receiver is not necessary.

Optimizing performance at 1 and 11 Mbps requires different metrics since their susceptibility to multipath effects are vastly different. As the data rate is not known at the antenna diversity decision time, redoing antenna diversity between the header and the start of 11 Mbps data requires no 1 or 2 Mbps specification changes while providing a very robust accurate hardware efficient metric optimized for the specific data rate. This scheme uses the 8 Walsh basis vectors received on each antenna.

A high performance receiver which corrects for the multipath would necessarily want to minimize the processed symbol error rate. How this can be accomplished varies with the particular receive processing. Typical examples include RMS residual error from an equalizer and trace back information from a maximum likelihood algorithm.

A simple access point (AP) transmit antenna diversity scheme, which can be added to receive diversity, to provide significant improvement with no hardware impact, is also presented.

4.2 IF Limiter Diversity Assumptions

The IF limiting low end receiver requires good multipath diversity performance for 25 to 50 ns RMS delay spreads with minimal hardware. This low end receiver will lose significant throughput with larger delay spreads. However the diversity scheme must work with higher delay spreads to choose the low delay spread antenna, if one is available.

The diversity scheme must be fully compliant with current DS IEEE 802.11 specification, when it is used with the low rate preamble . Changes to existing systems are unacceptable.

The diversity must be done during the Barker preamble where it is currently accomplished. Since the data rate is unknown to the receiver at the diversity decision time the performance will

necessarily be a compromise. This can be accomplished as performance is acceptable at 100 ns RMS which is beyond the useful operating RMS delay spread.

The diversity scheme must operate with an IF limiter. The receive limiter reduces cost by deleting the AGC function.

The diversity scheme must operate with differentially detected non-coherent bit sync samples. This information already exists and has been non-coherently combined to reduce its variance.

The goal is to minimize complexity and additional gate count. This has been accomplished as only approximately 500 additional gates are required for the multipath diversity metric.

4.3 IF Limiter Diversity Bit Sync Metric

The metric is computed by subtracting the four bit sync samples one and two chips on either side of the bit sync peak from the peak. The antenna with the higher result becomes the selected antenna. Not subtracting the sample two chip early results in only a small performance loss. The performance gain resulting from non unity simple weights for the samples is being investigated.

4.4 Walsh Distance

The Walsh distance, a robust measure of how close demodulated symbols are to making an error, It is computed by:

1) finding the minimum correlation of the 8 Walsh basis vectors transmitted sequentially on the I channel.
2) finding the maximum of the absolute value of the cross-correlation of the 8 Walsh basis vectors on both channels not including the 8 I correlation peaks above
3) subtracting #2 from #1 above

Assuming the Walsh distance is an indication of message error rate, it can be used as a quick indication of antenna diversity accuracy.

4.5 IF Limiter Diversity Metric Performance

The correlation of this non-coherent bit sync metric with Walsh distance is shown for 10 (Fig. 1), 25 (Fig. 2), 50 (Fig. 3) & 100 (Fig. 4) ns RMS. Each figure consists of 1000 trials. For the delay spreads of interest and an IF limiting receiver this metric appears highly correlated with symbol error rate.

4.6 Walsh Basis Vector Diversity Assumptions

Higher performance receivers require an antenna diversity metric with improved performance at delay spreads greater than 100 ns. This metric should be designed for use by both higher performance IF limiting and linear receivers. It must be fully compliant with current IEEE 802.11 specification at 1 & 2 Mbps. It must operate with an IF limited receiver with excellent performance at all delay spreads

Optimizing performance at 1 and 11 Mbps requires different metrics. Since the data rate is not known at the antenna diversity decision time, redoing antenna diversity between the header and start of the 11 Mbps data is the most obvious solution. Again the goal is to minimize complexity and additional gate count.

4.7 Walsh Basis Vector Diversity Concept

This scheme inserts a second antenna diversity period between the header, where the high rate is selected, and the start of high rate data. No changes to current IEEE 802.11 specification (except rate field) are required as the format of the high rate data field has not been specified, and the reception of an unspecified data rate is handled per the current specification.

The concept is to transmit the 8 Walsh basis vectors twice which permits the 8 Walsh basis vectors to be received on each antenna. By this method a compromise is achieved between complexity and performance. Since the basis vectors are actually passed through the channel de-convolution is not required for an accurate performance estimate.

The Walsh distance is hardware efficient as the correlators already exist for data demodulation. Implementing the minimum and maximum processing requires approximately 1000 gates.

4.8 Walsh Diversity High Rate Frame Format

The suggested frame format, as shown in the figure (Fig. 5), includes a new field for redoing the receive antenna diversity. At this point the following data rate is known. The antenna diversity can therefor be optimized for the rate. The MAC does need to take this field into account when computing the length field. By using an unused bit in the header the BBP could decode whether or not this field is included thus permitting short 11 Mbps messages to selectively delete this approximately 15 microsecond field.

4.9 Walsh Diversity High Rate Field Format

The suggested field format, as shown in the figure (Fig. 6), includes the 6 new sub-fields required for redoing the receive antenna diversity. These sub-fields include:

1) Walsh distance for the current antenna which was selected for optimum 1 Mbps operation.
2) Guard time for antenna switching and filter decay time.
3) Timing and carrier phase acquisition for the other antenna. Since the signal to noise ratio must be relatively high for 11 Mbps operation, compared to 1 Mbps operation, between 1 and 3 8 chip symbols should be sufficient.
4) Walsh distance for the other antenna using the same 8 symbol sequence.
5) Guard time for antenna switching and filter decay time. The receiver does not need this unless the original antenna was selected but must be included.
6) Timing and carrier phase acquisition for the selected antenna. This could be shortened but included to be conservative.

4.10 AP Protocol TX Diversity Assumptions

Transmit antenna diversity can provide significant throughput improvement at little cost beyond receive diversity. The following assumptions for a simplified access point (AP) transmit antenna diversity scheme permit a low cost improvement in throughput.

The scheme must be able to be integrated with IEEE 802.11 protocol. The network is “hub-spoke” consisting of an AP & one or more stations. This means all traffic goes through an AP. The AP has dual antenna diversity, stations do not (this is the important scenario). The scheme must work for diverse & non-diverse AP’s without prior knowledge by the stations. A node knows if it is an AP. An AP knows if it has dual diversity or not. The channel is stationary for several messages (multipath spec assumes this). Assume single & multiple isolated messages with acknowledgments (ACK). The probability of 1 Mbps header loss relatively low. The AP Media Access Controller (MAC) can store & process 1 bit per station for the selected antenna. One unused header bit can be used as ACK/NAK bit. Retries occur as soon as possible. A reciprocal channel is not necessary but may used. Note that Naks are only used to prevent other stations from transmitting via CCA.

4.11 AP Protocol TX Diversity

The following description is keyed to the access point figure which consists of the transmit diagram on the left and receive on the right.

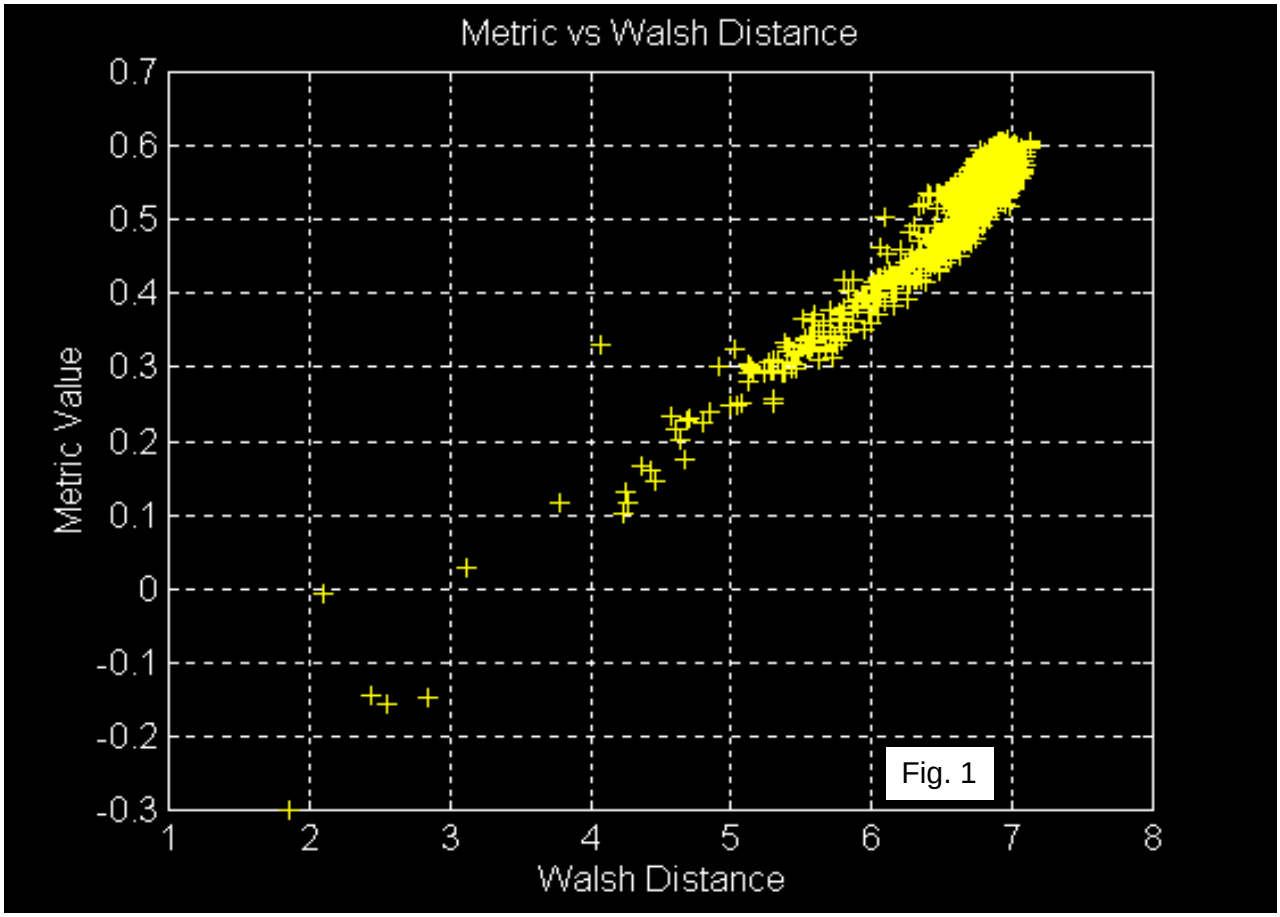
1) AP has information to transmit to a Rx Station. The Rx Station's previously selected TX antenna is used.
2) If an ACK is received the TX antenna will be used first for the next TX to that Station. The robust ACK bit in the header makes this work. The TX antenna may be modified by a later reception from the Rx Station.
3) If an ACK is not received, the message is quickly retransmitted on the other antenna.
4) See #2.
5) If an ACK is not received, neither TX antenna worked. This appears to the system as a missed message. The Rx Station's selected antenna remains unchanged as it was best in the past.
6) A Station has information to transmit to the AP. The AP's current HW diversity is used to select the Rx antenna.
7) If the data is verified the Rx antenna will be used for the ACK & the next TX to that Station. The robust ACK bit in the header makes this work. The TX antenna may be modified by a later reception from the Rx Station.
8) If the data is not verified a NAK is sent on the Rx antenna & the message will be quickly. retransmitted for reception on the other antenna. The Rx antenna is used for the NAK as the other may have no communication. The NAK prevents other Stations from transmitting.
9) See #7.
10) If the data is not verified, neither Rx antenna worked. This appears to the system as a missed message. A NAK may be retransmitted to reduce number of control states.

The following description is keyed to the station figure which consists of the transmit diagram on the left and receive on the right.

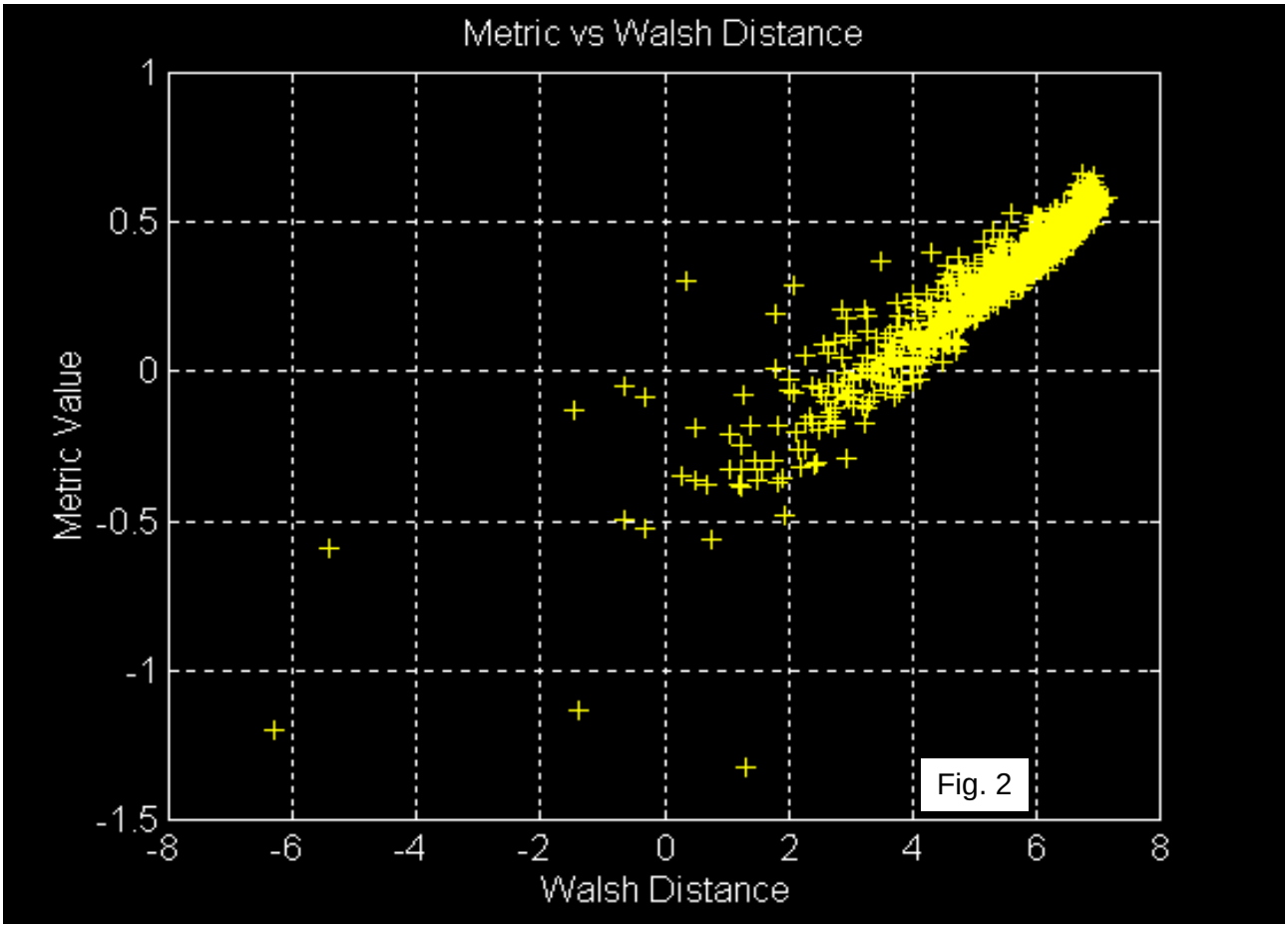
1) The station has information to transmit to an AP.
2) If an ACK is received the message was received. The robust ACK bit in the header makes this work.
3) If an ACK is not received, the message is quickly retransmitted.
4) See #2.
5) If an ACK is not received, neither AP Rx antenna worked. This appears to the system as a missed message.
6) AP has information to transmit to a station.
7) If the data is verified an ACK is transmitted to the AP. The robust ACK bit in the header makes this work.
8) If the data is not verified a NAK is sent & the message will be quickly retransmitted. The NAK prevents other stations from transmitting.
9) See #7.
10) If the data is not verified, neither AP TX antenna worked. This appears to the system as a missed message. A NAK may be retransmitted to reduce number of control states.

This scheme helps AP to station messages by adding AP TX antenna diversity, it does little for station to AP throughput unless short probe messages are used. Improvements can be made biased on various realistic assumptions: e.g. Having the stations tell the AP which Rx antenna to use biased on their receptions & a reciprocal channel assumption. This would require a change in the preamble or a change in the inter-message gap timing.

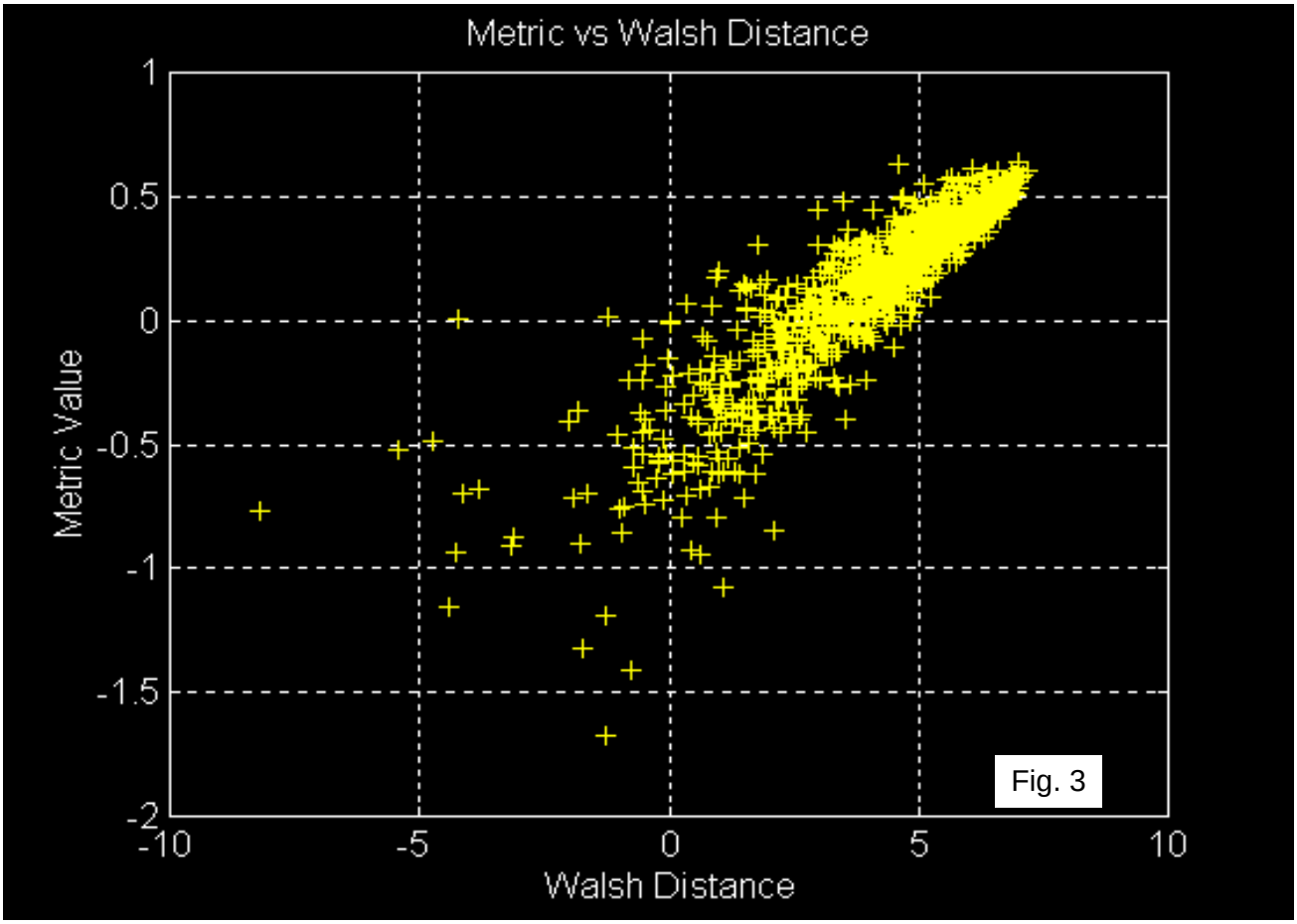
IF Limiter Diversity Metric Performance @ 10 ns RMS



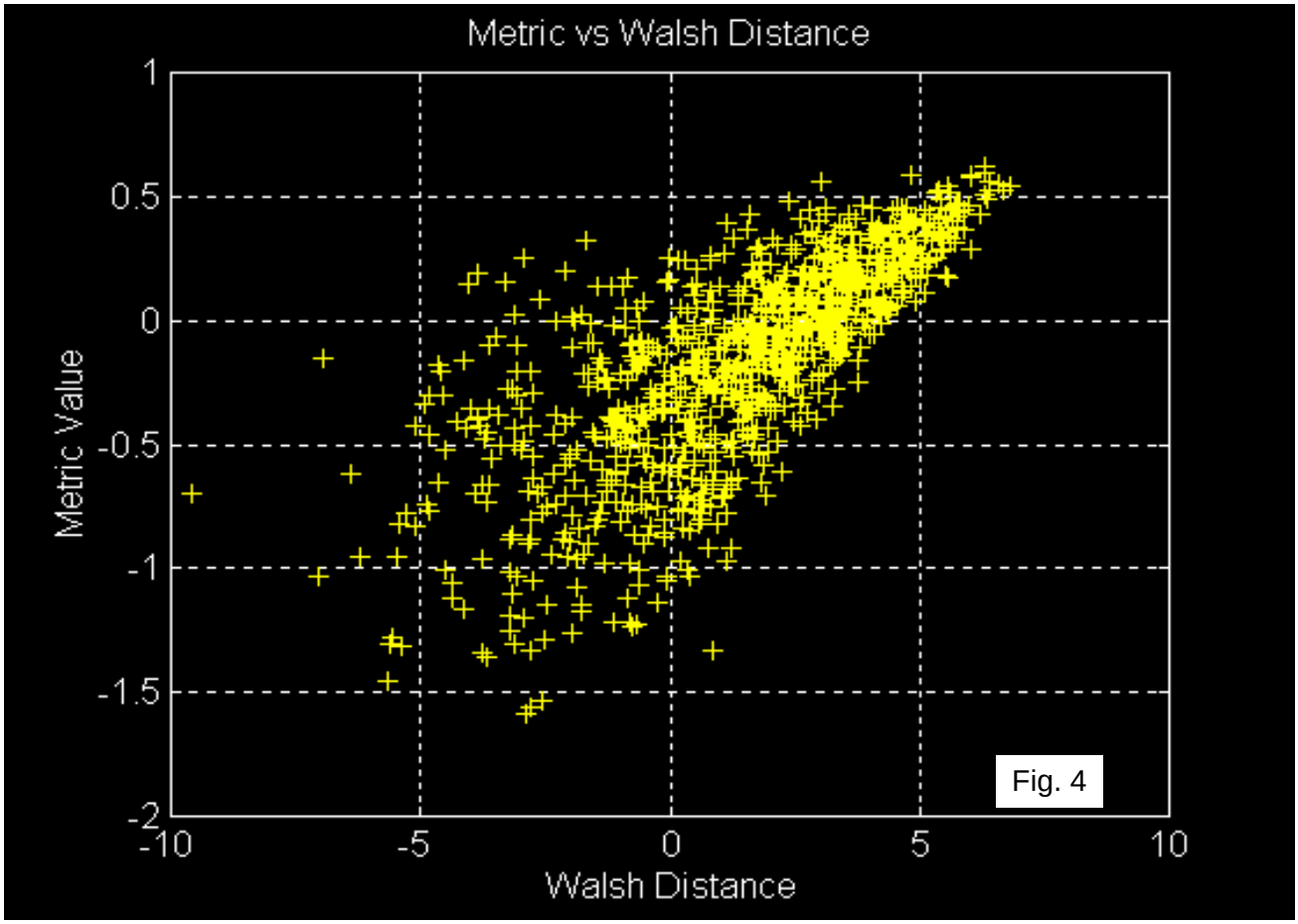
IF Limiter Diversity Metric Performance @ 25 ns RMS



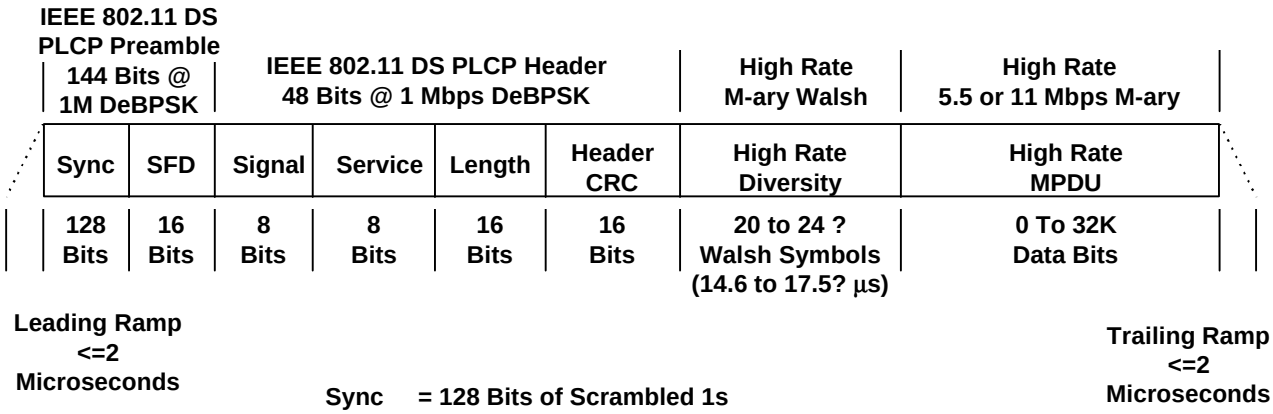
IF Limiter Diversity Metric Performance @ 50 ns RMS



IF Limiter Diversity Metric Performance @ 100 ns RMS



Walsh Diversity High Rate Frame Format



Sync = 128 Bits of Scrambled 1s
SFD = Start Frame Delimiter (Unique Word) (F3A0h)
Signal = 5.5 or 11 Mbps M-Ary
Service = Reserved (00h)
Length = 0 to 2^{16}-1 Microseconds
CRC = CCITT CRC-16 FCS

Note: 1 bit of the header could be used to indicate if the high rate diversity will be transmitted or not, this removes the the diversity time penalty for non diverse Rx stations

Fig. 5

Walsh Diversity High Rate Field Format

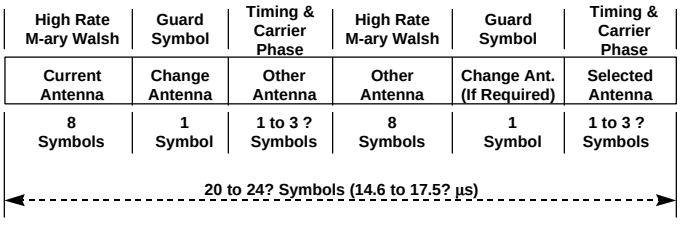


Fig. 6

AP Protocol Tx Diversity @ the AP

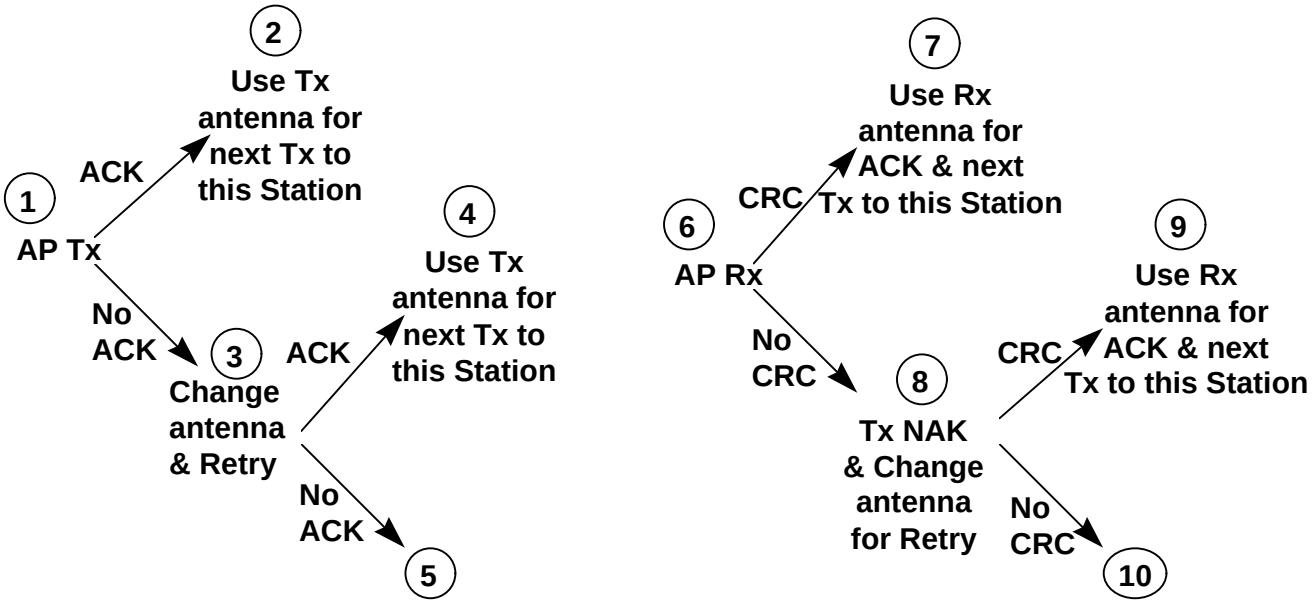


Fig. 7

AP Protocol Tx Diversity @ a Station

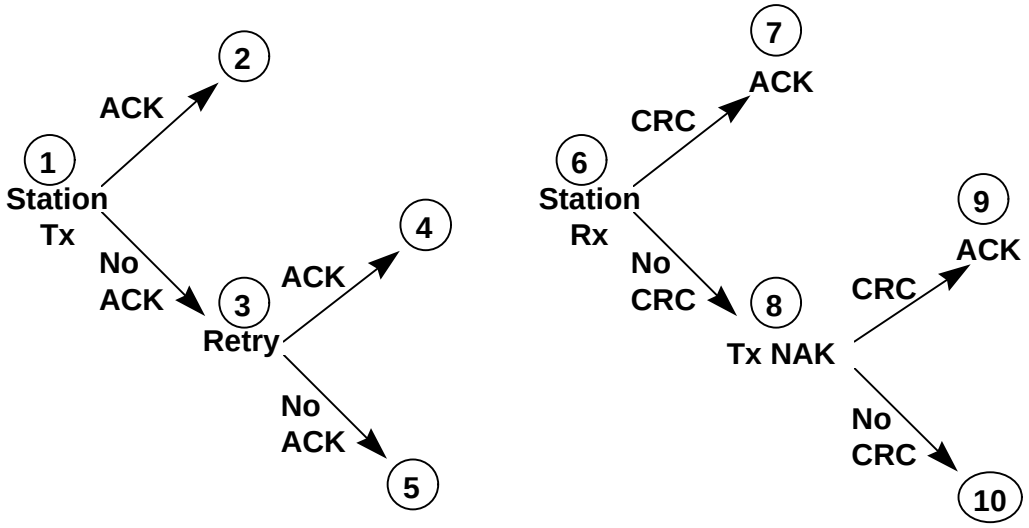


Fig. 8

5. Spectral and Waveform Efficiency.

This section includes data concerning the waveform and spectral efficiency of the proposed basic waveform. Most of the data is empirical using the Harris PCMCIA radio design which implements the Harris proposed basic waveform. The empirical data provides an excellent mechanism to estimate feasibility and implementation losses from theory.

The section begins with sensitivity data for all proposed rates, as well as TX power efficiency to continue with co-channel and adjacent channel performance data.

5.1 CO-CHANNEL INTERFERENCE PERFORMANCE OF THE HFA3860 WAVEFORM

5.1.1 Test Description

The objective of the testing is to establish the co-channel interference performance of the radio implementation of the HFA3860 waveform under controlled laboratory conditions.

5.1.2 Test Configuration

The tests are conducted with one HFA3860 evaluation platform operating as transmitter in a cabled connection to a second HFA3860 evaluation platform operating as receiver. Step attenuators are used to emulate the radio path loss to the receiver to maintain a level above the required sensitivity level of the receiver for maximum effective throughput. A third HFA3860 evaluation platform, operating on the same RF channel as the transmitter and receiver, is step attenuated and combined with the intended transmitter output to act as the interfering or jamming source on the link. Step attenuators at the output of the HFA3860 transmitter and step attenuators at the output of the interfering HFA3860 platform are set to control the relative level of jammer to signal (J/S) ratio on the cabled HFA3860 link.

The test configuration is depicted in Figure 5.1-1.

The Harris HFA3860 Evaluation Program is used to evaluate the packet error rate (PER) and effective throughput on the cabled link measured at the receiving HFA3860 platform, as the measurement parameters of J/S level in dB and the nominal data rate transmitted by the interfering source are varied.

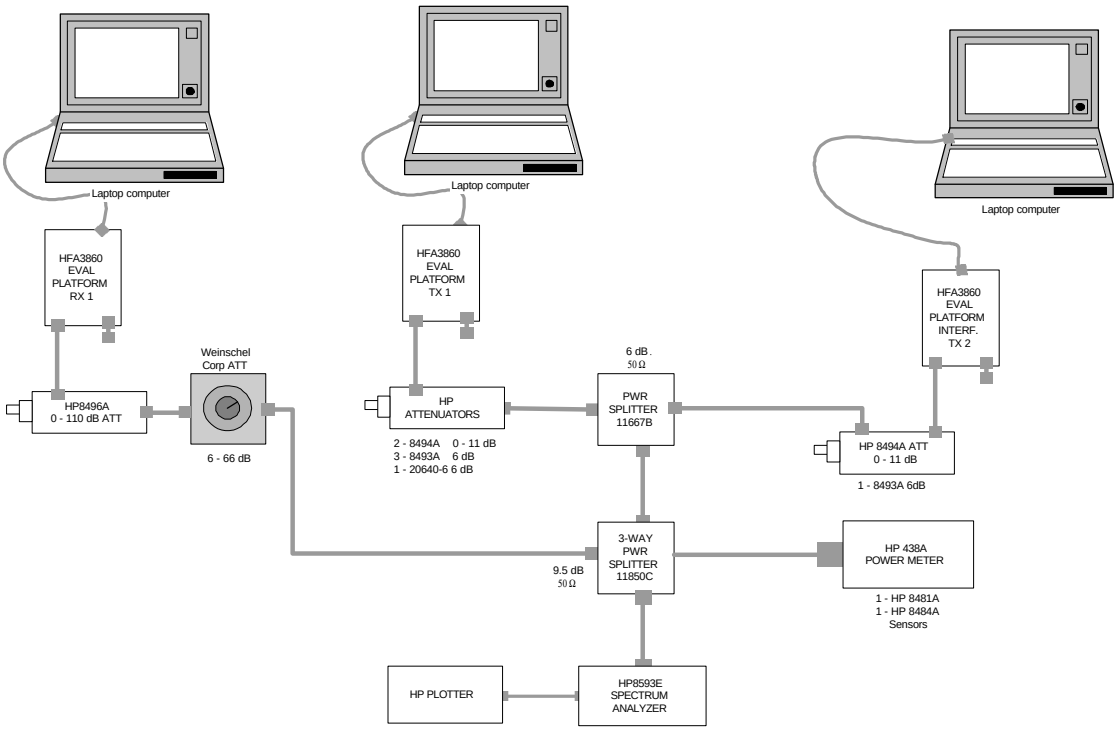


Figure 5.1-1 Test Configuration for Co-channel and Adjacent Channel Interference Testing

5.1.3 Procedure

The attenuation between the receiving HFA3860 platform and the combined output of the transmitting HFA3860 evaluation platform and interfering platform on the cabled link is held fixed. All three platforms are operating on the same RF channel. The nominal data rate on the intended HFA3860 link is set at 11 Mbps. The step attenuators at the output of the transmitting HFA3860 evaluation platform and at the output of the interfering platform are set to the smallest

values necessary to cause a measured PER of zero at the receiver platform. The attenuation settings are recorded. The signal levels from the transmitting HFA3860 platform and the interfering platform are individually recorded on an average power meter to establish the J/S value in dB for this result. The throughput and PER values for these settings are recorded.

In the next step, the step attenuators at the transmitter output and interfering platform output are incremented to values that result in a measured PER of close to 10% at the receiver platform . Again the signal levels of the transmitter and interferer outputs are individually measured and the corresponding J/S value computed. The effective throughput and PER values for these settings are recorded at the receiving HFA3860 platform.

The procedure is repeated to effect higher PER (lower throughput) values at the receiving platform, until the intended link is lost due to the interference level.

The procedure is performed for the nominal data rate of the interferer platform set to 1 Mbps and to 11 Mbps. The packet size for all platforms is set to 1024 bytes and the packet gap is set to 20 μs.

5.1.4 Test Results

The results of the co-channel interference tests for the HFA3860 waveform are summarized in Figures 5.1-2 through 5.1-5. Each chart displays the PER or throughput versus measured J/S value. The results shown are for the transmitter and receiver on Channel 6 at a nominal data rate of 11 Mbps, while the interfering platform transmits on the same channel at a nominal rate of 1 Mbps or 11 Mbps. It is clear from the results that the co-channel wideband interferer must be substantially below the intended transmitter's signal level for acceptable link performance to be achieved.

Figure 5.1-6 shows the spectral trace of the desired transmit signal (green) in Channel 6 with a second trace of the co-channel HFA3860 signal (blue) at the maximum power level to induce a PER of 0 at the receiver and a third trace at the higher power level (blue) to sufficient to cause a PER of 9% at the receiver. The nominal rate on the co-channel interferer is 1 Mbps. All traces were averaged over 100 samples.

Figure 5.1-2 PER VERSUS CO-CHANNEL INTERFERENCE TO SIGNAL RATIO
11-Mbps Interferer on 11-Mbps Link

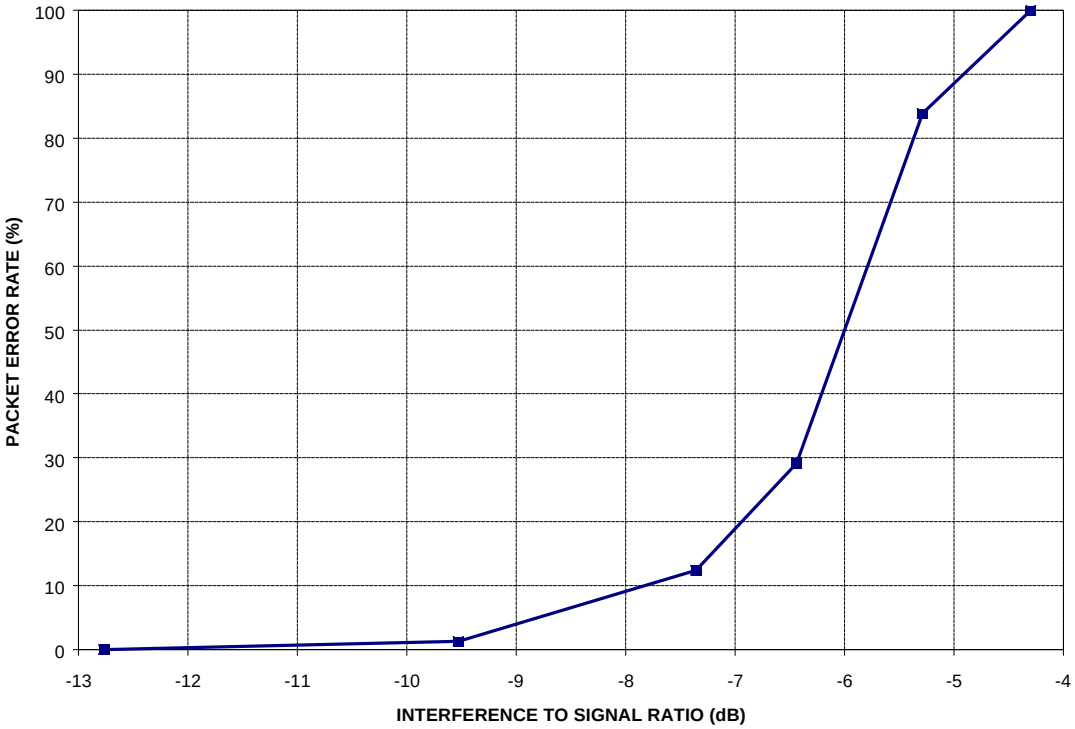


Figure 5.1-3 THROUGHPUT VERSUS CO-CHANNEL INTERFERENCE TO SIGNAL RATIO
11 Mbps Interferer on 11 Mbps Link in Channel 6

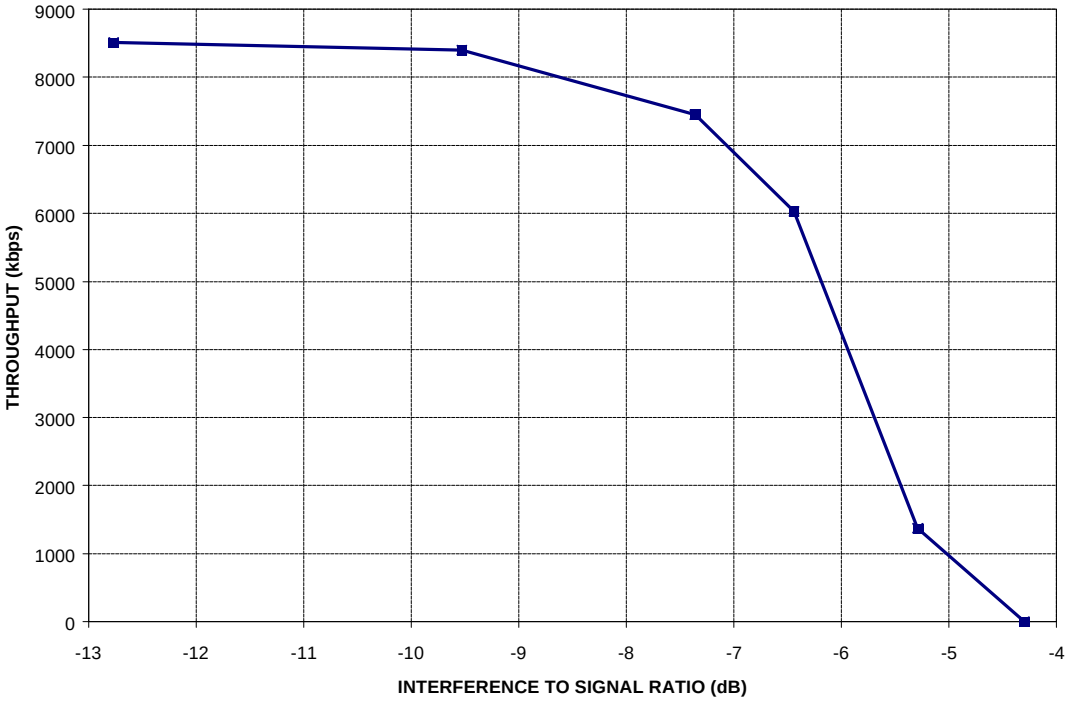


Figure 5.1-4 PER VERSUS CO-CHANNEL INTERFERENCE TO SIGNAL RATIO
1 Mbps Interferer on 11 Mbps Link in Channel 6

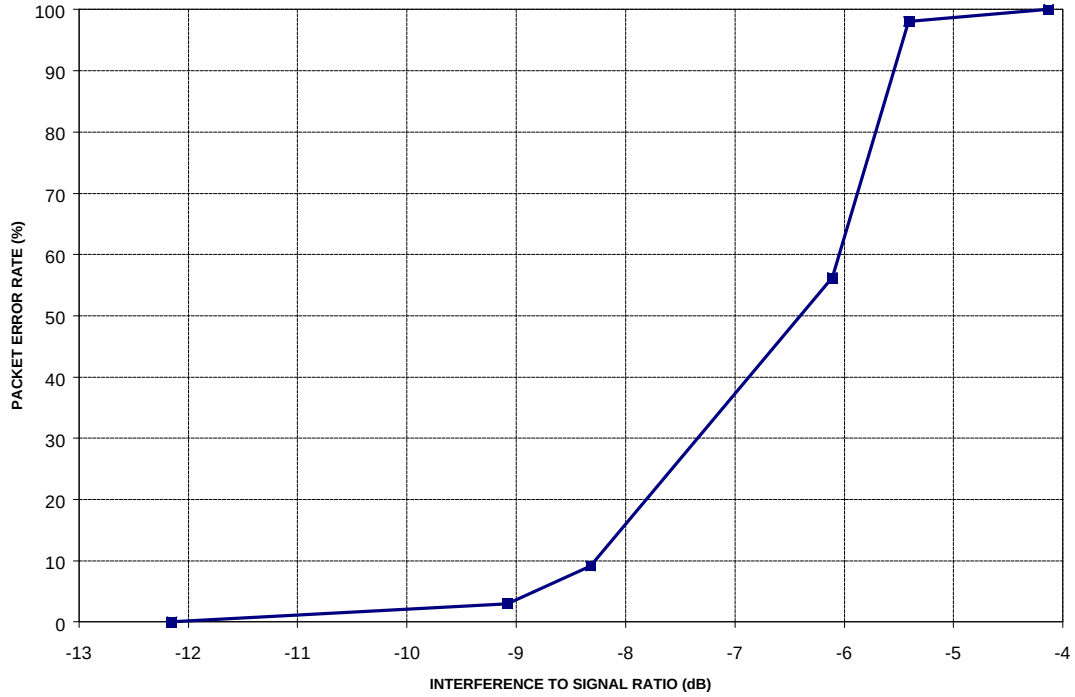
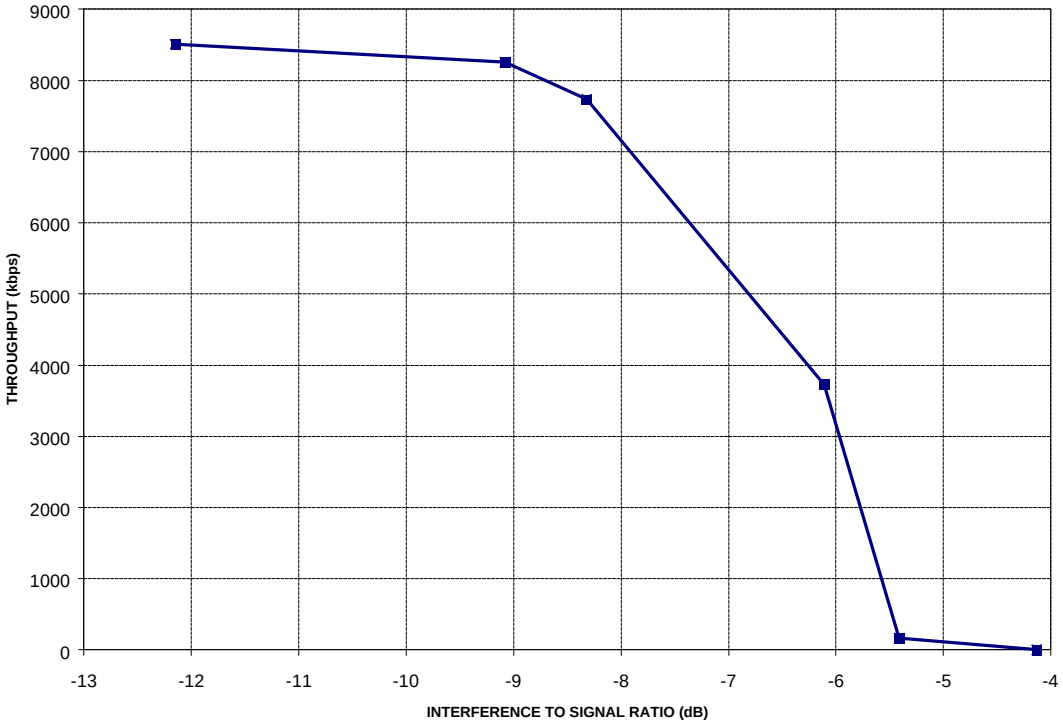


Figure 5.1-5 THROUGHPUT VERSUS CO-CHANNEL INTERFERENCE TO SIGNAL RATIO
1 Mbps Inteferer on 11 Mbps Link in Channel 6



5.2 ADJACENT-CHANNEL INTERFERENCE PERFORMANCE OF THE HFA3860 WAVEFORM

The adjacent channel performance is strongly dependent on the RF and IF components in the transmitter and receiver. This performance is expected to be only slightly worse than the performance of a radio designed to the 802.11 standard due to the 6 dB higher required operating SNR. With similar codes, there is the possibility of additional interference due to correlation just as with the 1 and 2 Mbps techniques.

5.2.1 Packet Error Rate and Sensitivity at 11Mbit and 5.5Mbit Data Rates

Packet Error Rate sensitivity data was taken at both the 5.5Mbit and 11Mbit rates. This data is plotted below for two units at each data rate. The expected 5.5Mbit and 11Mbit difference is -3dB for 11Mbit. The last point plotted for 100% PER indicates a no receive point. Data repeatability was confirmed for the last two PER points on each curve. Sensitivity measurements on a significant quantity of units show these as typical to good performance for PER.

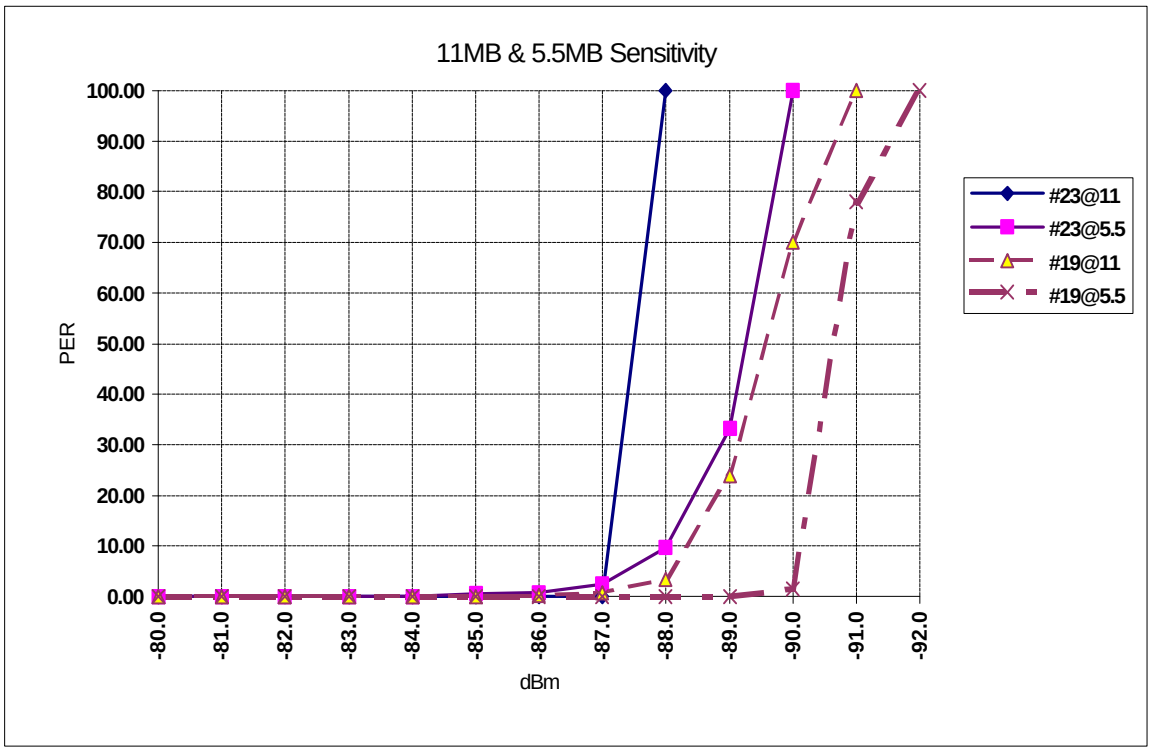
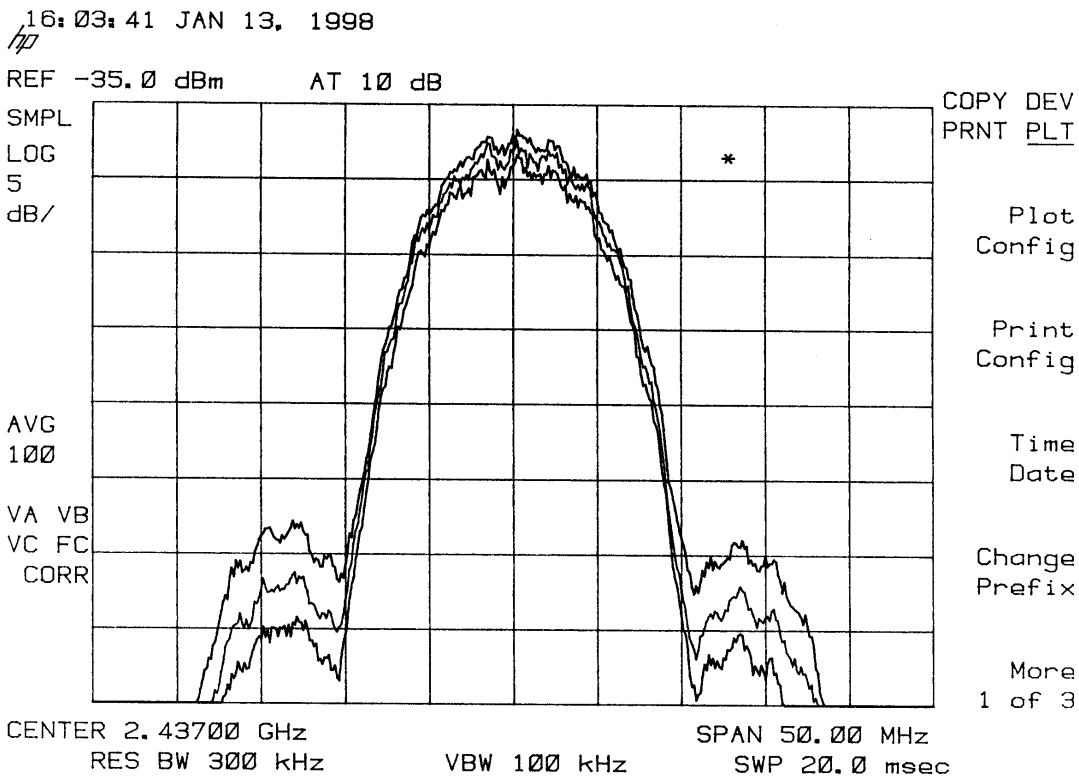


Figure 5.0.1 Sensitivity for all rates.

B. Frequency Spectrum and Amplifier Drive Level

The frequency plots for the spectrum of a transmitter adjusted for +18dBm, +19dBm, and +20dBm show the effects of reduced output backoff from the 1dB compression point . The plot below demonstrates amplifier overdrives of 1dB, 2dB, and 3dB. Sidelobe sensitivity is approximately 3dB for each 1dB of output increase. The amplifier typically operates at an output backoff from -5 to -2dB without sidelobe spectral regrowth above -30dB. Units are setup for +16dBm output and the spectrum verified for -30dB sidelobes.



6. Interference Immunity

This section includes interference immunity data taken empirically. The Harris PCMCIA radio design was used. This radio is an implementation of the basic waveform proposed by Harris. No architectural enhancements have been tested.
Three tests were used to test interference immunity.

A. A CW interference using the FCC CW test suggested for DS processing gain.

B. An FH (802.11) waveform jammer.

C. Broadband noise.

6.1 Interference using the FCC CW processing gain test

One of the interference immunity tests is the CW test recommended by the FCC for processing gain

6.1.1 Test Procedure

Obtain the simplex link as shown on the test configuration figure. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).

2. Signal Power at power meter between -20 and -40 dBm for optimal linearity.

3. Use spectrum analyzer to monitor test.

4. Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, S_r.

5. Disable Transmitter, and enable CW Jammer generator RF output. Set reference CW Jammer power level at power meter port 8.6 dB below S_r (minimum J/S, or 10 dB processing gain reference level), set frequency to signal carrier frequency. Note the power level setting on the generator, this is the reference CW Jammer power setting, J_r.

6. Disable CW Jammer, re-establish link. BER test set should be operating error-free.

7. Enable CW Jammer at a low power level and gradually increase the CW Jammer power until the BER test set indicates the reference BER level ($1 \bullet 10^{-5}$). Note nominal Jammer power setting, J_n.

This test is repeated for a fixed signal carrier frequency and for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is ±8.5 MHz. The procedure can be illustrated as follows:

For offset frequency - 8.5 MHz to carrier frequency + 8.5 MHz , Step 50 kHz.
Do:
Adjust Nominal Jammer Level setting.
Until:
Average BER is equal to reference BER.
Record Indicated Nominal Jammer Level setting.
Next offset frequency.

The nominal Jammer Level settings are tabulated versus offset frequency. The J/S ratio and the processing gain are then calculated as follows:

$$\left(\frac{J}{S}\right) = -\left[\left(S_r - J_n\right) - \left(S_r - 8.6\,dB - J_r\right)\right]$$

If $J_n = J_r$ then:

$$\left(\frac{J}{S}\right) = -\left[8.6\,dB\right]$$

is the J/S ratio associated with 10 dB processing gain.

The processing gain then is determined using the J/S ratio:

$$G_p = 18.6\ dB\ +\ \left(\frac{J}{S}\right)$$

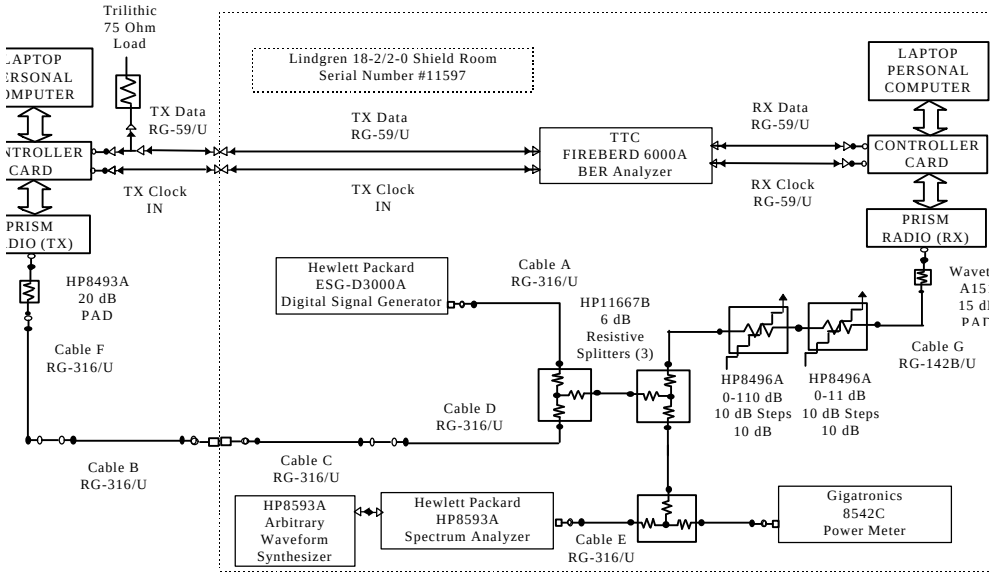
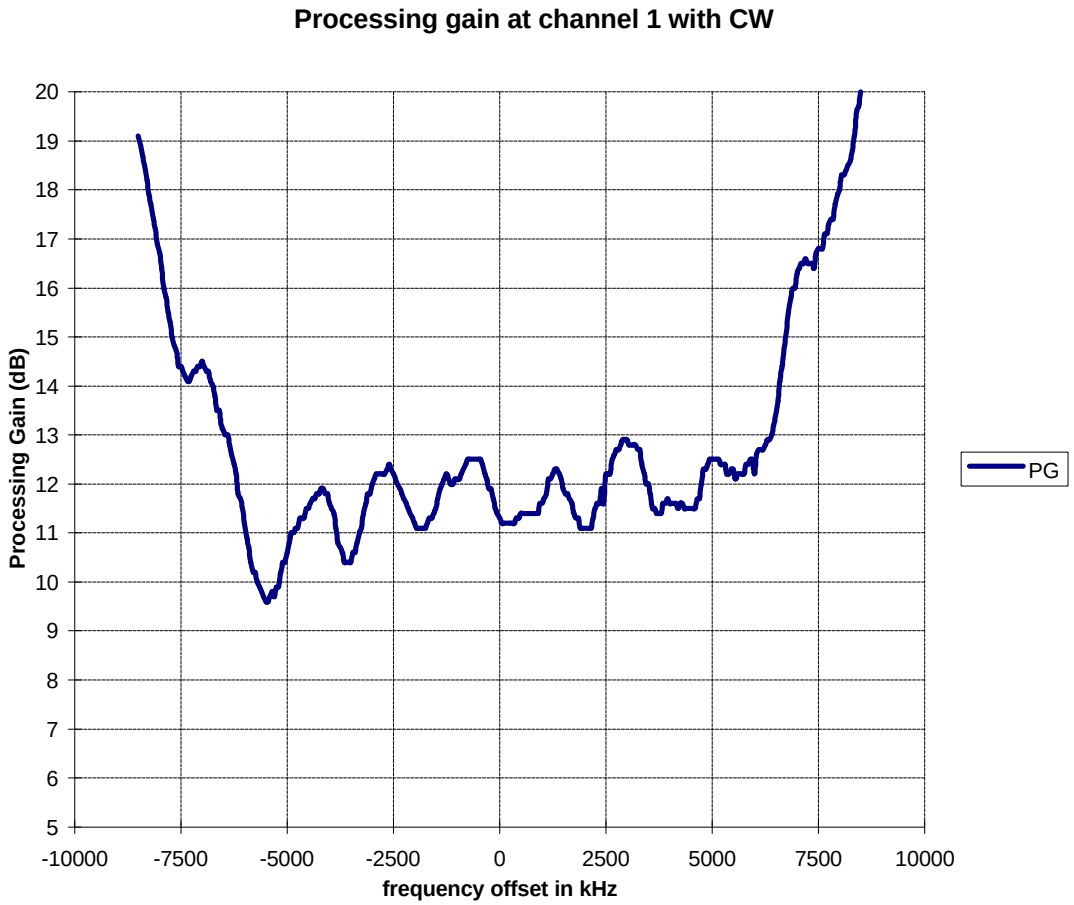


Figure 6.1.1 Test configuration for CW Interference tests.

The test results for Channel 1 are illustrated on the plot below. The results for this channel translate to a processing gain of 11.3 dB per the FCC suggested calculation.



The minimum processing gain with 20% worst points removed is 11.3 dB.
Figure 6.1.2 CW Interference data

6.2 Frequency Hop interference analysis.

The jamming margin tests were repeated with a simulated frequency hopping jammer. The frequency hopping jammer is essentially a FM modulated version of the jamming signal. A 31 bit maximal-length sequence was programmed into an arbitrary waveform synthesizer and applied to the FM modulation port of the Jamming signal source with a frequency deviation of ±110 kHz and a data rate of 1 Mbps. The frequency deviation was determined by adjusting the deviation until the 20 dB bandwidth of the resulting spectrum was 1 MHz. A plot of the baseband waveform and the resulting spectrum are presented in Appendix C.

The processing gain measurements were carried out in the same fashion with the modulated jammer. The number of offset frequency points was reduced due to the fact that this was a verification test that the frequency hopped jammer did not impair the CW derived processing gain. The frequency hopped jamming margin tests used 50 KHz increments for ±2 MHz and 200 KHz increments between ±2 MHz and ±8.5 MHz. The frequency hopped jammer points are overlaid onto the CW data for the same channel.

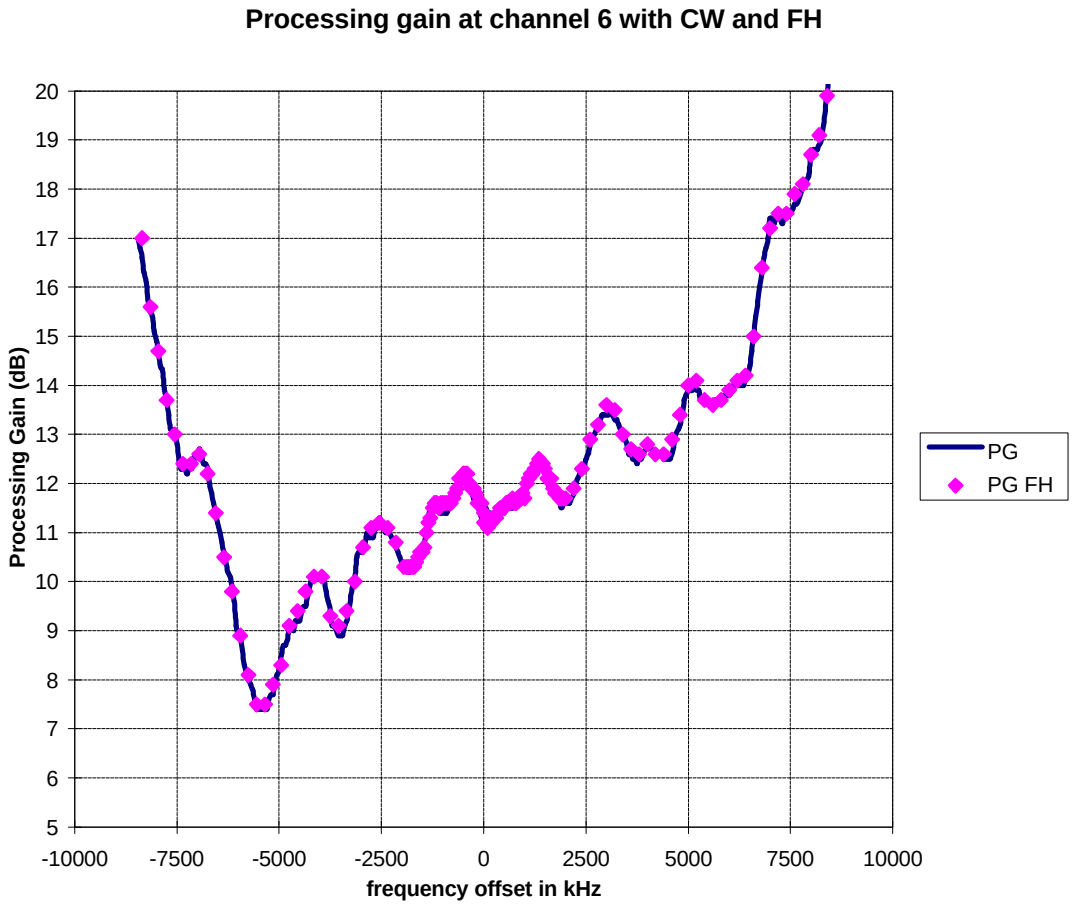
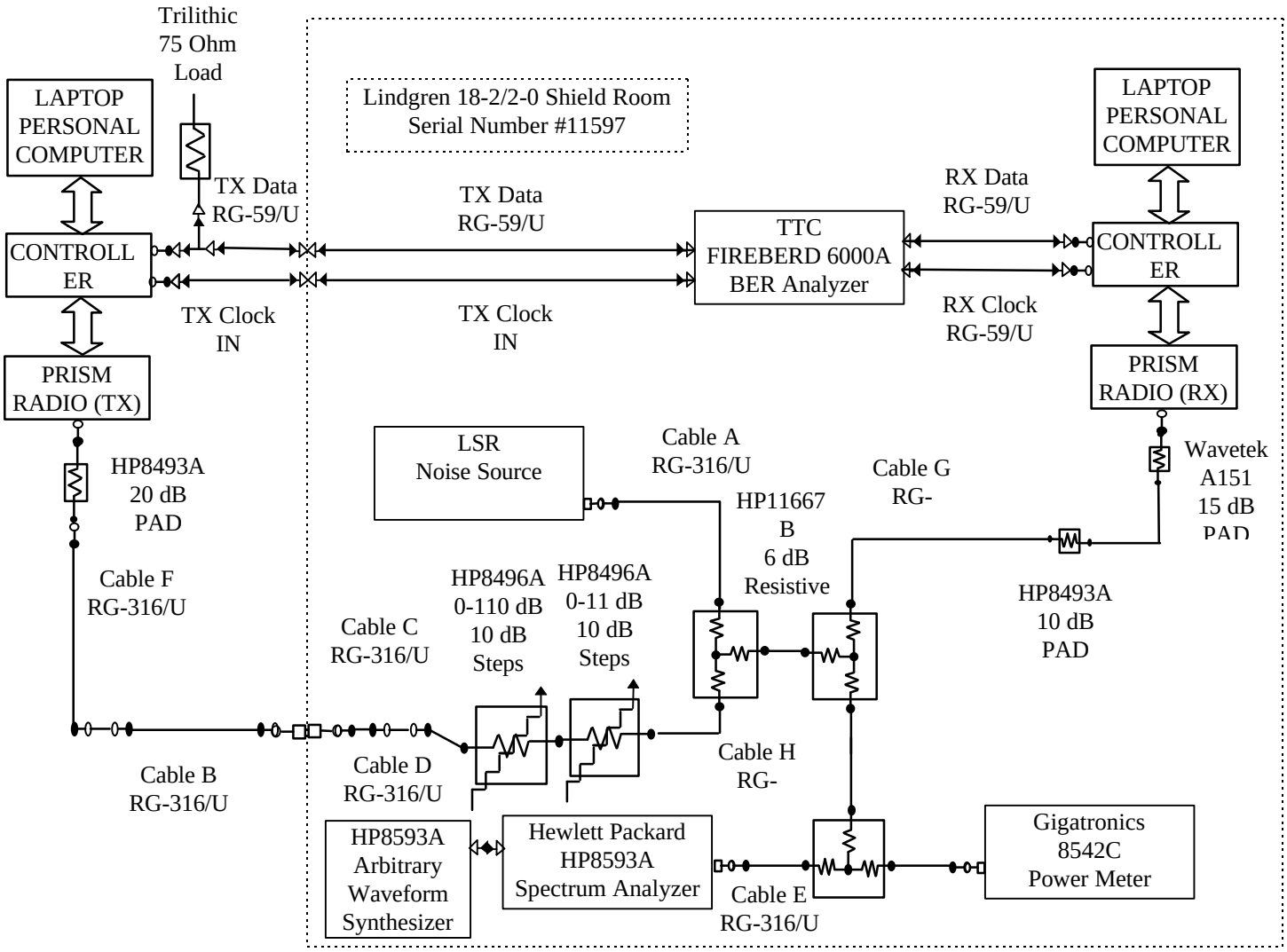


Figure 6.2.1 FH Interference data.

6.3 Broadband Jammer Interference Test.

An additional method of interference test is to use one broadband jamming source to perform the jamming margin tests and indirectly measure the processing gain. The test configuration was altered since the available noise source had a fixed output level. The variable attenuators were placed in front of the Jammer/signal summing junction in order to control the J/S ratio by variation of the signal level. The noise (jammer) and the signal levels were measured on the spectrum analyzer utilizing the channel power measurement mode.. A link was established for 5 different signal levels. At each signal level, the BER, and signal power was measured. Since the attenuators are continuously variable, the location of the reference BER needs to be interpolated from the aforementioned data.


Trilithic
75 Ohm
Load
LAPTOP
PERSONAL
COMPUTER
Lindgren 18-2/2-0 Shield Room
Serial Number #11597
LAPTOP
PERSONAL
COMPUTER
TX Data
RG-59/U
TX Data
RG-59/U
RX Data
RG-59/U
CONTROLL
ER
TTC
FIREBERD 6000A
BER Analyzer
CONTROLL
ER
TX Clock
IN
TX Clock
IN
RX Clock
RG-59/U
PRISM
RADIO (TX)
PRISM
RADIO (RX)
HP8493A
20 dB
PAD
LSR
Noise Source
Cable A
RG-316/U
Wavetek
A151
15 dB
PAD
Cable G
RG-
HP11667
B
6 dB
Resistive
Cable F
RG-316/U
HP8496A
0-110 dB
10 dB
Steps
HP8496A
0-11 dB
10 dB
Steps
HP8493A
10 dB
PAD
Cable C
RG-316/U
Cable B
RG-316/U
Cable D
RG-316/U
Cable H
RG-
HP8593A
Arbitrary
Waveform
Synthesizer
Hewlett Packard
HP8593A
Spectrum Analyzer
Gigatronics
8542C
Power Meter
Cable E
RG-316/U

C	N (J)	C/N (S/J)	PG	BER
-43.2	-52.2	9	9.6	1.20E-06
-44.2	-52.2	8	10.6	6.80E-06
-45.1	-52.2	7.1	11.5	2.30E-05
-45.9	-52.2	6.3	12.3	1.80E-04
-46.7	-52.2	5.5	13.1	6.40E-04

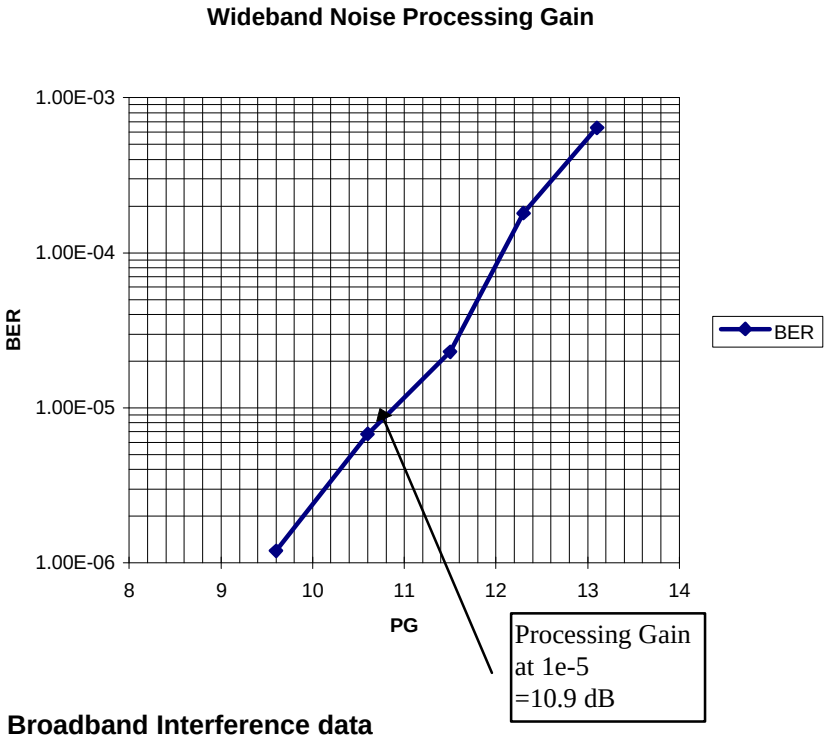


Figure 6.3.1 Broadband Interference data

6.4 INTERFERENCE BETWEEN THE HFA3860 WAVEFORM AND IEEE 802.11 FREQUENCY HOP WIRELESS LINKS

6.4.1 Performance of the HFA3860 Waveform in the Presence of 3-Mbps Frequency Hop Wireless Link

6.4.1.1 Test Description

The objective of the testing is to establish the performance of the radio implementation of the HFA3860 waveform in the presence of a typical high-rate IEEE 802.11 frequency hopped (FH) wireless link under controlled laboratory conditions.

6.4.1.2 Test Configuration

The tests are conducted with one HFA3860 evaluation platform operating as transmitter in a cabled connection to a second HFA3860 evaluation platform operating as receiver. Step attenuators are used to emulate the radio path loss to the receiver to maintain a level above the required sensitivity level of the receiver for maximum effective throughput. A second FH wireless link is established as a cabled connection between an FH access point adapter, operating as link transmitter, and an FH station adapter, taken to be the link receiver. The FH link is configured to operate at a nominal rate of 3 Mbps.

In order to verify the quality of the FH link, the Harris LAN Evaluation Program is run in Streaming Point-to-Point Mode to evaluate the effective throughput on the cabled FH link. The output of the FH transmitter is power split and one output is fed to a series of step attenuators and combined with the HFA3860 transmitter output to act as the interfering or jamming source on the link. Step attenuators at the output of the HFA3860 transmitter and step attenuators at the output of the interfering FH link transmitter are set to control the relative level of jammer to signal (J/S) ratio on the cabled HFA3860 link.

The test configuration is depicted in Figure 6.4-1.

The Harris HFA3860 Evaluation Program is used to evaluate the packet error rate (PER) and effective throughput on the cabled link measured at the receiving HFA3860 platform, as the measurement parameter of J/S level in dB is varied.

6.4.1.3 Procedure

The attenuation between the receiving HFA3860 platform and the combined output of the transmitting HFA3860 evaluation platform and interfering FH transmitter is held fixed. The HFA3860 transmitter and receiver are configured to operate on Channel 6. The nominal data rate on the intended HFA3860 link is set at 11 Mbps. The nominal data rate on the FH link is set at 3 Mbps. The throughput rate on the FH link is monitored using the Harris LAN Evaluation Program to ensure that the FH link is operating normally.

The step attenuators at the output of the transmitting HFA3860 evaluation platform and at the output of the interfering platform are set to the smallest values necessary to cause a measured PER of zero at the HFA3860 receiver platform. The attenuation settings are recorded. The signal levels from the HFA3860 transmitter and the interfering FH transmitter are individually recorded on an average power meter to establish the J/S value in dB for this result. The throughput and PER values are recorded at the HFA3860 receiver for these settings.

In the next step, the step attenuators at the transmitter output and interfering FH transmitter output are incremented in values that result in a measured PER of close to 10% at the receiver platform. Again the signal levels of the transmitter and interferer outputs are individually measured and the corresponding J/S value computed. The effective throughput and PER values for these settings are recorded at the receiving HFA3860 platform.

The procedure is repeated to effect higher PER (lower throughput) values at the receiving platform, until the intended link is lost due to the interference level.

The packet size for HFA3860 evaluation platforms is set to 1024 bytes and the packet gap is set to 20 μs. The packet size for the FH wireless adapters is set at the recommended 400 bytes.

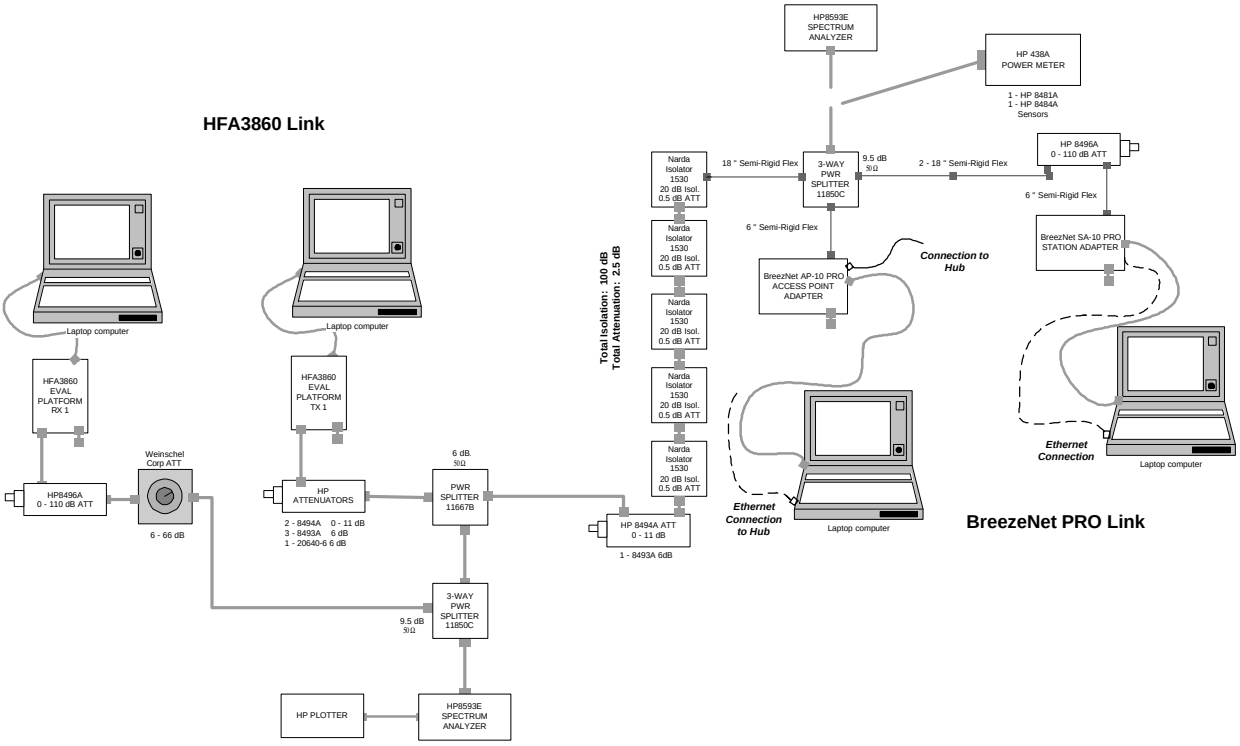


Figure 6.4.1-1 Test Configuration for Interference Testing of HFA3860 Evaluation Platforms and FH Wireless Adapters

6.4.1.4 Test Results

The results of the tests to characterize HFA3860 waveform's sensitivity to FH interference are summarized in Figure 6.4.1-2 and Figure 6.4.1-3. Each chart displays the PER or effective throughput versus measured J/S value. The results shown are for the transmitter and receiver on Channel 6 at a nominal data rate of 11 Mbps, while the interfering FH platform transmits at a nominal rate of 3 Mbps.

Figure 6.4.1-4 shows the spectral trace of the desired HFA3860 transmit signal in Channel 6 with a second trace of the FH interferer at a minimum level to maintain a PER of 0% at the HFA3860 receiver. Figure 6.4.1-5 shows the spectral trace of the HFA3860 signal in Channel 6 with a second trace of the FH interferer at a level that induces a PER of 9.75% at the HFA3860 receiver. The HFA3860 traces in Figures 6.4.1-4 and -5 are averaged over 100 samples.

Figure 6.4.1-2 PER VERSUS FREQUENCY HOPPING INTERFERENCE
Breeze Net FH Transmitter at 3 Mbps Interfering HFA3860 11-Mbps Link on Channel 6

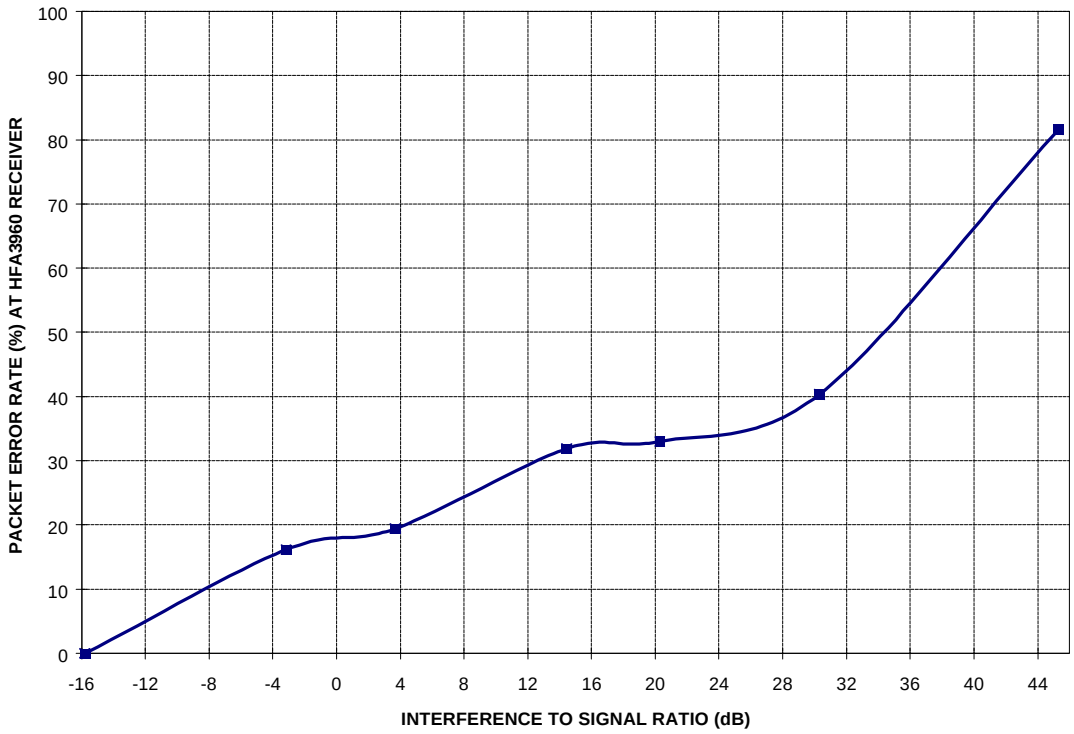
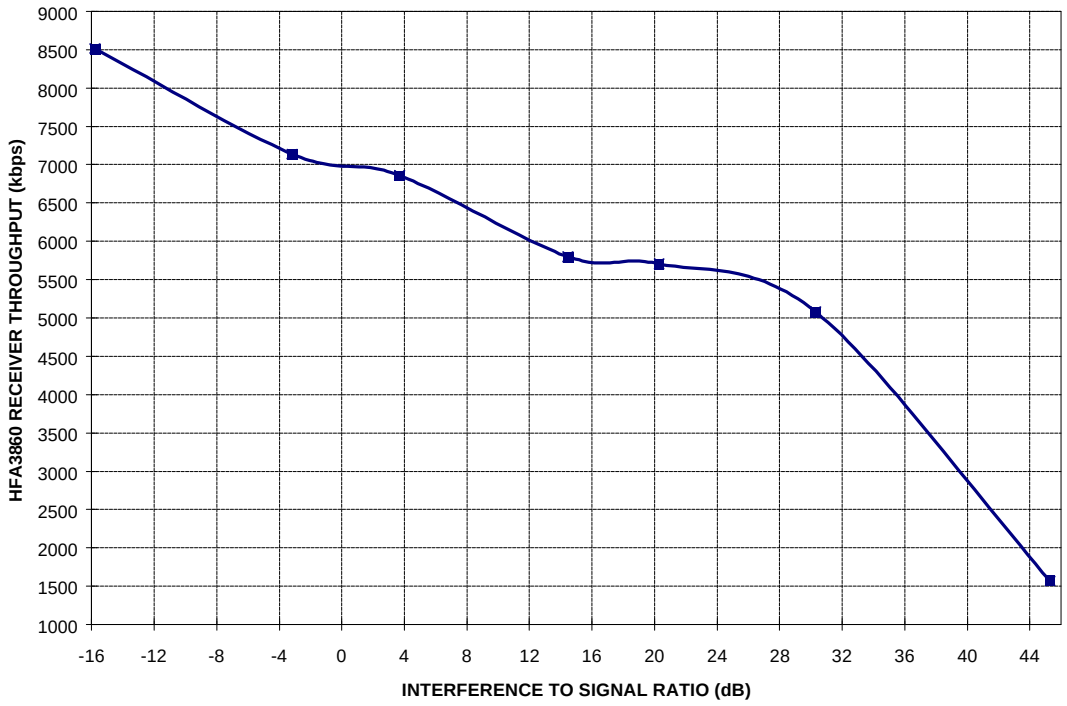


Figure 6.4.1-3 THROUGHPUT VERSUS FREQUENCY HOPPING INTERFERENCE
Breeze Net FH Transmitter at 3 Mbps Interfering HFA3860 11-Mbps Link on Channel 6



7. Interoperability for the 2.4 GHz High Rate Proposal

The development of a high data rate extension must address interoperability and compatibility to the existing 1 and 2 Mbps FH and DS WLAN systems. This section describes the options available for maintaining some or no backward compatibility and proposes an approach. The merits and drawbacks of the proposed approach are discussed relative to the market transition to 10 Mbps, data throughput and network system capacity.

7.1 Interoperability Defined

Interoperability can be defined in a number of ways. It can extend from full compliance to the existing architecture for higher data rates to a completely new modulation and protocol that does not communicate at all with existing 802.11 1 and 2 Mbps systems.
Some of the options to be considered for the interoperability of the low speed and high speed systems are:

1. **Use Of A Common Preamble And Header**
   This approach uses the mechanism defined in the current 802.11 standard. The preamble and header are always transmitted at 1 Mbps and the SIGNAL field is used to define the data rate for the Frame Body. The rates are defined in the Basis Service Set (BSS) Basic Rate Set. All Direct Sequence Spread Spectrum (DSSS) stations compliant to the current standard will be able to receive and understand the control fields. This approach allows for reliable clear channel assessment and use of the deferral mechanism. This will improve network coordination and reduce the frequency of collisions.
2. **Requirement for Backward Compatibility**
   If the selected high speed physical layer implementation does not provide any direct (antenna to antenna data transfer) connectivity to the legacy systems the standard could require backward compatibility at the lower rates. For a WLAN adapter to claim compliance to the 802.11 standard it would have to support either the existing FH or DS standard. This is analogous to dual mode cellular phones that can operate with digital or analog carriers.
3. **Data Connectivity Using Access Points**
   For methods that do not support direct antenna to antenna data communications the Access Point can provide a transfer mechanism. The APs would be required to support all rates for stations in the BSS. A high speed station would transmit a packet to the AP at the high data rate and then the AP would transmit the data to the destination at the lower rate. This would not provide any mechanism for ad hoc networks to operate with both low and high data rate stations.
4. **Carrier Sense Capability Only**
   Another option that could be used is for a high speed physical layer that does not communicate with low speed stations is to provide the carrier sense capabilities. Without some method of detecting existing low speed stations that are operating in the area the high rate station cannot participate in the Carrier Sense Multiple Access Collision Avoidance (CSMA/CA) mechanism. The use of incompatible high speed and low speed stations in the same area without any mutual carrier sense would result in what is effectively an Aloha protocol. Rather than deferring for a random back-off period when a carrier is sensed the stations will have to try to transmit and use the retry mechanism if a collision corrupts the packet. This will degrade the overall system throughput as the result of more collisions. By adding the capability to detect IEEE 802.11 transmissions (DSSS, FHSS or both) the high speed station could implement the CSMA/CA mechanism. However, depending of the modulation selected the stations using the current clear channel assessment method may not be able to sense the high data rate transmissions. If not, the rate of collisions will be higher than a system using common preamble and header.
5. **No Compatibility**

If there is no common data rates between high and low rate systems and neither can sense the other's carrier then collocated networks will work as an Aloha protocol as described above. There is no reasonable upgrade path for moving from 2 Mbps to 10 Mbps. Users will have to contend with the mutual interference of the two systems and have no direct mechanisms for the different rate stations to communicate. Dual APs would be required in an area where the customer wants to upgrade some users to the higher rate

7.2 Harris' Proposed Approach to Interoperability

In developing a physical layer proposal the following objectives were set:

1. Use the existing mechanism for the shifting to higher data rates.
2. Provide full compatibility to the IEEE 802.11-1997 standard in addition to the higher data rate.
3. Ensure that customers will have a reasonable upgrade path to move to the higher data rates while continuing to utilize the existing products.
4. Utilize the same bandwidth as existing systems.

The implementation that was developed is consistent with the rate shifting mechanism defined in the current DSSS standard. The physical layer implementation proposed uses the existing preamble and header for acquisition and synchronization. The modem acquires the carrier using the 1 Mbps DBPSK synchronization pattern and start of field delimiter (SFD). As with the current standard the header is also transmitted using the 1 Mbps modulation. The service field in the header will specify the data rate to be used for the MAC Protocol Data Unit (MDPU). The demodulator will detect the data rate specified in the SIGNAL field. The field will define four possible rates: 1, 2 ,5.5 and 11 Mbps. Based on the value in the SIGNAL the modem will automatically switch to the selected data rate beginning with the first bit of the data unit. In addition to the SIGNAL field the 1 Mbps header includes the LENGTH field. Since this approach transmits these field at the 1 Mbps rate existing 802.11 radios will be able to receive and interpret this field.

***7.3** Advantages of the Proposed Approach*

7.3.1 Minimal Cost Impacts

The implementation developed by Harris for the high rate waveform is comparable in cost to the existing 802.11 design. Since the transmitted bandwidth is identical the RF and IF components are not changed from the existing design. The cost for a baseband processor implementing both high and low data rate signals is within 10 % of the original 802.11 baseband processor. There is no reason to believe that vendors designing their own baseband processor will not get the same result.

7.3.2 Minimal MAC Changes

This approach uses the mechanisms defined in the IEEE 802.11-1997 release to implement rate switching. Few, if any, changes are required in the MAC software to implement the high data rate system.

7.3.3 System Upgrade Path

As customers adopt 1 and 2 Mbps WLANs they will want to be certain that their investment is protected as they move to higher data rates. With this proposed physical implementation the high speed adapters can be installed in the same Basic Service Sets served by the current products. The use of the compatible header supports many of the mechanisms included in the standard for network coordination to minimize the impacts of having collocated high and low data rate systems.

7.3.4 Clear Channel Assessment

In order to support the CSMA/CA access method adapters must be able to detect transmissions from other network nodes. Since the DSSS systems can operate near the noise floor the energy detection CCA mode can be unreliable. By providing a common modulation for the low and high rate headers the Carrier Sense mode can operate for both high and low speed devices.

7.3.5 Reduced Collision Rate

By transmitting the header fields at 1 Mbps the low rate stations can read the duration field. This provides them with the back-off time to defer collisions in the next contention period. The random back-offs will start at the end of the high speed data packet. This is important to dealing with the near/far problem.

7.3.6 Historical Perspective

The impacts to the data throughput are significant, however there are examples in communications and computer standards where performance impacts are tolerated in order to maintain backward compatibility. In the development of new modem standards up to 56 Kbps the acquisition mode supports all data rates down to 300 bps. In the PC arena both the microprocessors and the operating system have maintained some degree of backward compatibility at the expense of performance.
There is also precedence for maintaining backward compatibility to facilitate customer upgrade paths. Many of the new 100 Mbps Ethernet cards include support for the original 10 Mbps standard. This permits MIS managers to provide the capability to upgrade when purchasing Network Interface Cards (NIC) for an existing 10 Mbps network.

7.4 Drawbacks of the Proposed Approach

7.4.1 Data Throughput

The effect of the use of 1 Mbps headers is documented in IEEE 802.11-97/78a. The approach proposed here follows the curves for the Modified Compatibility method of operation. The Acknowledge control frames are transmitted at the 11 Mbps data rate. There is a decrease in the available throughput due to the time to transmit the preamble and header at the 1 Mbps rate. The reduction in throughput relative to an approach that does acquisition, synchronization and control using 10 Mbps fields varies with the packet length. Since the data packet is transmitted at 11 Mbps the longer the data portion of the packet the smaller percentage of time used by the 1 Mbps portion of the packet. To minimize the impacts to throughput the largest practical packet size should be used.

7.4.2 FH Compatibility

The signaling used for the proposed approach is a variation of DSSS. As such the modem does not process FH signals. Also the transmitted waveform will not be detected by FH systems using carrier sense.

7.5 Impacts of a Non-Compatible Approach

The development of the 802.11 MAC included mechanisms to handle the problems associated with hidden nodes. The RTS/CTS exchange permits those stations that can hear the access point (AP) but not the station to receive the duration of the stations transmission time. This time permits the other station to know the amount of time to defer before doing Clear Channel Assessment and random back-off if needed. If a PHY standard is adopted that does not able to receive and interpret the duration fields that define the Network Allocation Vector (NAV) then it will not participate in the virtual carrier sense mechanism. In situations as shown in figure 7.1 the incompatible high speed station will corrupt the low speed stations transmission since it will sense the channel is available. Figure 7.2 illustrates the timing of transmissions for the source low speed station, other low speed stations and incompatible high speed stations.

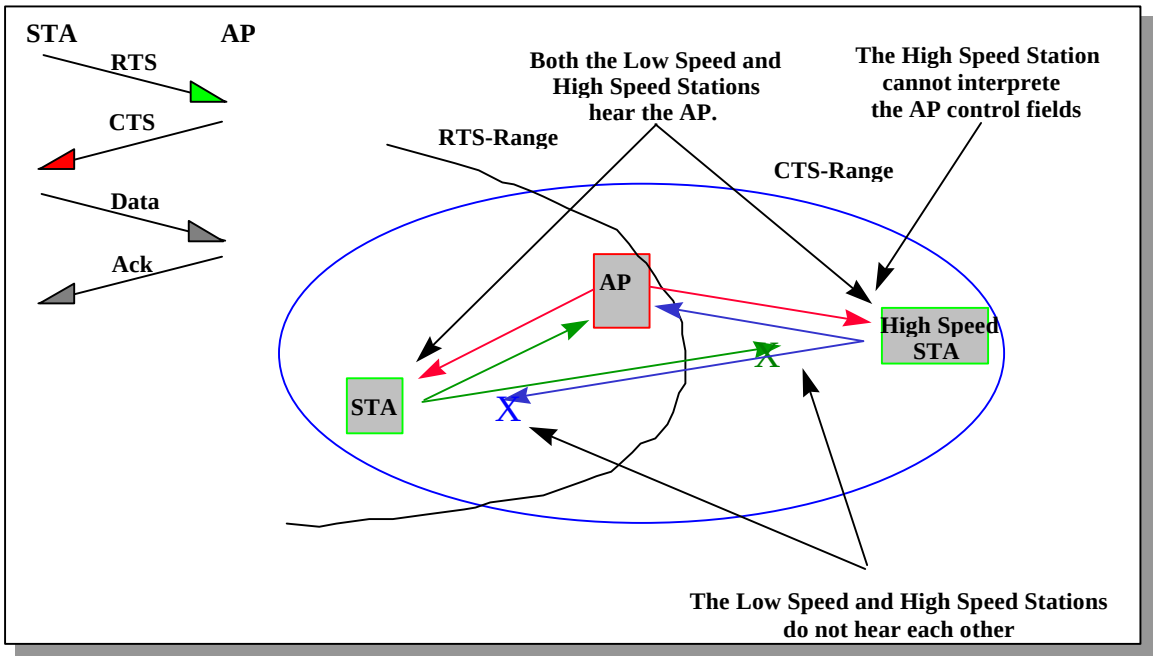


Figure 7.1

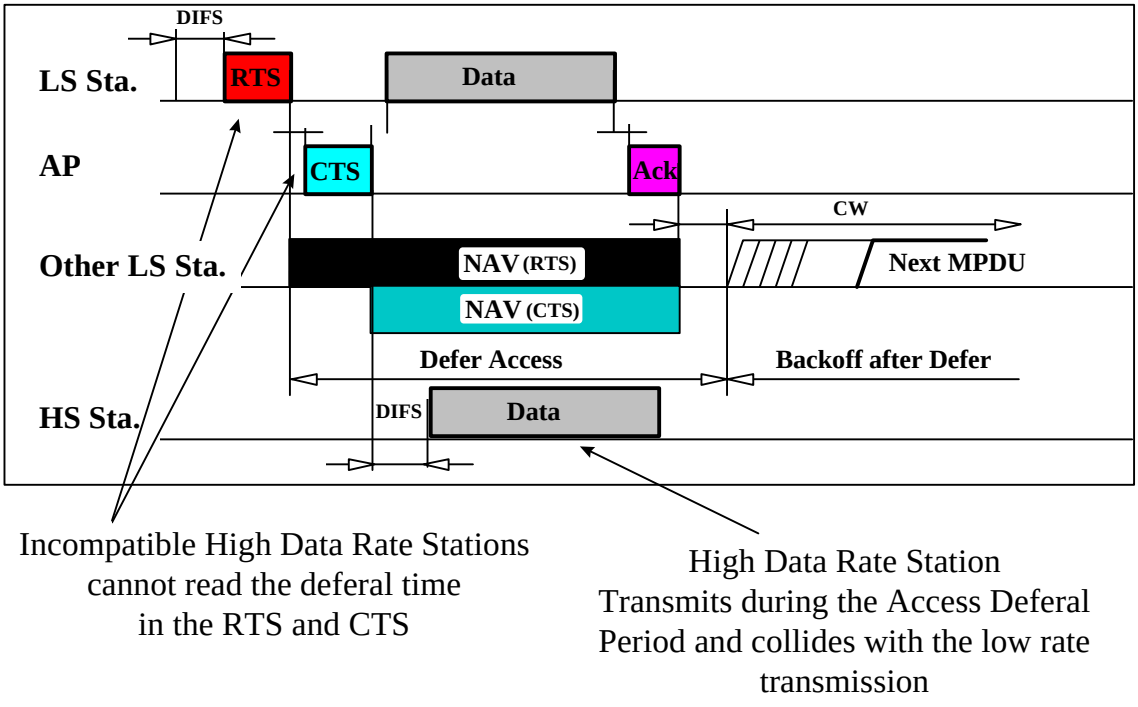


Figure 7.2

By using a PHY implementation that includes the current header fields the high speed station can interpret the duration field and implement the additional deferral time. The high speed station can also supply the duration field to low speed stations so that can implement the same deferral mechanism.

8. Implementation

This note will detail the RF and analog design of the PRISM™ 11Mbps PC Card Wireless LAN card. Figure 1 shows a block diagram of the 11Mbps radio design. This Direct Sequence Spread Spectrum (DSSS) radio has been designed to provide data rates of 1, 2, 5.5, and 11Mbps. The 5.5 and 11Mbps waveforms are interoperable with the existing IEEE 802.11 specification for DS 1 and 2Mbps data rates and FCC rules that cover the operation at 2.4GHz for DSSS modulation.

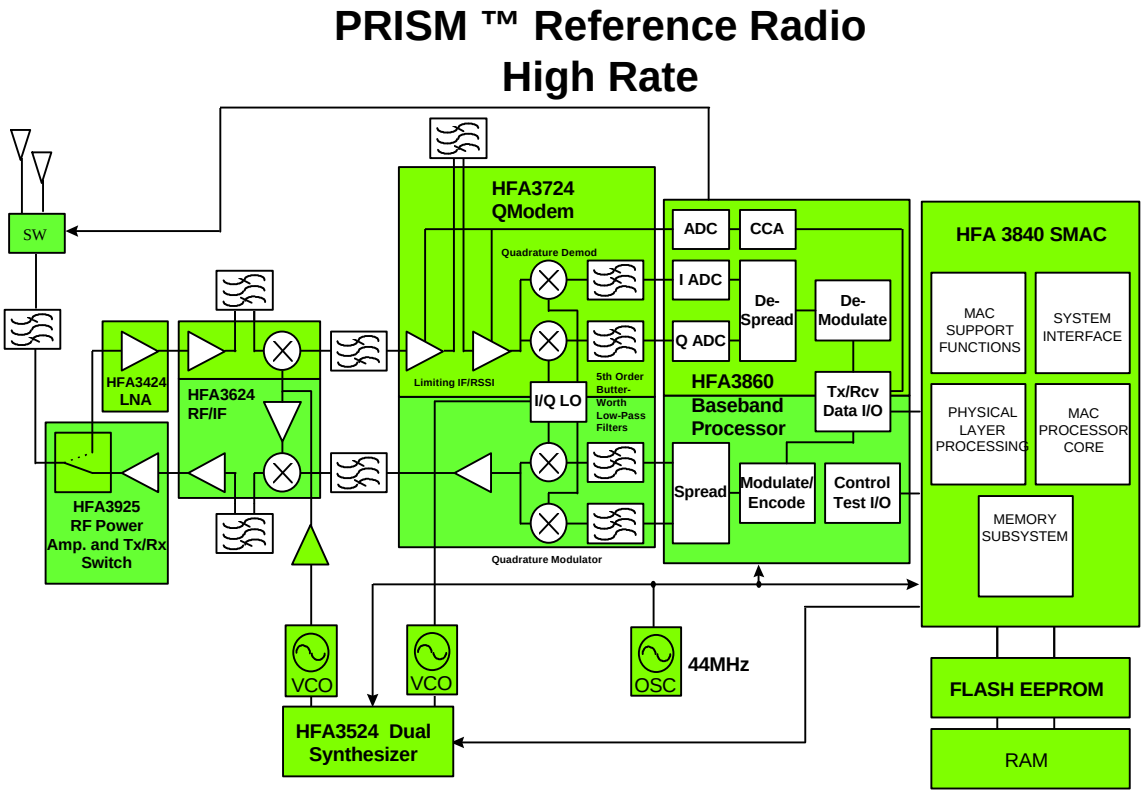


FIGURE 1. PRISM™ 11Mbps PC Card Block Diagram

The specifications of the PC Card Wireless LAN are as follows:

General Specifications

Targeted Standard	IEEE 802.11 Interoperable
Data Rate	1 Mbps DBPSK 2 Mbps DQPSK 5.5Mbps BMBOK

	11Mbps QMBOK
Frequency Range	2412MHz to 2484MHz
Step Size	1MHz
IF Frequency	280MHz
IF Bandwidth	17MHz
RX/TX Switching Speed	2us (Typ)
Operating Voltage	4.5VDC - 5.5VDC
Operating Current	290mA (w/o pwr saving)(Note 1) 60mA (w pwr saving)(Note 2)
Standby Current	190mA at 1us Recovery (Note 3) 70mA at 550us Recovery (Note 3) 60mA at 2ms Recovery (Note 3) 30mA at 5ms Recovery (Note 3)
Operating Temperature Range	0oC to 70oC
Storage Temperature Range	-55oC to 125oC
Mechanical	Type II PCMCIA Card with Antenna Extension
Antenna Interface	SMA, 50 ohm

Receive Specifications

Sensitivity	-93dBm (Typ), 1 Mbps, 8E-2 FER (Note 4) -90dBm (Typ), 2 Mbps, 8E-2 FER (Note 4) -87dBm (Typ), 5.5Mbps, 8E-2 FER (Note 4) -84dBm (Typ), 11Mbps, 8E-2 FER (Note 4)
Input Third Order Intercept Point	-17dBm (Typ)
Image Rejection	80dB (Typ)
IF Rejection	80dB (Typ)
Adjacent Channel Rejection	35dB (Min) at 25MHz Offset
Supply Current	287mA (Typ), 11Mbps

Transmit Specifications

Output Power	+18dBm (Typ)
Transmit Spectral Mask	-32dBc (Typ) at First Side-Lobe
Supply Current	488mA (Typ), 11Mbps , 100% Duty Cycle
Notes: 1. 2% transmit, 98% receive without power savings mode. 2. 2% transmit, 8% receive, 90% standby with power savings mode	

3. Recovery times do not include MAC recovery. Refer to Application Note “PRISMTM Power

Management Modes” AN9665.

4. FER = Frame Error Rate or Packet Error Rate

Receive Processing

Referring to the block diagram in Figure 1, the schematic in Appendix A, and the bill of materials in Appendix B, a single antenna is used. Up to two antennas are supported in the HFA3860 [1] Baseband Processor to implement diversity, countering the adverse effects of multi-path fading. As space is at a premium in a PCMCIA Card environment, only one antenna is used. In an actual system implementation, if one can achieve diversity in at least one end of a link, such as at the access point where it is possible to achieve physical separation between diversity antennas, multipath performance will be improved.

From the antenna, the received input is applied to FL1, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

The T/R switch is integrated in the HFA3925 [2] RF Power Amplifier (RFPA). The HFA3925 RFPA operates from the unregulated 5V PC Card supply.

Following the T/R switch, the HFA3424 [3] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5V supply. A logic-level PMOS switch, RF1K49093 [7], is used to control the drain supply voltage to the HFA3424 LNA, and implement a power down mode when transmitting.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISM™ radio, an attenuator follows the HFA3424 LNA. The attenuation chosen is 5dB. To improve noise figure, this attenuation may be reduced; alternatively, to improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure, input intercept point, and gain distribution analysis is shown in Table 1.

Next, the signal enters the HFA3624 [4] RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5V supply.

Down-conversion from the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz, and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50 ohm environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broad-band matching network is described in the HFA3624 RF/IF Converter Application Note [5], and does not require any tunable elements. A direct impedance match to the IF filter, FL3 could be implemented if desired. The 50 ohm environment was chosen to allow ease in measurement of portions of the radio with external test equipment. An analysis of the mixer spurious responses is shown in Appendix C. There are no crossing spurious responses, therefore only tuned responses are shown.

The IF receive filter, FL3, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280MHz, the 3dB bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270 ohm, and a series 33nH inductor is used to match the filter input to 50 ohm. The SAW output is matched directly to the IF input of the HFA3726 [6] Quadrature IF

Modulator/Demodulator, using a shunt 56nH inductor. This presents a 250 ohm source impedance to the limiter input, thereby optimizing the limiter's NF. Measured performance of the SAW filter is shown in Appendix D.

In the receive mode, the HFA3726 Quadrature IF Modulator/ Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3726 operate from a regulated 3.5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter, FL4, is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor, as described in the HFA3726 data sheet.

An additional limiter filter FL4A was added for the 11M bit data rate application at the output of the second limiter. This filter is needed to shape the hard limited, clipped, limiter 2 output into a more sinusoidal waveshape to restore phase and amplitude balance of the data vectors. This filter is a low pass with gain peaking at 280MHz.

The gain distribution/limiter noise analysis is shown in Appendix G. If the alternative HFA3624 broadband matching network is used, the HFA3624 mixer conversion gain will be higher, which will help ensure that the second limiter is fully limited on front-end noise.

At the output of the limiters, a $200mV_{P-P}$ differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3726 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 560MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally $500mV_{P-P}$ single-ended, and are intended to be AC coupled to the HFA3860 Baseband Processor. The AC coupling time constant for 11Mbps QMBOK must be longer than that required for 2Mbps QPSK modulation due to more low frequency content and is implemented with 0.22uF series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HFA3860 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The sample rate is 44MSPS, which results in four samples per chip. A 44MHz Fox F4106 crystal oscillator is used to provide the main clock for the HFA3860. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an optional active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HFA3860 Baseband Processor correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, BMBOK, or QMBOK symbols. The demodulator includes a frequency tracking loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes (where appropriate) and descrambles the data. The data is output through the RX Port to the external processor.

The PRISMTM baseband processor, HFA3860 uses differential demodulation for the initial acquisition portion of the DBPSK header and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The part then uses time invariant correlation to strip the PN spreading and phase processing to demodulate the resulting signals in the header and DBPSK/DQPSK demodulation modes.

In the 1Mbps DBPSK mode, data demodulation is performed the same as in header processing. In the 2Mbps DQPSK mode the demodulator demodulates two bits per symbol and differentially decodes these bit pairs. The bits are then serialized and descrambled prior to being sent to the output.

In the MBOK modes, the receiver uses a complex multiplier to remove carrier frequency offsets and a bank of serial correlators to detect the modulation. A biggest picker finds the largest correlator in the I and Q channels and determines the sign of those correlations. For this to happen, the demodulator must know absolute phase which is determined by referencing the data to the last bit of the header. Each symbol demodulated determines 1 or 2 nibbles of data. This is then serialized and descrambled before passing to the output.

In 1Mbps and 2Mbps modes the radio uses a spread spectrum signal with 10.4dB of processing gain (10 log (11 chip PN)), the signal to noise ratio (SNR) in the chip rate bandwidth is approximately 0dB when the demodulator is at 1E-5 bit error rate (BER) in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm in the BPSK mode of operation.

Since the 11Mbps QMBOK modulation carries 11 times as many bits as the 1Mbps DBPSK case, in the same bandwidth, the energy per bit is 11 times less. Therefore the 11Mbps mode requires 10.4dB (10log(11Mb/1Mb)) greater SNR (defined as ES/N0) for the same bit error rate. In addition, QMBOK modulation is slightly more efficient than DBPSK by approximately 1.6dB. This gives a SNR increase for 11Mbps QMBOK modulation of 8.8dB when the demodulator is at 1E-5 BER. This results in a typical sensitivity of -84dBm in the 11Mbps QMBOK mode and -87dBm for 5.5Mbps BMBOK mode.

The HFA3860 Baseband Processor provides decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send (RTS) packet to the other end of the link and receives a Clear to Send (CTS) packet. The MAC then formats the payload data packet (MPDU) by appending it to a preamble and header and sends it on to the HFA3860 Baseband Processor which clocks it in. The HFA3860 Baseband Processor scrambles the packet and applies the selected spread spectrum modulation.

The modulator can support data rates of 1, 2, 5.5 and 11Mbps. The data can be either DPSK modulated at 1 MSPS (Million Symbols Per Second) or MBOK modulated at 1.375 MSPS and utilizes a baseband quadrature signal with I and Q components for all modulation modes. The DPSK spreading uses an 11 chip Barker sequence that is clocked at 11MHz. While the MBOK modulation takes the scrambled data and partions it into nibbles (4 bits). For Binary MBOK modulation (5.5Mbps) one nibble is used per symbol and for Quaternary MBOK (11Mbps) two are used. The data is not differentially encoded, just scrambled, in these modes.

These are then output to the HFA3726 as CMOS logic signals. Following the RTS/CTS/MPDU is an acknowledge (ACK) packet by the receiving side of the link.

Transmit quadrature single-bit digital inputs are applied to the HFA3726 Quadrature IF Modulator/Demodulator from the HFA3860 Baseband Processor. These inputs are internally attenuated and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, using a 909 ohm fixed tuning resistor external to the HFA3726.

In the PC Card wireless LAN, the goal is to control the regrowth of the side-lobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3726. The baseband AC coupling is implemented with 0.1uF series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3726 is reactively matched to FL5, with a 250 ohm resistive load presented to the HFA3726. A shunt 27nH inductor, in parallel with a 316 ohm resistor, is used to provide this match, to negate the effects of board and component capacitance, and provide a DC return to V_{CC} to prevent saturation in the IF output stage of the HFA3726.

The output of FL5 is terminated in a 200 ohm potentiometer that is used for transmit gain control. A shunt 39nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the potentiometer. This potentiometer has it's center wiper connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately 3k ohm. By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the main lobe to side lobe ratio of the output PSK waveform, typically -32dBc to -35dBc, at an output power of +18dBm.

Up conversion to the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL6, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter amplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20dBm, as measured at the T/R switch output. This represents a back-off from 1dB compression of approximately 4.5dB. Transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off. Allowing for approximately 2dB of loss between the T/R switch output and the antenna connector results in a final output power of +18dBm.

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA [7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor. A base-emitter junction is used as part of the gate bias network to provide temperature compensation, and all three gates are driven from one source to reduce the impact of process variation on pinch-off voltage. The nominal quiescent drain bias currents are 20mA for stage one, 53mA for stage two, and 90mA for stage three.

A second logic-level PMOS switch, RF1K49093, is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. A 2N2222 NPN transistor is used to level shift the 3.5V logic level from the MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate. The T/R Vdd pin is connected to the three PA Vdd pins, and is powered down in the receive mode by the PMOS switch. In this manner the T/R control pin transfer characteristic is less dependent on it's voltage, with the receive state being valid for T/R control voltages as low as 3 volts. If the T/R VDD pin was connected to a supply in both transmit and receive modes, the T/R control voltage would have to be within a few hundred millivolts of the supply to obtain similar performance.

Following the T/R switch, FL1 is reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as providing additional suppression of the LO. As the loss of FL1 is approximately 2dB, the amount of transmit power available at the antenna is approximately +18dBm.

As the transmit chain is operated linearly, any gain flatness from the HFA3624 and HFA3925, as well as from FL6, FL7, and FL1, will result in the transmit output power varying across the operating channels. To reduce the amount of variability, three 1pF capacitors are used as coupling elements to provide a form of simple equalization. Care must be exercised to ensure that the filter rejection is still acceptable in meeting the requirements of FCC 15.247. If desired, more complicated equalization could be used to maintain an improved 50 ohm environment for all passband frequencies. Using the simple equalization, the transmit output varies approximately 2.5dB across the band.

Synthesizer Section

The dual frequency synthesizer section uses the HFA3524 [9] Synthesizer and two voltage controlled oscillators to provide a tunable 2132MHz to 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from the 44MHz Fox F4106 crystal oscillator. Isolation of the HFA3524 synthesizer 44MHz clock from the HFA3860 clock line is accomplished with a 560 ohm resistor and careful layout. Both feedback loops are fourth order (four poles in the transfer function) and were designed to have loop bandwidths of 10kHz, and phase margins of 50 degrees. The feedback loop analysis is included for both loops in Appendix E. Measured phase noise performance and calculated RMS phase jitter is included in Appendix F. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator is a Motorola KXN1332A VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming. A 2N2907 PNP transistor was used to implement this function, and the

MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3dBm. An active buffer using an additional HFA3424 is used to provide additional isolation between the VCO and the HFA3624 LO input.

The fixed 560MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524 Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will degrade the quadrature phase accuracy of the HFA3726. A transconductance network is used at the HFA3726 LO input to convert the second LO voltage into a current, as recommended in the HFA3726 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divide-by-two LO buffer output of the HFA3726 is disabled, as recommended in the HFA3726 data sheet.

Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5V operating point, as opposed to a 5V operating point. The 3.5V operating point was chosen specifically as the lowest voltage that would support the MAC controller.

The only components operating directly from the 5V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PCMCIA Card interface sections of the MAC controller.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator supplies voltage to the HFA3860 Baseband Processor and portions of the MAC, as well as the HFA3424 LNA and HFA3624 RF/IF Converter. A second regulator supplies voltage to the synthesizer. The third regulator supplies voltage to the HFA3726 Quadrature IF Modulator/Demodulator.

PCB Layout Guidelines

Although the actual PCB layout is proprietary, some of the techniques utilized are worthy of discussion [10]. As there are many RF, IF, analog, and digital circuits in close proximity, isolation is of prime concern. All RF and IF circuits utilize coplanar waveguide with ground transmission line techniques to allow for easy integration of varied line widths and component pin widths, and to provide a low dispersion, high isolation environment. A Radio Schematic is available on the Internet at http://www.semi.harris.com/prism/lanref.htm.

The outside two planes of each side of the PCB are dedicated to RF and IF signal processing, and form two pairs of coplanar waveguide with ground circuits. As the two sides of the PCB contain circuitry that must be isolated from each other, blind via techniques are used, and the only places that the two sides share common ground or signal connections are when signals are passed between them, mainly when LO1 and LO2 need to pass from the synthesizer side to the RF/IF transceiver side.

In general, the RF and IF circuit layouts need to be as short and direct as possible to avoid costly shielding. This is especially critical in the receive IF stages where spurious signal coupling can easily occur, resulting in poor sensitivity or high packet error rates.

Appendix A
Reference Radio Schematics

Note: Please contact any Harris representative to IEEE 802.11 for copies of the schematics.

8.1 Appendix B Reference Radio Bill Of Materials

TABLE1. PRISM™ REFERENCE RADIO BILL OF MATERIALS (VERSION 1.0, /4/98)

DESCRIPTION	VALUE	QTY	PART NUMBER	MANUFACTURER	REFERENCE DESIGNATOR
IC, RF Low Noise Amplifier	N/A	2	HFA3424IB96	Harris	U19, U24
IC, Synthesizer	N/A	1	HFA3524IA96	Harris	U22
IC, RF/IF Converter	N/A	1	HFA3624IA96	Harris	U4
IC, IF Qmodem	N/A	1	HFA3726IN	Harris	U1
IC, Baseband Processor	N/A	1	HFA3860VI	Harris	U6
IC, RF Power Amplifier	N/A	1	HFA3925IA96	Harris	AR1
IC, Charge Pump	N/A	1	ICL7660SIBA-T	Harris	U12
IC, MAC	N/A	1	TBD	TBD	U3
IC, FLASH RAM	N/A	1	AM29F010-55EC	AMD	U2
IC, SRAM	N/A	1	M5M5256CVP-55LL	Mitsubishi	U8
			KM62256CLTG-5L	Samsung	
IC, Voltage Regulator 3.5V	N/A	3	TK11235AMTL	Toko	U13, U16, U21
Transistor, NPN	N/A	1	BFR505	Philips	Q2
Transistor, NPN	N/A	2	MMBT2222ALT1	Motorola	Q3, Q5
Transistor, PNP	N/A	1	MMBT2907ALT1	Motorola	Q4
			SMBT29077A	Siemens	
Transistor, PMOSFET	N/A	2	RF1K4909396	Harris	U9, U25
Diode, Varactor	N/A	1	BBY51-E6327	Siemens	CR3
LED, Red	N/A	1	597-3401-407	Dialight	DS3
LED, Yellow	N/A	1	597-3111-407	Dialight	DS2
LED, Green	N/A	1	597-3311-407	Dialight	DS1
VCO, 2.1GHz	N/A	1	KXN1332A	Motorola	U18
Crystal Osc, 40MHz, 100 PPM	N/A	1	CXO-M-10N-40MHZ-100PPM	Statek	U10
Crystal Osc, 44MHz, 25 PPM	N/A	1	F4106-44MHz	Fox	U20, U23
			CXO-M10N22M-25PPM	Statek	
Crystal, 32.768kHz	N/A	1	CX-6V-SM2-32.768K-C/I	Statek	U11
Filter, RF 2.45GHz	N/A	2	TDF2A-2450T-10	Toko	FL3-4
Filter, RF 2.45GHz	N/A	2	LFJ30-03B2442BO84	Murata	FL1-2
Filter, IF 280MHz	N/A	2	TQS-432A-7R	Toyocom	U5, U7
Capacitor, 0402, NPO, 0.1pF	1pF	3	04025A1R0CAT*A	AVX	C59, C131, C137
Capacitor, 0603, NP0, 0.1pF	4.7pF	1	06035J4R7BAWTR	AVX	C116
Capacitor, 0402, NP0, 5%	4.7pF	1	04025A4R7CAT2A	AVX	C93
			C1005COG1H4R7CT	TDK	
Capacitor, 0402, NPO, 0.25pF	5pF	4	04025A5R0CAT*A	AVX	C67, C123, C144, C151
			C1005COG1H5R0CT	TDK	
Capacitor, 0402, NP0, 5%	5.6pF	3	04025A5R6CAT2A	AVX	C68, C78, C122
			C1005COG1H5R6CT	TDK	
Capacitor, 0402, NP0, 5%	10pF	1	04025A100CAT2A	AVX	C31
			C1005COG1H100CT	TDK	
Capacitor, 0402, NP0, 1%	15pF	2	04023A150FAT2A	AVX	C73, C77
			C1005COG1E150FT	TDK	
			NMC0402NPO150F25TR	NIC	

Capacitor, 0402, NP0, 1%	20pF	1	04023A200FAT2A	AVX	C62
			C1005COG1E200FT	TDK	
Capacitor, 0402, NP0, 5%	22pF	6	04025A220JAT2A	AVX	C23-24, C52, C69, C98, C143
			C1005COG1H220JT	TDK	
Capacitor, 0402, NP0, 5%	47pF	4	04025A470JAT2A	AVX	C13, C18, C28, C60
			C1005COG1H470JT	TDK	
Capacitor, 0402, NP0, 1%	100pF	5	04023A101FAT2A	AVX	C44, C49, C54, C61, C111
			NMC0402NPO101F025TR	NIC	
Capacitor, 0402, NP0, 5%	100pF	20	04025A101JAT2A	AVX	C6, C9, C11-12, C14-15, C22, C30, C43, C47-48, C65, C72, C90, C92, C100, C104, C109-110, C118
			C1005COG1H101JT	TDK	
Capacitor, 0402, X7R, 5%	500pF	2	04025C501JAT2A	AVX	C32, C154
			C1005XR7R1H501JT	TDK	
Capacitor, 0402, X7R, 10%	1000pF	14	04023C102KAT2A	AVX	C17, C19, C25, C33, C39, C50, C63-64, C75, C95, C113, C138, C140-141
			C1005X7R1C102KT	TDK	
Capacitor, 0402, X7R, 10%	1800pF	1	0402YC182JAT*A	AVX	C86
			C1005XR71C182JT	TDK	
Capacitor, 0402, X7R, 10%	2200pF	1	04025C222JA2TA	AVX	C142
			C1005X7R1H222JT	TDK	
Capacitor, 0402, X7R, 10%	5600pF	1	0402YC562JAT*A	AVX	C91
			C1005X7R1C562JT	TDK	
Capacitor, 0603,X7R,5%	0.01uF	1	06035C103JAT2A	AVX	C89
			C0603C103J5RAC	Kemet	
			GRM39X7R103J050AD	Murata	
Capacitor, 0402, X7R, 10%	0.01uF	16	04023C103KAT2A	AVX	C1-5, C7-8, C10, C16, C29, C35, C76, C94, C96, C147, C153
			C1005X7R1C103KT	TDK	
Capacitor, 0805, X7R, 10%	0.056uF	1	0805YC563JAT*A	AVX	C115
			C2012X7R1C563JT	TDK	
Capacitor, 0603, X7R, 10%	0.1uF	39	GRM39X7R104K016AD	Murata	C21, C26-27, C34, C36-38, C40-42, C45-46, C53, C55, C57-58, C66, C70-71, C74, C79-80, C82, C99, C101-102, C106, C119-121, C124-130, C132, C136

			0603YC104KAT2A	AVX	
			C0603C104K5RAC	Kemet	
Capacitor, 0805, X7R, 5%	0.1uF	1	08053C104JAT*A	AVX	C97
			C0805C104J5RAC	Kemet	
Capacitor, 3216L, Tantalum	4.7uF	6	TAJS475K6R3R	AVX	C51, C56, C83, C85, C133-134
			T491S475K006AS	Kemet	
Capacitor, 3528L, Tantalum	4.7uF	2	TAJT475K010R	AVX	C84, C135
Capacitor, 3528L, Tantalum	10uF	1	TAJT106K010R	AVX	C81
			ECS-T1AY106R	Panasonic	
			TMC1AA106MLRH	KOA	
Capacitor, Trimmer	2pF - 6pF	1	JZ060	Voltronics	C139
Inductor, 0603, 2%	10nH	1	L0603100GFWTR	AVX	L3
Inductor, 0603, 2%	12nH	1	L0603120GFWTR	AVX	L17
Inductor, 0603, 10%	12nH	2	LL1608-F12NK	Toko	L15, 16
Inductor, 0603, 10%	15nH	4	LL1608-F15NK	Toko	L7, L9, L14, L23
Inductor, 0603, 10%	33nH	1	LL1608-F33NK	Toko	L5
Inductor, 0805, 10%	47nH	2	LL2012-F47NK	Toko	L2, L6
Inductor, 0805, 10%	56nH	1	LL2012-F56NK	Toko	L4
Inductor, Ferrite Bead	N/A	7	NCB1206B320TR	NIC	L1, L8, L12, L19, L21-22, L24
Resistor, 0402	0 ohm	10	ERJ2GEJ0R00X	Panasonic	R7, R20, R48, R59-62, R68-70
			MCR01MZSJ0R00	Rohm	
Resistor, 0505, 1%	1 ohm	1	9C06031A1R0F	Philips	R3
Resistor, 0402, 5%	10 ohm	6	ERJ2GEJ100X	Panasonic	R39, R47, R49, R53, R66, R85
			MCR01MZSJ100	Rohm	
Resistor, 0402, 5%	16 ohm	2	ERJ2GEY160V	Panasonic	R55, R56
			MCR01MZSJ160	Rohm	
Resistor, 0402, 5%	56ohm	3	ERJ2GEJ560X	Pansonic	R23, R86-87
			MCR01MZSJ560	Rohm	
Resistor, 0402, 5%	68 ohm	1	ERJ2GEJ680X	Panasonic	R54
			MCR01MZSJ680	Rohm	
Resistor, 0402, 5%	75 ohm	1	ERJ2GEJ750X	Panasonic	R51
			MCR01MZSJ750	Rohm	
Resistor, 0402, 5%	100 ohm	4	ERJ2GEJ101X	Panasonic	R33, R45, R67, R78
			MCR01MZSJ101	Rohm	
Resistor, 0402, 5%	120 ohm	1	ERJ2GEJ121X	Panasonic	R36
			MCR01MZSJ121	Rohm	
Resistor, 0402, 5%	220 ohm	1	ERJ2GEJ221JX	Panasonic	R2
			MCR01MZSJ221	Rohm	
Resistor, 0402, 1%	261 ohm	1	ERJ2RKF2610X	Panasonic	R5
			MCR01MZSF2610	Rohm	
Resistor, 0603, 1%	316 ohm	1	ERJ3EKF3160V	Panasonic	R17
			MCR03EZHMF3160	Rohm	
Resistor, 0402, 5%	330 ohm	2	ERJ2GEJ331X	Panasonic	R21, R24
			MCR01MZSJ331	Rohm	
Resistor, 0805, 5%	330 ohm	1	ERJ6GEYJ331V	Panasonic	R32

			MCR10EZHMJX331	Rohm	
Resistor, 0402, 5%	430 ohm	1	ERJ2GEJ431X	Panasonic	R42
			MCR01MZSJ431	Rohm	
Resistor, 0402, 1%	499 ohm	1	ERJ2RKF4990X	Panasonic	R10
			MCR01MZSF4990	Rohm	
Resistor, 0402, 5%	510 ohm	1	9. ERJ2GEJ511X	Panasonic	R82
			MCR01MZSJ511	Rohm	
Resistor, 0402, 5%	560 ohm	1	ERJ2GEJ561X	Panasonic	R9
			MCR01MZSJ561	Rohm	
Resistor, 0603, 5%	680 ohm	2	ERJ3GSYJ681V	Panasonic	R58, R65
			MCR03EZHMJ681	Rohm	
Resistor, 0402, 1%	715 ohm	2	ERJ2RKF7150X	Panasonic	R43, R84
			MCR01MZFS7150	Rohm	
Resistor, 0402, 5%	750 ohm	2	ERJ2GEJ751X	Panasonic	R26, R52
			MCR01MZSJ751	Rohm	
Resistor, 0402, 1%	909 ohm	1	ERJ2RKF9090X	Panasonic	R34
			MCR01MZFS9090	Rohm	
Resistor, 0402, 5%	910 ohm	2	ERJ2GEJ911X	Panasonic	R31, R44
			MCR01HZSJ911	Rohm	
Resistor, 0402, 5%	1k ohm	1	ERJ2GEJ102X	Panasonic	R4
			MCR01MZSJ102	Rohm	
Resistor, 0402, 5%	1.5k ohm	1	ERJ2GEJ152X	Panasonic	R50
			MCR01MZSJ152	Rohm	
Resistor, 0402, 1%	3.01k ohm	2	ERJ2RKF3011X	Panasonic	R14, R25
			MCR01MZSF3011	Rohm	
Resistor, 0402, 5%	3.9k ohm	1	ERJ2GEJ392X	Panasonic	R13
			MCR01MZSJ392	Rohm	
Resistor, 0402, 5%	4.3k ohm	2	ERJ2GEJ432X	Panasonic	R63-64
			MCR01MZSJ432	Rohm	
Resistor, 0402, 5%	4.7k ohm	2	ERJ2GEJ472X	Pansonic	R38, R76
			MCR01MZSJ472	Rohm	
Resistor, 0402, 5%	8.2k ohm	2	ERJ2GEJ822X	Panasonic	R22, R35
			MCR01MZSJ822	Rohm	
Resistor, 0402, 5%	9.1k ohm	1	ERJ2GEJ912X	Panasonic	R1
			MCR01MZSJ912	Rohm	
Resistor, 0402, 5%	10k ohm	2	ERJ2GEJ103X	Panasonic	R37, R41
			MCR01MZSJ103	Rohm	
Resistor, 0402, 5%	15k ohm	2	ERJ2GEJ153X	Pansonic	R46, R77
			MCR01MZSJ153	Rohm	
Resistor, 0402, 5%	100k ohm	1	ERJ2GEJ104X	Panasonic	R27
			MCR01MZSJ104	Rohm	
Resistor, 0402, 5%	390k ohm	1	ERJ2GEJ394X	Panasonic	R79
			MCR01MZSJ394	Rohm	
Resistor, 0603, 10%	10M ohm	1	ERJ3GSYK106V	Panasonic	R57
			MCR03EZHUK106	Rohm	
Potentiometer, SMT	200 ohm	1	EVM1SSW00B22	Panasonic	R19
Potentiometer, SMT	1k ohm	1	EVM1SSW00B13	Panasonic	R75
Connector, PC Card	N/A	1	050-E51-0000-BPO	ITT Cannon	

Connector, SMA Jack	N/A	1	142-0701-235	EF Johnson	U15

Appendix C
Receive Mixer Spurious Analysis

SystemPlus 1.0 S/N 11158 Copyright (c) 1992-1993 Webb Laboratories All Rights Reserved
PRISM Reference Radio, 08/29/1996, 16:08:48
Receive Crossover Responses in Receive Band (2400MHz to 2500MHz)
LO Level = +7dBm

IF FREQ	LO FREO	RCV FREO	SPUR FREO	M	N	MXR

No spurs recorded.

PRISM Reference Radio, 08/29/1996, 16:08:50
Spurious Responses in 0MHz to 5000MHz Band (-90dBC Minimum)
LO Level = +7dBm
Fixed Bandpass Preselector
Band Edges are 2400MHz and 2500MHz
4 Section Butterworth - Corner Attenuation = 1dB
Ultimate Preselector Rejection = 80dB

IF FREO	LO FREC	RCV FREQ	SPUR FREQ	M	N	MXR	FLT	TOT
280.0000	2120.0000	2400.0000	2400.0000	+1	-1	0	1	1
280.0000	2120.0000	2400.0000	1840.0000	-1	+1	0	80	80
280.0000	2120.0000	2400.0000	2488.0000	-5	+6	90	0	90
280.0000	2120.0000	2400.0000	2426.6667	-6	+7	90	0	90
280.0000	2120.0000	2400.0000	2462.8571	+7	-8	90	0	90
280.0000	2130.0000	2410.0000	2410.0000	+1	-1	0	0	0
280.0000	2130.0000	2410.0000	1850.0000	-1	+1	0	80	80
280.0000	2130.0000	2410.0000	2438.3333	-6	+7	90	0	90
280.0000	2130.0000	2410.0000	2474.2857	+7	-8	90	0	90
280.0000	2140.0000	2420.0000	2420.0000	+1	-1	0	0	0
280.0000	2140.0000	2420.0000	1860.0000	-1	+1	0	80	80
280.0000	2140.0000	2420.0000	2450.0000	-6	+7	90	0	90
280.0000	2140.0000	2420.0000	2485.7143	+7	-8	90	0	90
280.0000	2140.0000	2420.0000	2405.7143	-7	+8	90	0	90
280.0000	2150.0000	2430.0000	2430.0000	+1	-1	0	0	0
280.0000	2150.0000	2430.0000	1870.0000	-1	+1	0	80	80
280.0000	2150.0000	2430.0000	2461.6667	-6	+7	90	0	90
280.0000	2150.0000	2430.0000	2417.1429	-7	+8	90	0	90
280.0000	2160.0000	2440.0000	2440.0000	+1	-1	0	0	0
280.0000	2160.0000	2440.0000	1880.0000	-1	+1	0	80	80
280.0000	2160.0000	2440.0000	2473.3333	-6	+7	90	0	90
280.0000	2160.0000	2440.0000	2428.5714	-7	+8	90	0	90
280.0000	2170.0000	2450.0000	2450.0000	+1	-1	0	0	0
280.0000	2170.0000	2450.0000	1890.0000	-1	+1	0	80	80

IF FREO	LO FREC	RCV FREQ	SPUR FREQ	M	N	MXR	FLT	TOT
280.0000	2170.0000	2450.0000	2485.0006	-6	+7	90	0	90
280.0000	2170.0000	2450.0000	2440.0000	-7	+8	90	0	90

280.0000	2180.0000	2460.0000	2460.0000	+1	-1	0	0	0
280.0000	2180.0000	2460.0000	1900.0000	-1	+1	0	80	80
280.0000	2180.0000	2460.0000	2273.3333	+3	-3	50	39	89
280.0000	2180.0000	2460.0000	2451.4286	-7	+8	90	0	90
280.0000	2190.0000	2470.0000	2470.0000	+1	-1	0	0	0
280.0000	2190.0000	2470.0000	1910.0000	-1	+1	0	80	`80
280.0000	2190.0000	2470.0000	2283.3333	+3	-3	50	37	87
280.0000	2190.0000	2470.0000	2462.8571	-7	+8	90	0	90
280.0000	2200.0000	2480.0000	2480.0000	+1	-1	0	0	0
280.0000	2200.0000	2480.0000	1920.0000	-1	+1	0	80	80
280.0000	2200.0000	2480.0000	2293.3333	+3	-3	50	35	85
280.0000	2200.0000	2480.0000	2474.2857	-7	+8	90	0	90
280.0000	2210.0000	2490.0000	2490.0000	+1	-1	0	0	0
280.0000	2210.0000	2490.0000	1930.0000	-1	+1	0	80	80
280.0000	2210.0000	2490.0000	2303.3333	+3	-3	50	32	82
280.0000	2210.0000	2490.0000	2485.7143	-7	+8	90	0	90
280.0000	2220.0000	2500.0000	2500.0000	+1	-1	0	1	1
280.0000	2220.0000	2500.0000	1940.0000	-1	+1	0	79	79
280.0000	2220.0000	2500.0000	2360.0000	+2	-2	74	15	89
280.0000	2220.0000	2500.0000	2313.3333	+3	-3	50	30	80

TABLE 1. RECEIVE SPUR TABLE – LO POWER = 7dBm

IF = |(MIIN) +/- (N*LO)|

(M)	(N) 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
15	99															
14	99	99														
13	90	99	90													
12	99	99	99	99												
11	90	99	90	95	90											
10	99	99	99	99	99	99										
9	90	95	90	90	90	99	90									
8	99	95	99	95	99	95	99	95								
7	90	90	90	90	90	87	90	90	90							
6	90	90	90	90	90	90	90	90	90	90						
5	90	80	90	71	90	68	90	65	88	65	85					
4	86	90	86	88	88	85	86	85	90	85	85	85				
3	67	64	69	50	77	47	74	44	74	47	75	44	70			
2	73	73	74	70	71	64	69	64	69	62	74	62	72	60		
1	24	0	35	13	40	24	45	28	49	33	53	42	60	47	63	
0	---	26	35	39	50	41	53	49	51	42	62	51	60	47	77	50

Appendix D
IF SAW Filter Measured Data

8.1.1.1 Toyocom TQS-432E-7R, VHF-Range Wideband Low Loss SAW Filter

SPECIFICATIONS (TENTATIVE)	
Reference Frequency (f_O):	280MHz
Passband:	fo ± 8.5MHz
Maximum Insertion Loss in Passband:	10dB Max
Attenuation:	fo ± 38.8MHz at 50dB
Terminating Impedance:	270 ohm //-5pF
Operating Temperature Range:	-10°C to 50°C
Package:	SS-752A

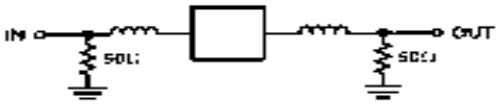


FIGURE 1.

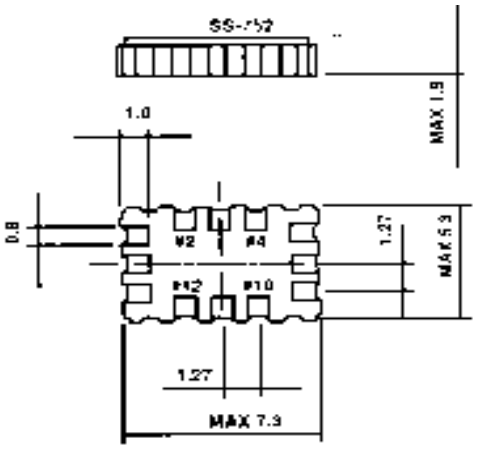


FIGURE 2.

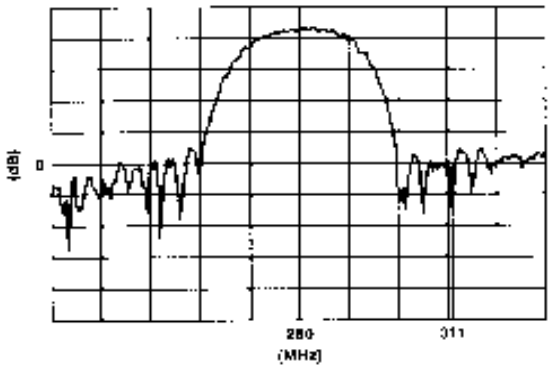


FIGURE 4

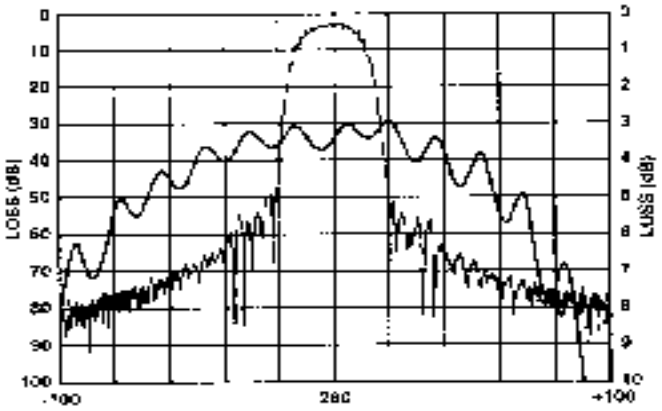


FIGURE 3.

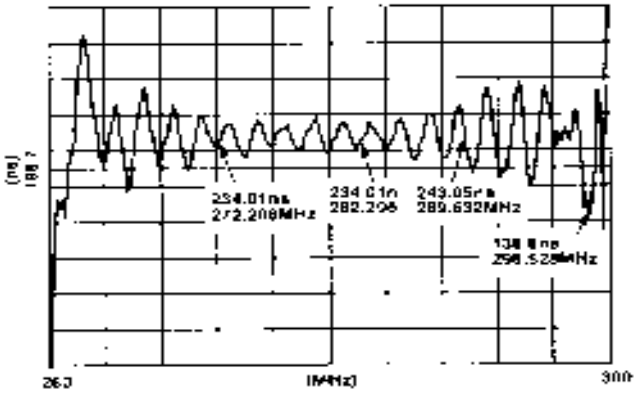


FIGURE 5.

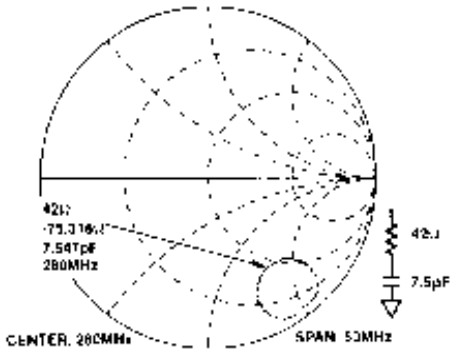


FIGURE 6.

Appendix E
Synthesizer Loop Analysis

A. Schaldenbrand and R.D. Schultz, 5/8/96

Where:

LO1, 2132MHz to 2204MHz,

floop is the desired bandwidth of the PLL, in Hz,

fref is the reference frequency of the loop, in Hz,

phi is the desired phase margin of the PLL, in degrees,

Kvco is the VCO Tuning Voltage Constant in Hz/V,

Kpd is the Phase Detector Pump Constant in A/rad,

N is the divider ratio,

1.424 is a constant to account for impact of R3/C3 pole.

$floop := 10 \cdot 10^{3}$ $wp := 2 \cdot \pi \cdot floop$ $wp = 6.283 \cdot 10^{4}$

$fref := 1 \cdot 10^{6}$ $wr := 2 \cdot \pi \cdot fref$ $wr = 6.283 \cdot 10^{6}$

$Kvco := 88 \cdot 10^{6}$ $Kvco := 2 \cdot \pi \cdot Kvco$ $Kvco = 5.529 \cdot 10^{8}$

$Kpd := 0.004$ $Kpd := \frac{Kpd}{2 \cdot \pi}$ $Kpd = 6.366 \cdot 10^{-4}$

$N := 2168$

$T3 := \frac{1}{10 \cdot wp}$ $wp := 1.424 \cdot wp$

$T1 := \frac{\sec(phr) - \tan(phr)}{wp}$ $T1 = 4.068 \cdot 10^{-6}$

$$wc := \frac{\tan(phr) \cdot (T1 + T3)}{[T1 + T3^{2} + T1 \cdot T3]} \cdot \left[\sqrt{1 + \left[\frac{(T1 + T3)^{2} + T1 \cdot T3}{(\tan(phr) \cdot (T1 + T3))^{2}}\right]} - 1\right]$$

$$T2 := \left[\frac{1}{wc^{2} \cdot (T1 + T3)}\right] \qquad fc := \frac{wc}{2 \cdot \pi}$$

$$C1 := \left(\frac{T1 \cdot Kpd \cdot Kvco}{N \cdot T2 \cdot wc^{2}}\right) \cdot \sqrt{\frac{1 + (wc \cdot T2)^{2}}{[[1 + (wc \cdot T1)^{2}] \cdot [1 + (wc \cdot T3)^{2}]]}}$$

$$C2 := C1 \cdot \left[\left(\frac{T2}{T1}\right) - 1\right]$$

$$R2 := \frac{T2}{C2}$$

$T1 = 4.068 \cdot 10^{-6}$

$T2 = 4.472 \cdot 10^{-5}$

$T3 = 1.592 \cdot 10^{-6}$

$fc = 1 \cdot 10^{4}$

$C1 = 1.075 \cdot 10^{-8}$ $C1 := 0.01 \cdot 10^{-6}$

$C2 = 1.075 \cdot 10^{-7}$ $C2 := 0.1 \cdot 10^{-6}$

$R2 = 416.209$ $R2 := 430$

Rules of thumb for selecting the values of the reference frequency suppression filter are:

1. Choose C3 < C1/10

$C3 := \frac{C1}{10}$ $R3 := \frac{T3}{C3}$

$R3 = 1.592 \cdot 10^{3}$ $C3 = 1 \cdot 10^{-9}$

2. Choose R3 < 2 • R2

$R3 := 2 \cdot R2$ $R3 = 860$ $R3 = 910$

$C3 := \frac{T3}{R3}$ $C3 = 1.749 \cdot 10^{-9}$ $C3 := 1800 \cdot 10^{-12}$

$k = 10..70$ $kp(k) := 10^{\left(\frac{k}{10}\right)}$

$\omega(k) := 2j \cdot \pi \cdot kp(k)$

$$GH(k) := Kpd \cdot Kvco \cdot \frac{1 + \omega(k) \cdot T2}{(C1 \cdot N \cdot \omega(k) \cdot \overline{\omega(k)}) \cdot (1 + \omega(k) \cdot T1)} \cdot \frac{T1}{T2} \cdot \left[\frac{1}{(1 + \omega(k) \cdot T3)}\right]$$

$MAGdb\_GH(k) := 20 \cdot \log(GH(k) \cdot \overline{GH(k)})$

$$PHI\_GH(k) := \operatorname{atan}\left(\frac{Im(GH(k))}{Re(GH(k))}\right)$$

$$f\_GH(k) := \left(\frac{180 \cdot PHI\_GH(k)}{\pi}\right) - 180$$

$MAG\_GH(k) := (GH(k) \cdot \overline{GH(k)})$ $Phim(k) := 180 + f\_GH(k)$

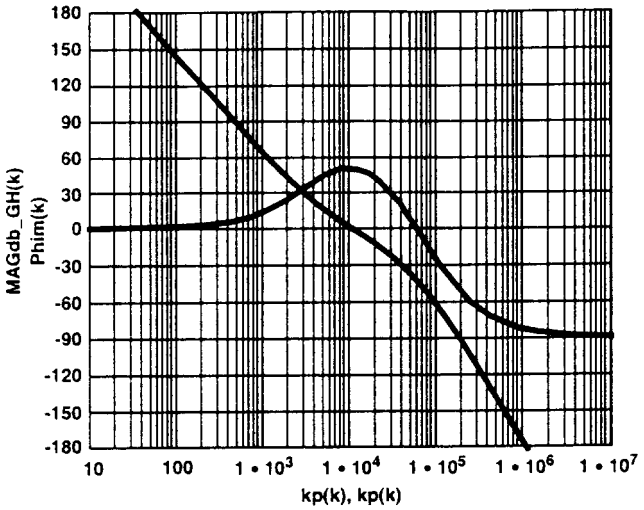


FIGURE 1.

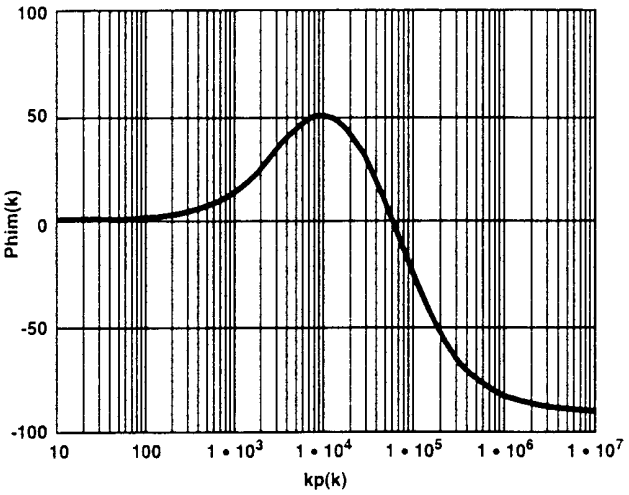


FIGURE 2.

This analysis calculates the loop filter components for the PRISM™ HFA3524 Dual PLL.

A. Schaldenbrand and R.D. Schultz, 5/8/96

Where:

LO2, 560MHz,

floop is the desired bandwidth of the PLL, in Hz,

fref is the reference frequency of the loop, in Hz,

phi is the desired phase margin of the PLL, in degrees,

Kvco is the VCO Tuning Voltage Constant in Hz/V,

Kpd is the Phase Detector Pump Constant in A/rad,

N is the divider ratio,

1.424 is a constant to account for impact of R3/C3 pole.

$floop := 10 \cdot 10^3$ $wp := 2 \cdot \pi \cdot floop$ $wp = 6.283 \cdot 10^4$

$fref := 1 \cdot 10^6$ $wr := 2 \cdot \pi \cdot fref$ $wr = 6.283 \cdot 10^6$

$$phr := \left(\pi \cdot \frac{phi}{180}\right)$$

$Kvco := 13 \cdot 10^6$ $Kvco := 2 \cdot \pi \cdot Kvco$ $Kvco = 8.168 \cdot 10^7$

$Kpd := 0.004$ $Kpd := \frac{Kpd}{2 \cdot \pi}$ $Kpd = 6.366 \cdot 10^{-4}$

$N := 560$

$$T3 := \frac{1}{10 \cdot wp} \qquad wp := 1.424 \cdot wp$$

$$T1 := \frac{\sec(phr) - \tan(phr)}{wp} \qquad T1 = 4.068 \cdot 10^{-6}$$

$$wc := \frac{\tan(phr) \cdot (T1 + T3)}{[T1 + T3^2 + T1 \cdot T3]} \cdot \left[\sqrt{1 + \left[\frac{(T1 + T3)^2 + T1 \cdot T3}{(\tan(phr) \cdot (T1 + T3))^2}\right]} - 1\right]$$

$$T2 := \left[\frac{1}{wc^2 \cdot (T1 + T3)}\right] \qquad fc := \frac{wc}{2 \cdot \pi}$$

$$C1 := \left(\frac{T1 \cdot Kpd \cdot Kvco}{N \cdot T2 \cdot wc^2}\right) \cdot \sqrt{\frac{1 + (wc \cdot T2)^2}{[[1 + (wc \cdot T1)^2] \cdot [1 + (wc \cdot T3)^2]]}}$$

$$C2 := C1 \cdot \left[\left(\frac{T2}{T1}\right) - 1\right]$$

$$R2 := \frac{T2}{C2}$$

Loop Filter Component Values

$T1 = 4.068 \cdot 10^{-6}$

$T2 = 4.472 \cdot 10^{-5}$

$T3 = 1.592 \cdot 10^{-6}$

$fc = 1 \cdot 10^4$

$C1 = 6.149 \cdot 10^{-9}$ $C1 := 5600 \cdot 10^{-12}$

$C2 = 6.146 \cdot 10^{-8}$ $C2 := 0.056 \cdot 10^{-6}$

$R2 = 727.746$ $R2 := 750$

Rules of thumb for selecting the values of the reference frequency suppression filter are:

1. Choose C3 < C1/10

$$C3 := \frac{C1}{10} \qquad R3 := \frac{T3}{C3}$$

$R3 = 2.842 \cdot 10^3$ $C3 = 5.6 \cdot 10^{-10}$

2. Choose R3 > 2 • R2

$R3 := 2 \cdot R2$ $R3 = 1.5 \cdot 10^{3}$ $R3 = 1500$

$C3 := \frac{T3}{R3}$ $C3 = 1.061 \cdot 10^{-9}$ $C3 := 1000 \cdot 10^{-12}$

$k = 10..70$ $kp(k) := 10^{\left(\frac{k}{10}\right)}$

$\omega(k) := 2j \cdot \pi \cdot kp(k)$

$$GH(k) := Kpd \cdot Kvco \cdot \frac{1 + \omega(k) \cdot T2}{(C1 \cdot N \cdot \omega(k) \cdot \overline{\omega(k)}) \cdot (1 + \omega(k) \cdot T1)} \cdot \frac{T1}{T2} \cdot \left[\frac{1}{(1 + \omega(k) \cdot T3)}\right]$$

$MAGdb\_GH(k) := 20 \cdot Log(GH(k) \cdot \overline{GH(k)})$

$PHI\_GH(k) := atan\left(\frac{Im(GH(k))}{Re(GH(k))}\right)$

$f\_GH(k) := \left(\frac{180 \cdot PHI\_GH(k)}{\pi}\right) - 180$

$MAG\_GH(k) := (GH(k) \cdot \overline{GH(k)})$ $Phim(k) := 180 + f\_GH(k)$

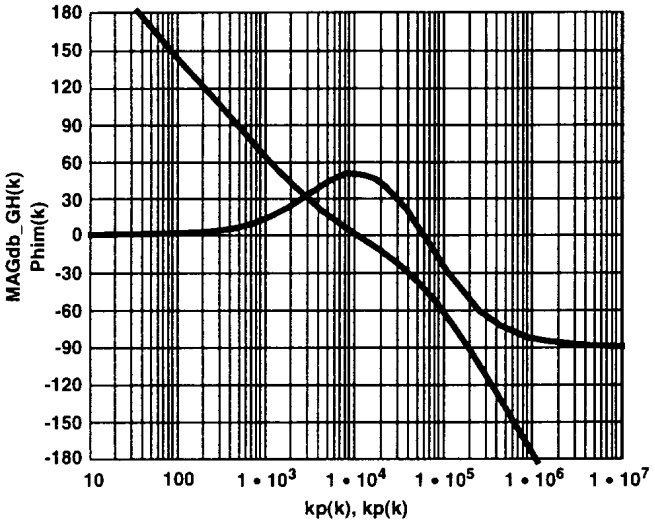


FIGURE 3.

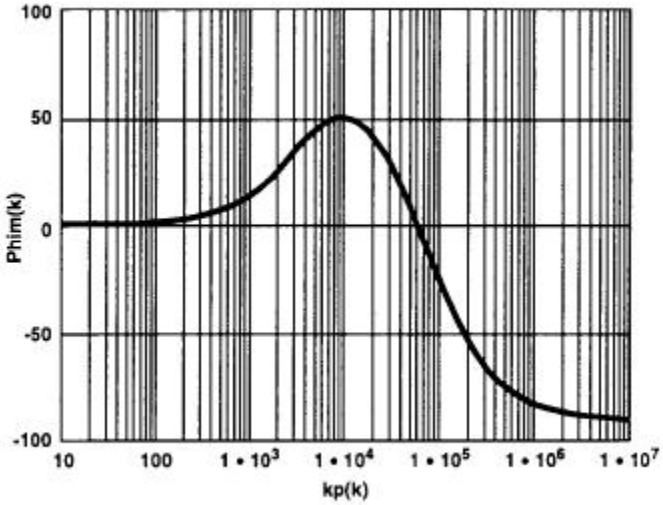


FIGURE 4.

Appendix F
Synthesizer Phase Noise/Jitter Analysis

8.1.1.1.1 TABLE 1. PRISM PHASE NOISE ANALYSIS

PRISM 1 LO PHASE NOISE ANALYSIS				
3/22/96 RDS				
2.1GHz LO MEASURED PERFORMANCE				
FREQ OFFSET	**dBc/Hz**	**NOTES**	**PHASE JITTER (RADIANS SQUARED)**	**PHASE JITTER (RMS DEGREES)**
10K	-76.6		2.382E-04	0.884
20K	-81.8		1.243E-04	0.639
50K	-92.4		8.781E-05	0.537
200K	-97.6		1.782E-05	0.242
300K	-103.7		5.511E-06	0.135
400K	-107.6		7.919E-06	0.161
750K	-111.2			
Total			4.816E-04	1.257
560MHz LO MEASURED PERFORMANCE				
10K	-83.5		4.051E-05	0.365
20K	-90.5		1.768E-05	0.241
50K	-102.1		3.865E-06	0.113
100K	-106		1.608E-05	0.230
>200K	-111			
Total			7.814E-05	0.506
"Assume worst case, RMS measured 2.1 GHz and 560MHz LO"				
			PHASE JITTER (RADIANS SQUARED)	**PHASE JITTER (RMS DEGREES)**
2.1GHz LO			4.816E-04	1.257
560MHz LO			7.814E-05	0.506
Total			5.597E-04	1.355

Appendix G
Gain Distribution/IF Limiting Analysis

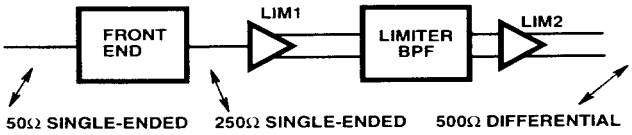


FIGURE 1.

The minimum limiter 1 voltage gain (SE to DIFF) is 39dB. The minimum limiter 2 voltage gain (DIFF to DIFF) is 45dB. The limiter 1/2 output limiting voltage is 200mV$_{P-P}$ into a differential 500? load. Using 3dB loss in the limiter BPF, the limiter 1, limiter BPF, limiter 2 cascaded voltage gain is 81dB (SE to DIFF). With a 200mV$_{P-P}$ output, the input limiting voltage is 17.8?V$_{P-P}$, or -98dBm at 250ohm source, or -91dBm at 50 ohm source. The above gain specifications are 25 C minimums, the typical gain/limiter is 6dB higher.

As the noise bandwidth of the limiters is over 500MHz, the cascaded limiters will be fully limited on their own noise if no limiter BPF is used (500MHz kTB is -87dBm, and the limiter NF is 7dB, resulting in an input noise power of -80dBm). Even if the limiter BPF is 20MHz, the cascaded limiters will be nearly limiting on their own noise (20MHz kTB is -101dBm, and the limiter NF is 7dB, resulting in an input noise power of -94dBm). Under the typical gain case the cascaded limiters would be fully limited. Only a modest increase in front end gain/NF is required to guarantee full limiting (4dB).

The front end 3dB bandwidth is approximately 17MHz, with an estimated noise bandwidth of 20MHz, as defined by the IF SAW filter. 20MHz kTB is -101dBm. If the limiter BPF was also 20MHz, the front end output noise floor would need to be 4dB in order to be limited in a 20MHz bandwidth. A 20MHz limiter BPF would require an additional SAW filter, or multi-pole tuned LC filter, and is therefore not cost effective or practical. The alternative chosen to implement is a simple one-pole LC BPF with a bandwidth wide enough such that variability in the fixed components used to not result in the filter being off frequency with respect to our desired 17MHz signal bandwidth. The filter chosen has a 3dB bandwidth of 50MHz, and an estimated noise bandwidth of 100MHz. Using this method, the front end gain must be increased to compensate for the excess limiter bandwidth.
In our system, we desire the second limiter to be fully limited on front end noise, as opposed to noise generated in the first limiter. This requires the front end output noise floor must be greater than the sum of the following: the limiter NF (7dB), the ratio of limiter BPF noise bandwidth to front end IF SAW noise bandwidth (10 log (100/20) or 7dB), and the amount of limiting margin (6dB for -1dB limiting). The front end output noise floor must therefore be greater than 20dB. The limiting margin was measured on from an HFA3724 device, with good agreement with a theoretical estimate based upon the hyperbolic tangent response of a bipolar differential limiter. The measurement means that if a non-desired jamming signal, noise in this case, is 6dB below the level of the desired signal, the desired output will be reduced 1dB.

As can be seen from Table 1, the front end output noise floor will be 17.2dB typically, resulting in a slight drop in baseband quadrature output voltage to the HFA3824 A/D converters when no signal is present, due to the excessive limiter bandwidth. The net impact to the system is a small reduction in sensitivity. If desired, additional front end gain could be used, or a different limiter BPF could be implemented with a reduced noise bandwidth.

References:

[1] HFA3860 AnswerFAX document # 4347, 407-724-7800. Available on Internet, Harris' home page is www.harris.com

[2] HFA3925 AnswerFAX document #4132, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[3] HFA3424 AnswerFAX document #4131, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[4] HFA3624 AnswerFAX document #4066, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[5] Application Note AN9618 "Using the PRISM™ HFA3624 Evaluation Board" AnswerFAX document #99618, 407-724-7800. Available on Internet, Harris' home page is www.harris.com

[6] HFA3726 AnswerFAX document #4310, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[7] ICL7660S AnswerFAX document #3179, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[8] RF1K49093 AnswerFAX document #3969, 407-724- 7800. Available on Internet, Harris' home page is www.harris.com.

[9] HFA3524 AnswerFAX document #4062, 407-724-7800. Available on Internet, Harris' home page is www.harris.com.

[10] "Integrating RF and Digital Circuits in a PC Card Environment", *Portable Design*, May 1996.