

Project: IEEE P802.15 Study Group for Wireless Personal Area Networks (WPANs)

Submission Title: PSSS proposal – Parallel reuse of 2.4 GHz PHY for the sub-1-GHz bands

Date Submitted: 12 September 2004

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Re: Proposal and Discussion of equal higher data rates for PHY for 900 and 2400MHz bands

Abstract: The proposed parallel reuse of the 2.4 GHz 802.15.4 modulation technology in PSSS offers highly attractive performance improvement, fulfilling all key OEM requirements, and visibly increasing market opportunities.

Purpose: Proposal for consideration by TG4b

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PSSS Proposal

Parallel reuse of 2.4 GHz PHY for the sub-1-GHz bands

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Presentation Contents

- Introduction
 - Changes vs. PSSS presentation at March 2003 meeting (Orlando)
 - Motivation and requirements for TG4b PHY
 - New Specifications for Low Bands
- PHY Performance
- PHY Technology
 - O-QPSK / I/Q and BPSK/ASK
- PHY Implementation aspects
 - Selected Rx implementation options
 - Crystal quality – frequency offset tolerance
 - Linearity
 - Chip size and power consumption
- Status
- PAR compliance
- Summary

Changes vs. PSSS presentation at March 2004 meeting (Orlando)

- **Unchanged proposal for parallel reuse of 2.4 GHz PHY!**
 - Added option of use of BPSK/ASK instead of O-QPSK
 - Based on OEM and semiconductor manufacturers requirements
 - To avoid added complexity and cost for two radio cores
 - To avoid doubling required bandwidth for O-QPSK
 - Added option to reduce 868 Mhz bandwidth to 500 Khz
 - Reduce implementation complexity and cost
 - Achieve still 234 kbit/s
 - Details of combining provided that were not shown in March 2004
 - Coding gain through simple precoding in combiner
- Added new results on PSSS
 - Solution performance
 - Implementation aspects
 - Status

Why do we want higher data rate

- Visibly over 200 kbit/s required especially in Europe (i.e. CEPT countries) due to 1% Tx duty cycle limit
 - Prohibits many application from using 868 MHz PHY today
 - Visibly 200 kbit/s would effectively turn limitation for devices into protection against interference from other applications
- Power consumption reduction (if done well)
- Reduced delay for packets
- Better performance and increased scalability for mesh networks
 - Removes today's functional limitations of 868/915 MHz meshes
- Marketing

What is important for the technical selection ?

- Data rate visibly higher than 200 kbit/s – in existing 868 MHz regulation
- Visibly better multipath fading robustness
- Backward compatible to 868/915 MHz PHY – must in IEEE802
- Small implementation, *low* cost – but not *lowest* cost

 *We believe it is key to listen to OEM requirements*

New Specifications for the Low Bands

- We can expect new frequency bands specifications for the sub-1-GHz ISM bands (868, 915 MHz) in Europe and Asia with increased RF bandwidth
 - However, it will take years until the changed SRD band specifications are implemented by all relevant CEPT countries
-
- Therefore 3 forms of *derivative modulations yielding higher data rates¹* are desirable:
 - Higher rate in 915 MHz band
 - Higher rate in existing European band
 - Higher rate in new, upcoming European 863-870 MHz band

1: Scope as defined in PAR

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PHY Performance

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System characteristics

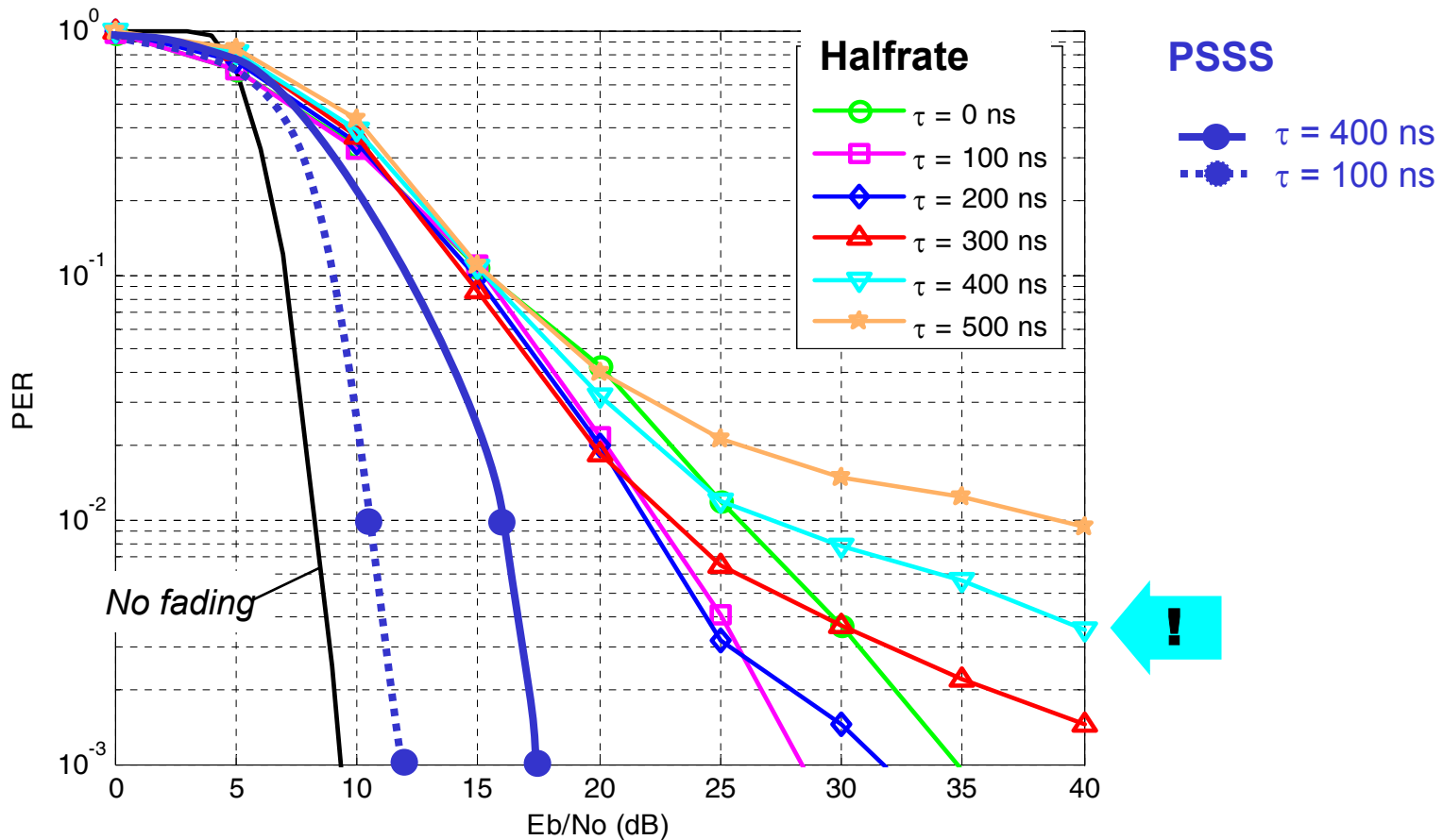
	IEEE 802.15.4-2003 868 / 915 MHz PHY	PSSS proposal – (March 2004: 8x parallel 2.4 GHz PHY in 868 / 915 MHz)	“Halfrate” proposal
Bandwidth	600 / 2000 Khz	600 (600) / 2000 (2000) kHz	2000 Khz
Chiprate	300 / 600 kcps	300 (500) ¹⁺² / 1000 (2000) ² kcps	1000 kcps
Bitrate	20 / 40 kbit/s	300 (234) ¹⁺² / 1000 (938) ² kbit/s	125 kbit/s
Spectral efficiency	1/15 bit/s/Hz	1/2 (15/32) bit/s/Hz	1/16 bit/s/Hz
Spreading	15 chip sequence	32 chip sequence	32 chip sequence
Channelization	1 / 10 channels	<i>unchanged, 1 / 10 channels</i>	<i>unchanged, 1 / 10 channels</i>
RF backward compatibility	BPSK	(Single BPSK/ASK radio) BPSK + O-QPSK / I/Q	Requires <i>duplicate</i> Rx + Tx cores for BPSK and O-QPSK
Synchronization, clock recovery	BPSK	(Single BPSK/ASK radio) BPSK + O-QPSK / I/Q	Required <i>twice</i> for BPSK and O-QPSK

“(…)” Proposed options of PSSS proposal – Changes are 1: Reduce EU signal bandwidth, 2: Use BPSK/ASK


System performance

	PSSS proposal	“Halfrate” proposal
Coding gain (vs. coherent BPSK, at 10^{-5} BER)	$\approx 1...3$ dB	≈ 1 dB
Target for MP fading robustness	Tolerates 1...2 μ s frequency selective multipath fading (coding immanent)	“> 100 ns” (Source: 01229r1, Motorola)
Loss in link budget due to MP fading (RMS 400ns) - 10^{-2} PER - 10^{-3} PER	$\approx -8...9$ dB $\approx -8...9$ dB	≈ -18 dB > 32 dB
MP fading range & Coverage	Range 2...4x better than Halfrate \rightarrow <i>Very small holes in coverage</i>	\rightarrow <i>Significant holes in coverage</i>
Practical Rx sensitivity (0.18 μ CMOS)	Better than -94 dB	

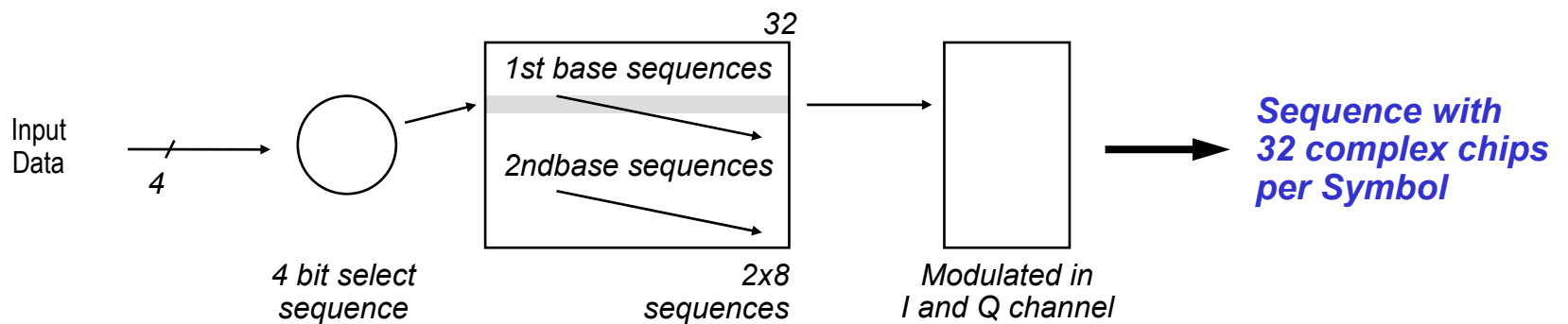
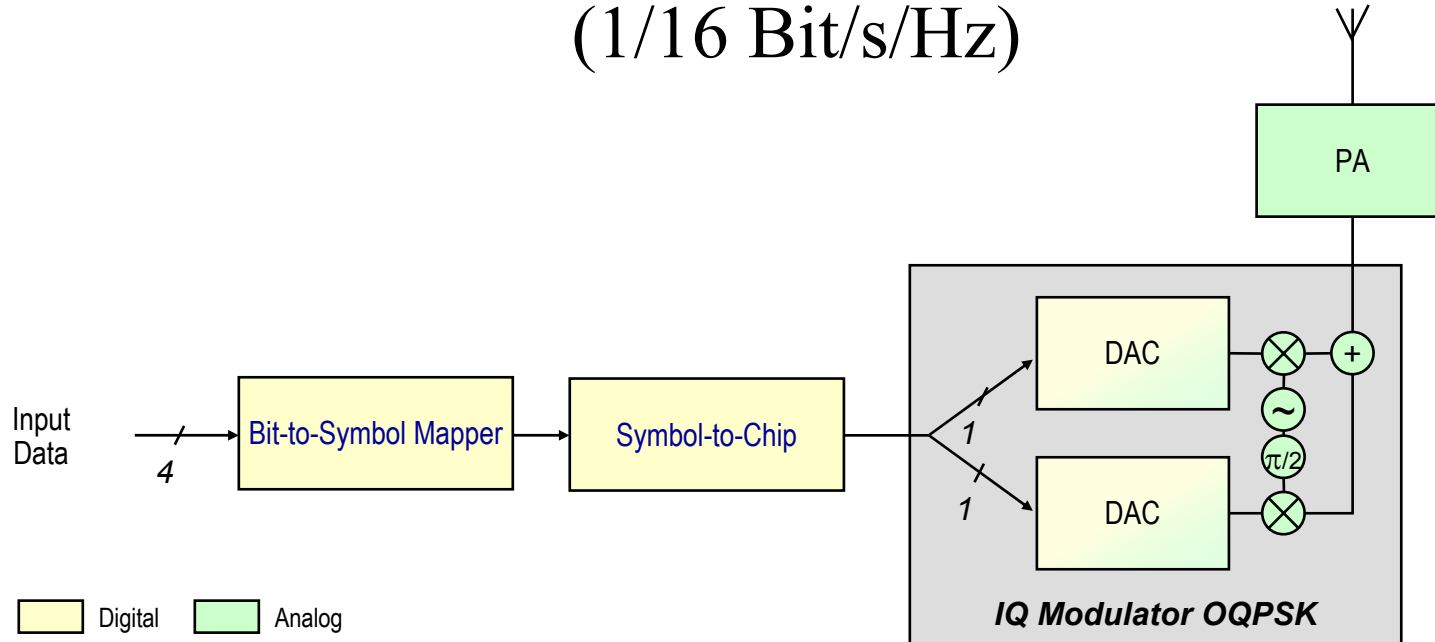
MP fading performance – Diffuse exponential model



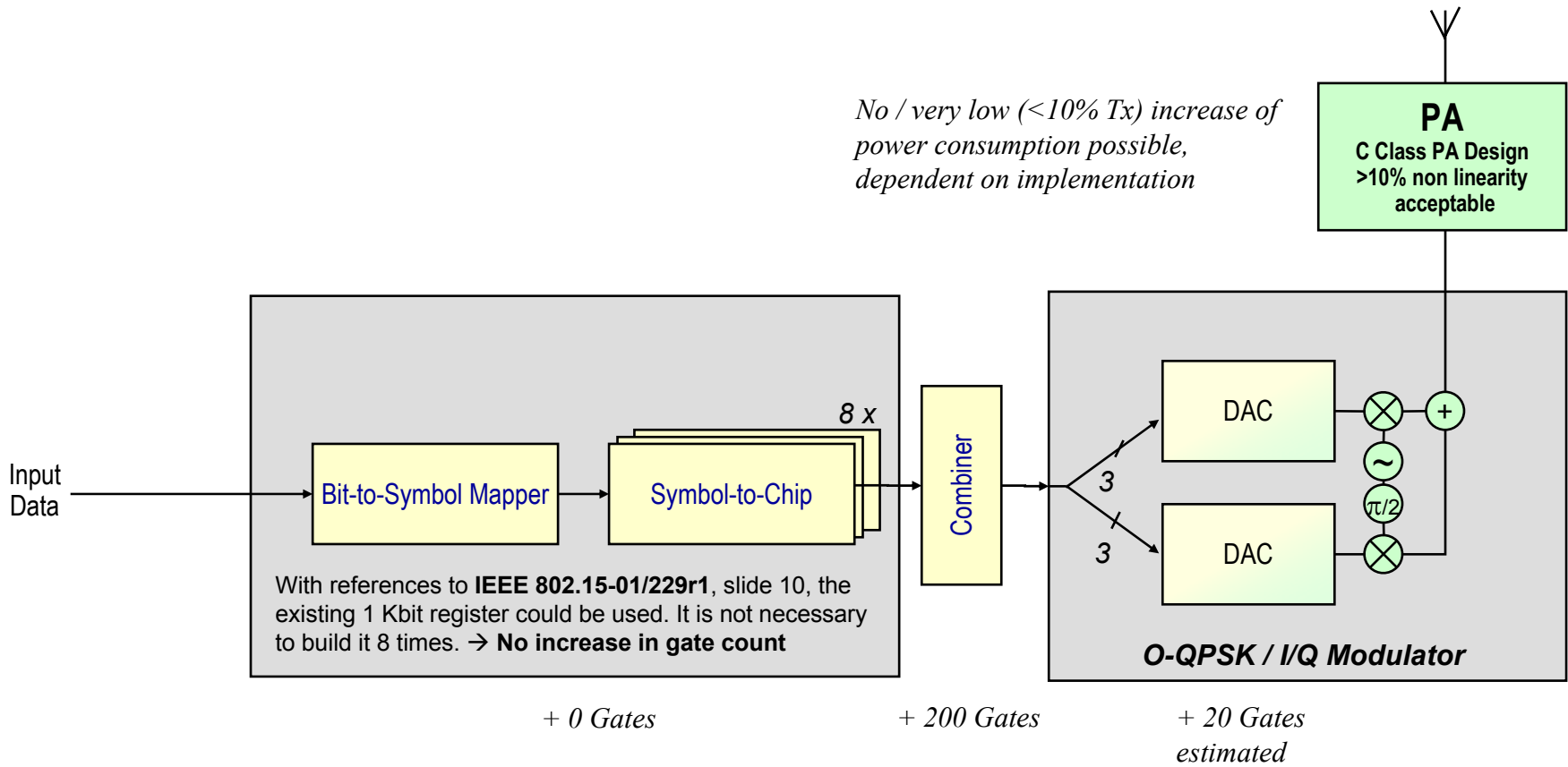
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Current 2.4 GHz / Halfrate PHY Tx architecture (1/16 Bit/s/Hz)

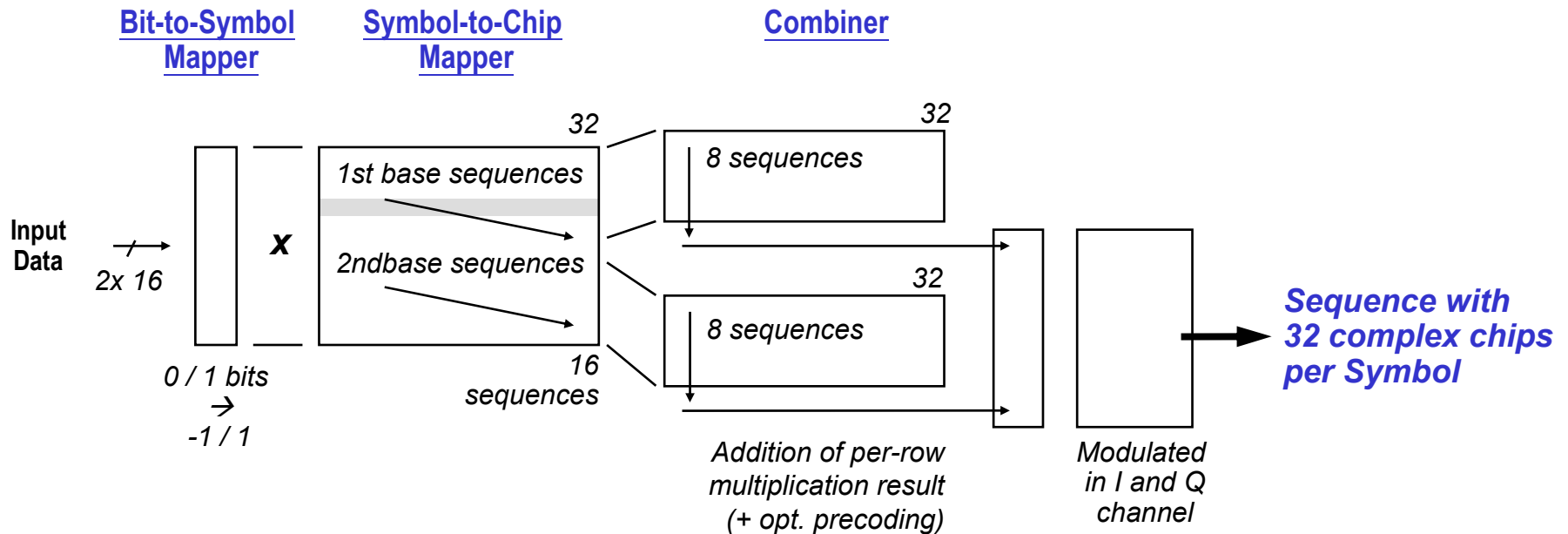


PSSS - 8 Times parallel 2.4 GHz PHY derivate – Tx - Original O-QPSK / I/Q proposal (1/2 bit/s/Hz)



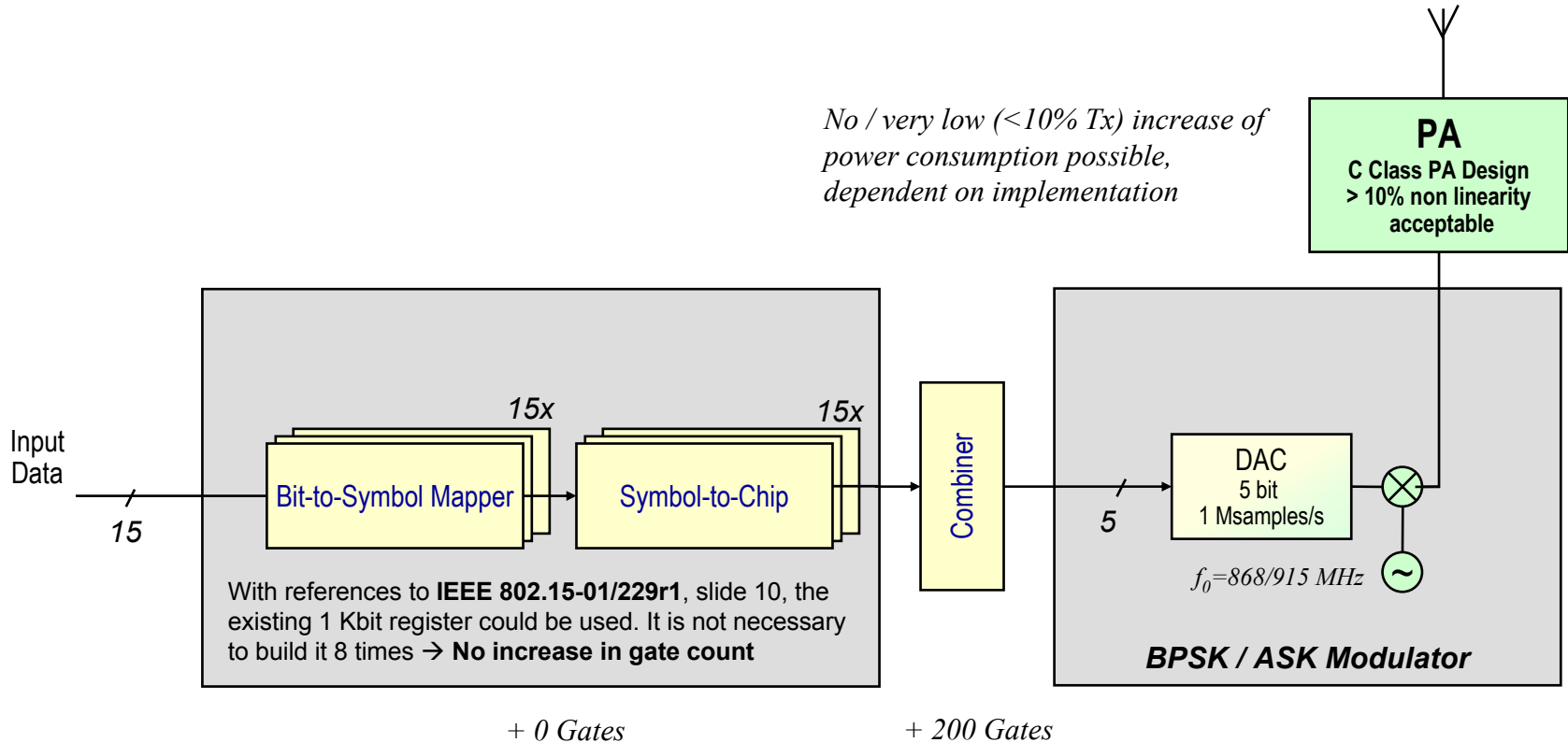
Digital
 Analog

PSSS - 8 Times parallel 2.4 GHz PHY derivate – Tx - Original O-QPSK / I/Q proposal (1/2 bit/s/Hz)



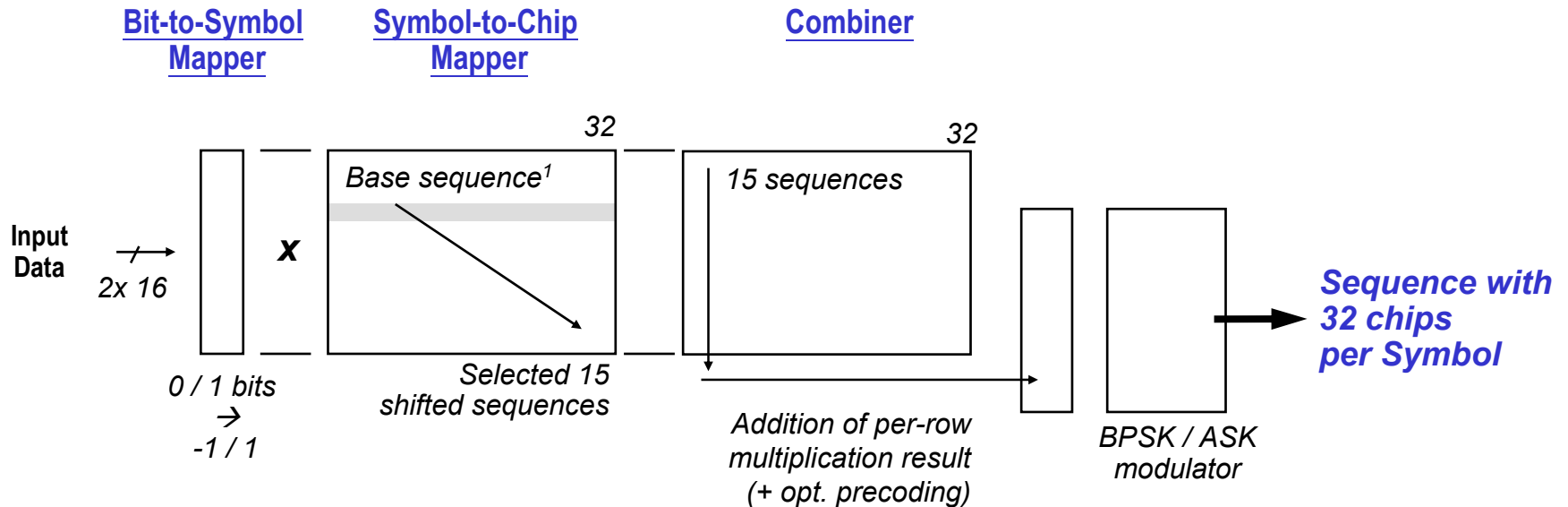
...addition of multiple parallel sequences instead of selection of single sequence

PSSS – Tx – BPSK/ASK option (15/32 bit/s/Hz)



Digital Analog

PSSS – Tx – BPSK/ASK option (15/32 bit/s/Hz)



...addition of multiple parallel sequences instead of selection of single sequence

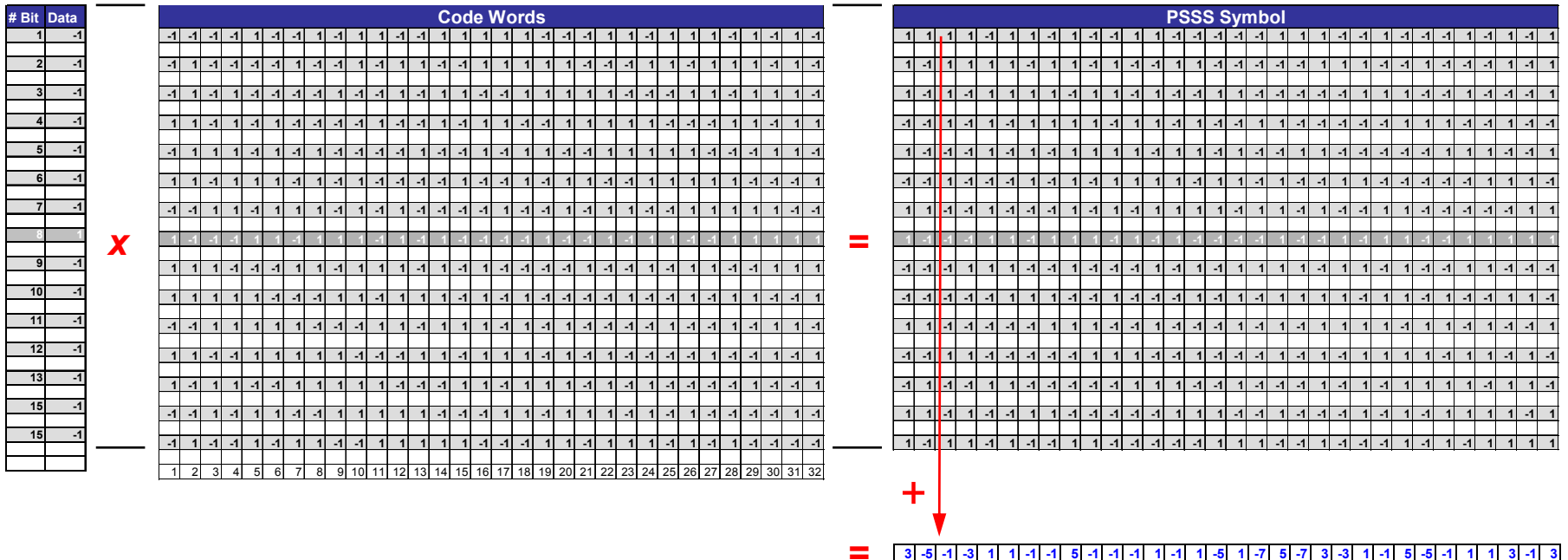
1: Use of single base sequence simplifies implementation in Rx

PSSS –BPSK/ASK option (15/32 bit/s/Hz) – Coding table

Symbol-to-Chip Mapper

# Bit	Chip Values																																				
1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	1	-1	1	-1		
2	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	
3	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	1	1	-1	-1	1	1	-1	1	1	1	-1	1	-1	
4	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	-1	1	1		
5	-1	1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	1	-1	-1	1	1	1	1	1	1	-1	-1	-1	1	1	-1	-1	1	1	-1	1	-1	
6	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	1	1	1	1	-1	-1	-1	1	1	
7	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	
8	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	1	1	
9	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	-1	1	1	-1	1	1	-1	-1	1	1	1	1	
10	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	-1	1	-1	-1	1	
11	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	1	-1	1	-1
12	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	-1	-1	1	-1	-1	1	-1	-1	1	-1	1
13	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1
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15	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	1	-1	1	-1	1	-1	-1	-1	-1	-1	-1
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32					

PSSS –BPSK/ASK option (15/32 bit/s/Hz) – Coding example



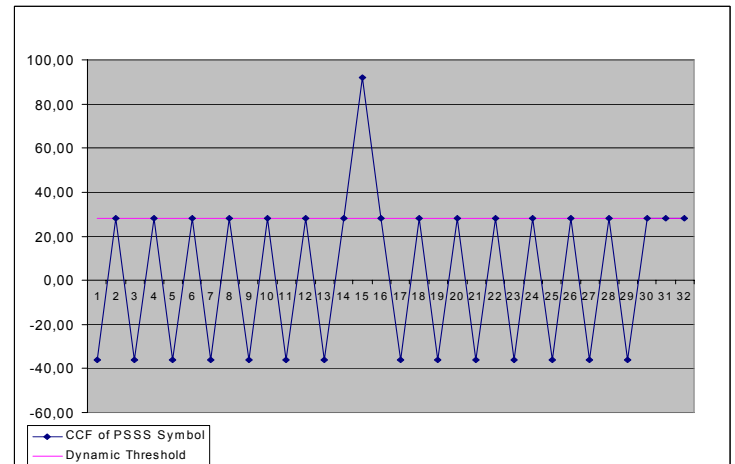
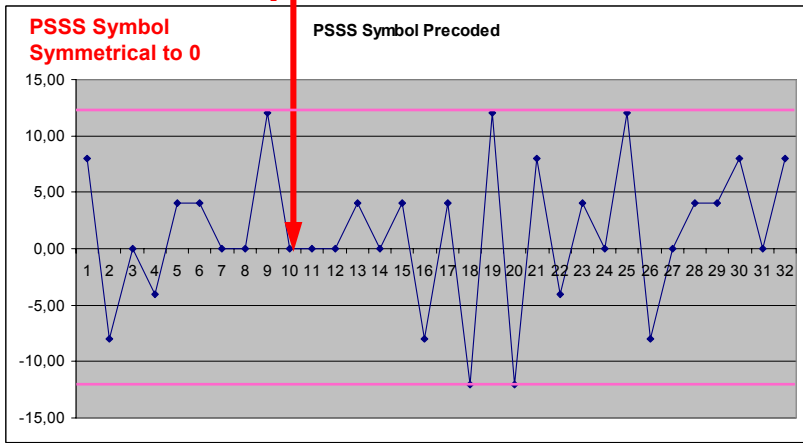
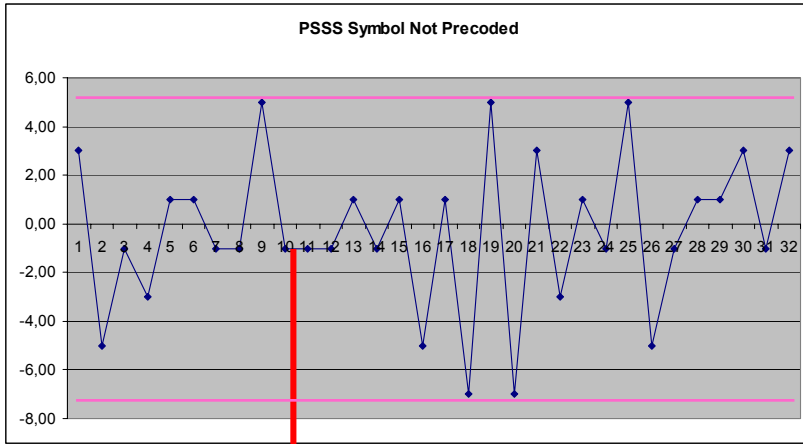
PSSS Symbol with 32 Chips

PSSS –BPSK/ASK option (15/32 bit/s/Hz) – Precoding

1. Align PSSS symbol maxima symmetrical to 0
2. Scale PSSS symbol to amplitude limit

Original signal resolution: 4 bit
Resolution after precoding: 5 bit


Note:
Higher resolution further improves performance, but does not limit interoperability



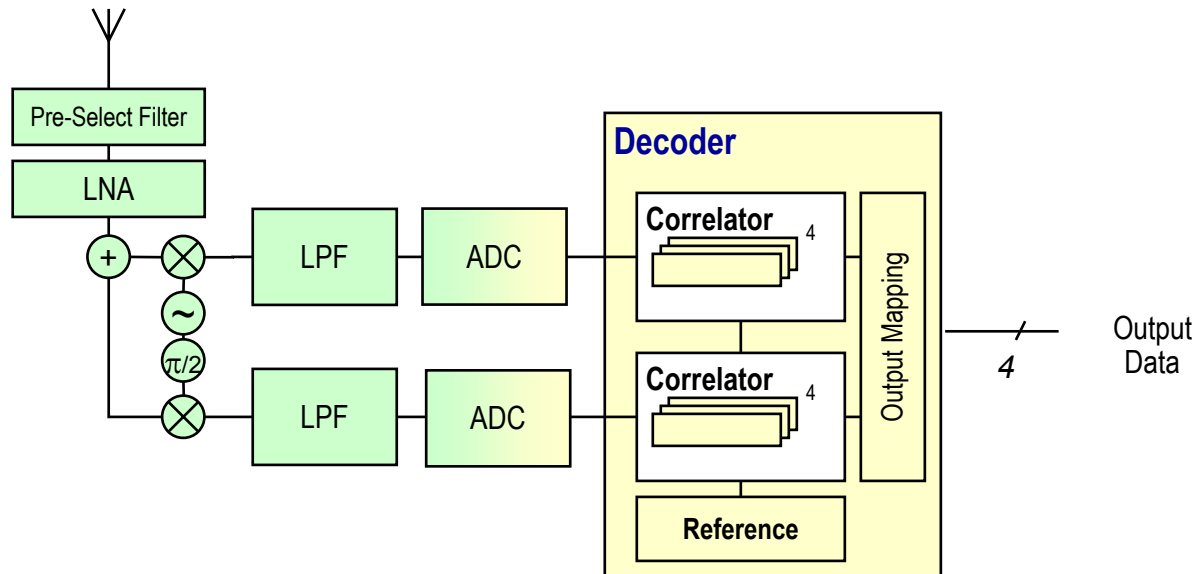
Tx

Rx

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2.4 GHz PHY – Rx architecture example (1/16 Bit/s/Hz)

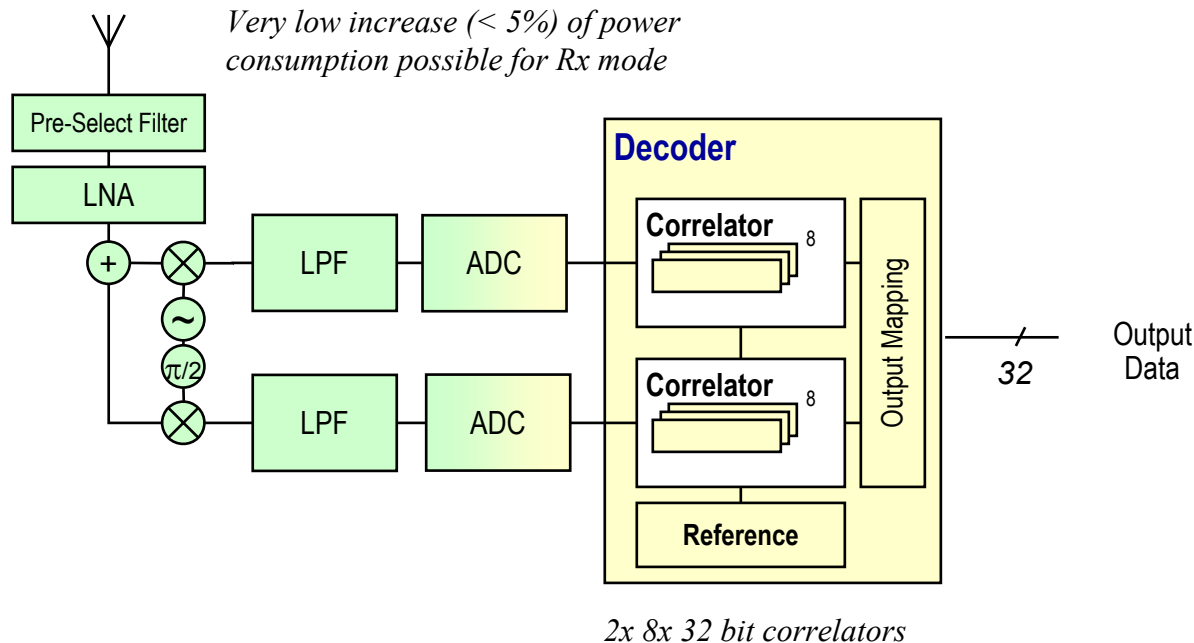


Digital Analog

Note:

Most existing IEEE802.15.4 2.4 GHz chips are built with ≥ 4 -bit ADCs

PSSS - 8 Times parallel 2.4 GHz PHY derivate – Rx: Original O-QPSK / I/Q proposal (1/2 bit/s/Hz) – Digital correlation example

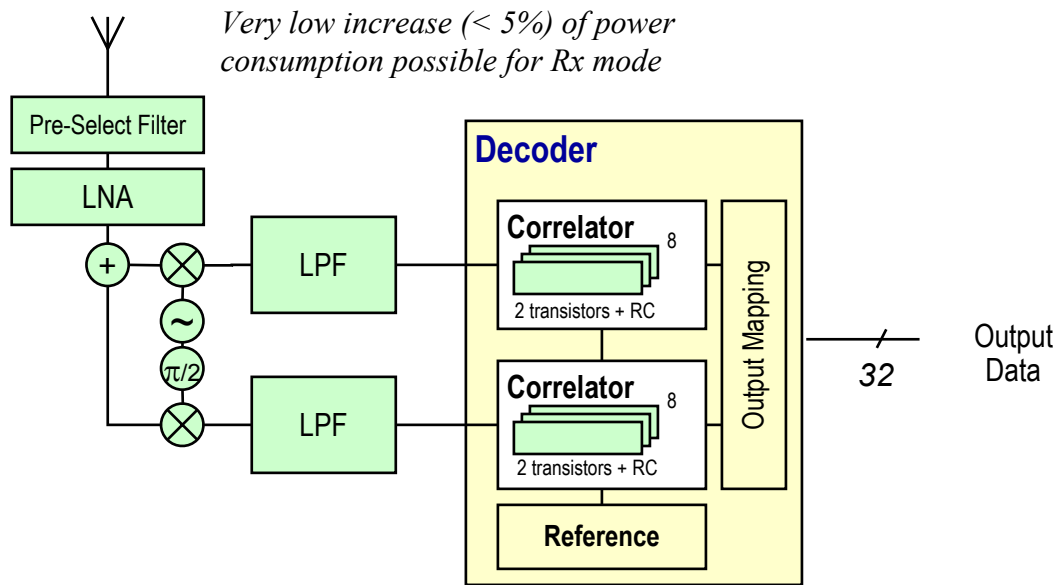


Digital
 Analog

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PSSS - 8 Times parallel 2.4 GHz PHY derivate – Rx: Original O-QPSK / I/Q proposal (1/2 bit/s/Hz) – Analog correlation example



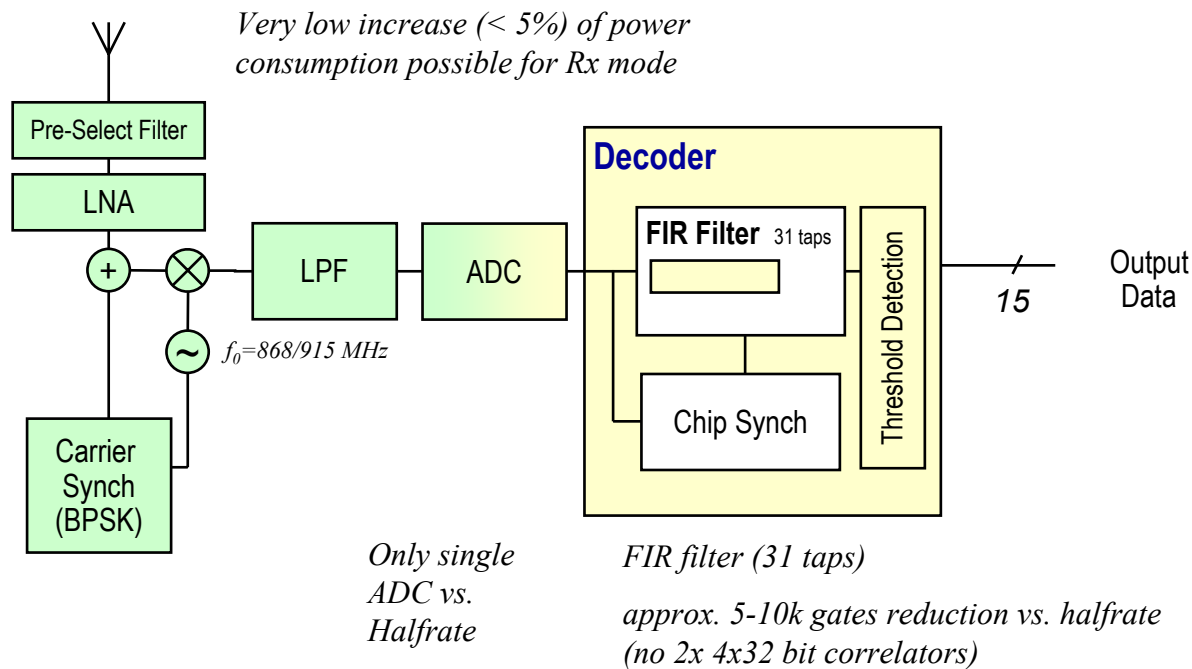
No ADCs vs. Halfrate

16 analogue integrate & dump, approx. 5-10k gates reduction (no 2x 4x32 bit correlators)

Note:
The Rx example architectures shown (digital, analog, FIR correlator) and the modulation variant can be freely combined

Digital
 Analog

PSSS - 8 Times parallel 2.4 GHz PHY derivate – Rx - BPSK/ASK option (15/32 bit/s/Hz) – FIR filter correlation example



Digital
 Analog

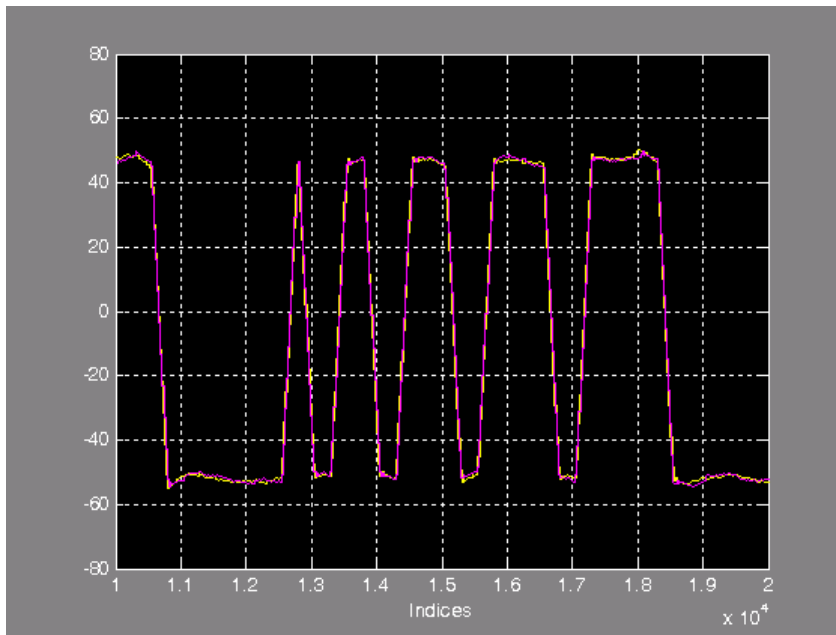
Crystal quality – Tolerated frequency offset

- Performance against frequency offset –
Original target in TG4: Up to $\pm 40\text{ppm}$
 - Assumptions for chip clock:
 - PDU length 127 Byte = $8 \cdot 127$ bit = 1016 bit
 - 15 bit per PSSS Symbol (32 chip)
 - \rightarrow 68 PSSS Symbols with 2176 chips (Chip duration $T_c = 2\mu\text{s}$)
 - Results
 - 40ppm for 2176 chips = 0.087 chip error for the whole PDU
 - For one PSSS Symbol with 32 chips
the error is about $40\text{ppm} \cdot 32$ chip = 0,00128 chip

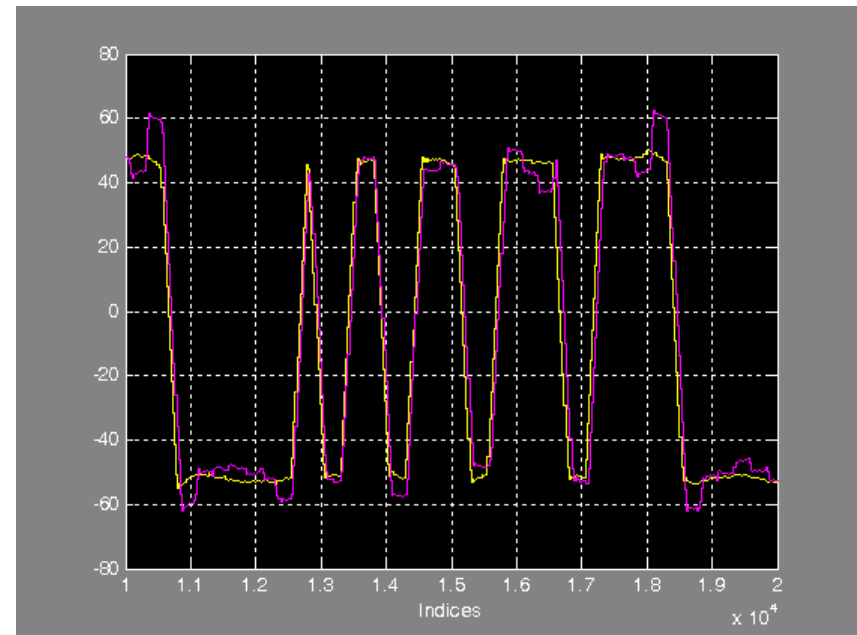
 **No influence to PSSS Performance by $\pm 40\text{ppm}$ and worse crystal**

Crystal quality – Tolerated frequency offset – Measurements from PSSS prototype

0.1% Chip Clock Error



1% Chip Clock Error

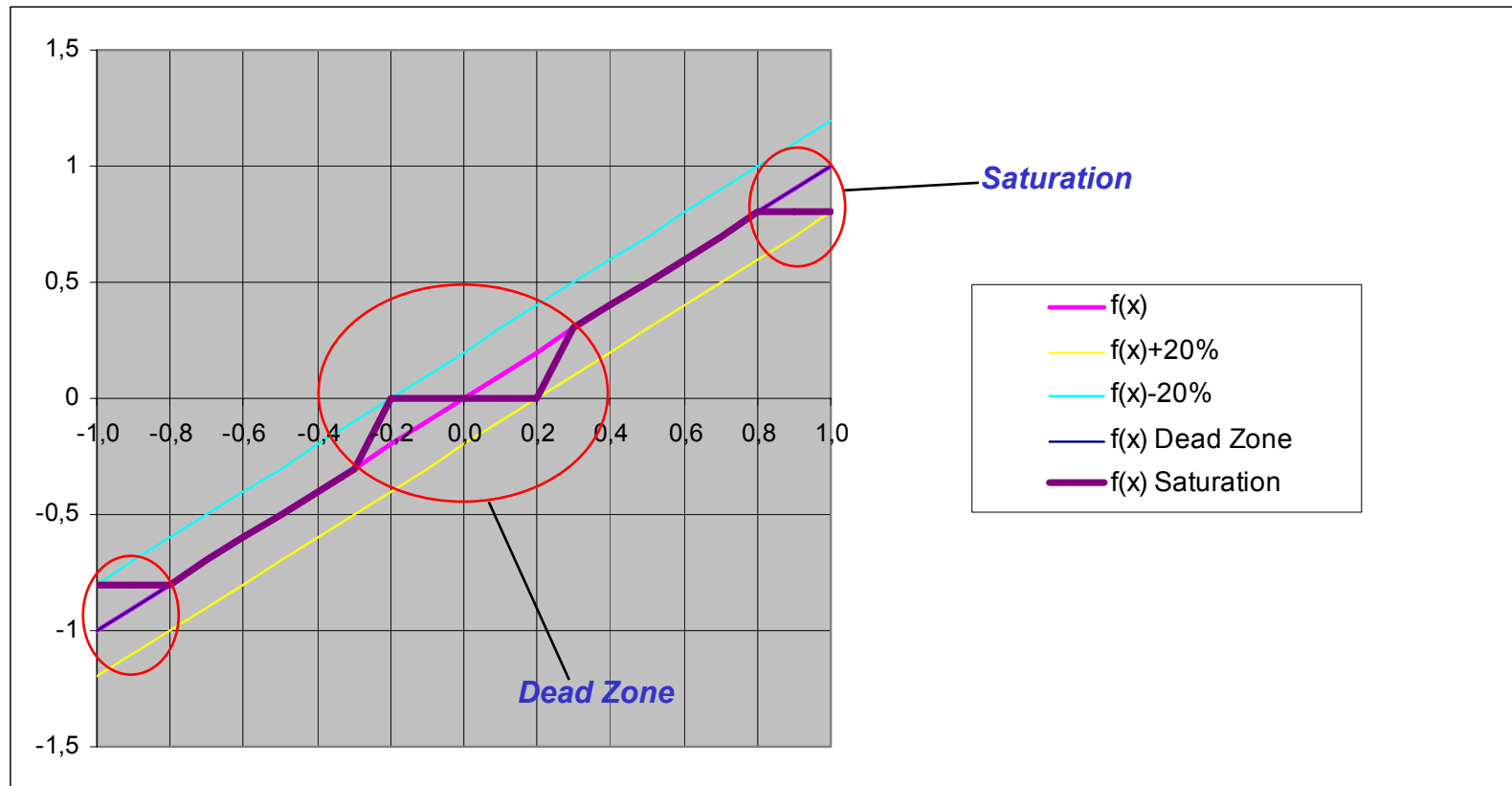


Yellow: 0% chip clock error reference signal
Pink: 0.1% and 1% chip clock error

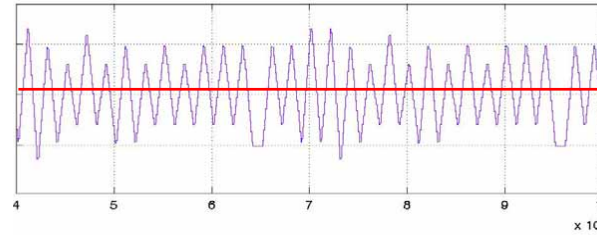
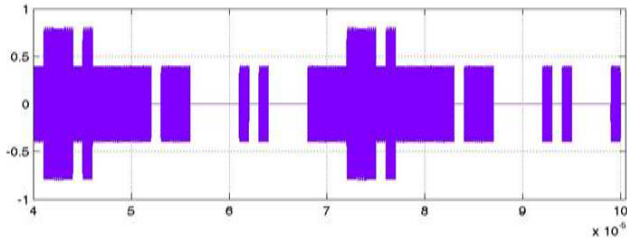


Calculation of crystal quality tolerance confirmed with prototype

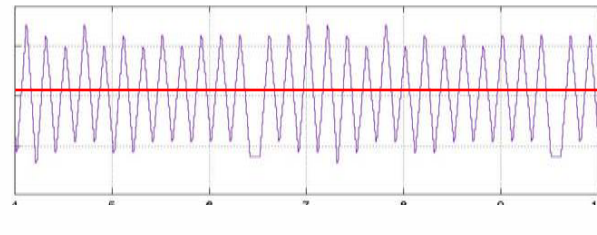
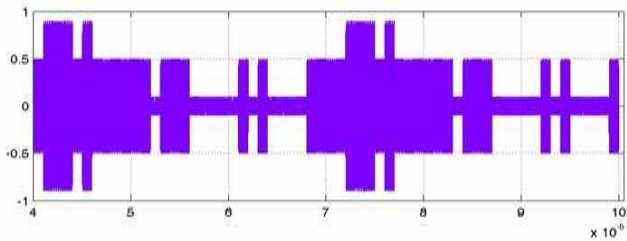
Linearity – Transfer function for non-linear system simulated



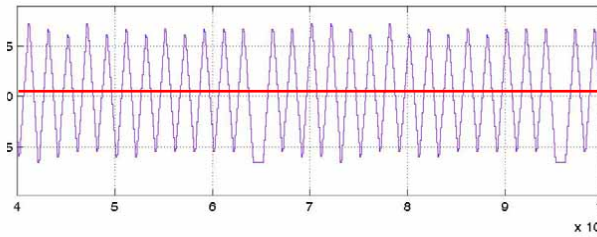
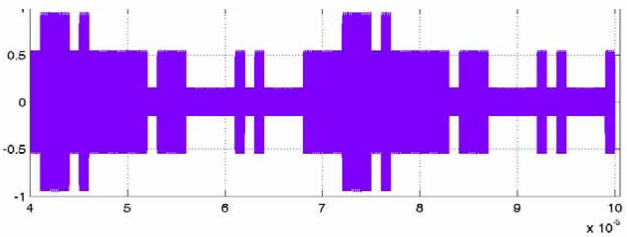
Linearity – Simulation results



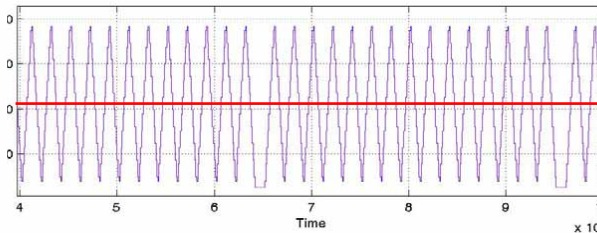
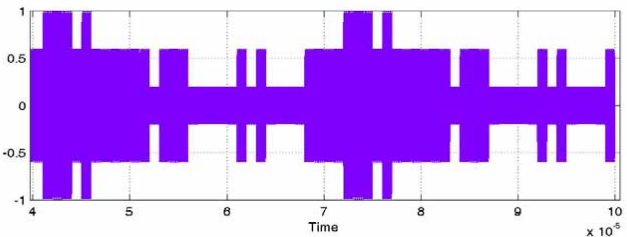
20% non-linearity



10% non-linearity



5% non-linearity



0% non-linearity

— Detection threshold (for '0' or '1' data bits)

Linearity - Conclusions

- PSSS works even with 20% non linear PA and LNA
- PA and LNA designs are available off-the-shelf with
 - No increase in chip cost even for linearity of 2%
 - No additional power consumption compared to C class PA used in IEEE802.15.4-2003 today
- No impact of linearity requirements on power consumption
 - Reviewed and confirmed with two large semiconductor manufacturers
- No implementation risk due to increased linearity required for PSSS !

 **Non-linearity simulations are confirmed with PSSS prototype**

Note:

Raised cosine pulse shaping in IEEE802.15.4-2003 2.4 GHz in baseband requires higher linearity than binary signal – Class-C PA insufficient

Chip size and power consumption

Chip size


- High tolerance towards non-linearity and simplicity of PSSS minimizes increase in analog part
 - Estimate 0.25 mm² max.
- Digital part: No increase expected due to reduced complexity.
- **Total increase:** 7-10 % PHY max.
4-6 % TRx die
2-3 % SoC die
< 2% SoC cost !
- Increase in size also for Halfrate for required dual radio core
- PSSS proposal option with BPSK/ASK would even reduce chip sizes

Power consumption

- High tolerance against non-linearity and simplicity of PSSS minimizes increase in power consumption
 - Estimate Rx/Tx: 5-10% max.
Sleep: <0.05 μ A
- 15.4 2.4 Ghz chips today spread between 15...55 mA Rx
 - Effect of implementation + process is large vs. increase from PSSS (if any)
- **No visible change in battery lifetime**
 - Most energy for sleep+discharge
 - Longer battery life vs. current 868/915
- Increase expected also for Halfrate due to required dual radio core
- PSSS proposal option with BPSK/ASK has even lower power needs

Assumption: 0.18 μ CMOS process

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Status

- Comprehensive research and development on PSSS has been performed based on:
 - **Full simulation**
 - **Configurable prototype for PSSS**
 - **Analytical model for PSSS**

 Minimal risk for implementation due to well understood technology and all building blocks being widely available

PAR compliance

- PSSS as proposed is *derivative* of current 2.4 GHz PHY – *fulfills PAR*
 - 32-chip base codes, shifted to derive multiple codes
 - 32 complex chips per symbol in airlink
 - 8x parallel use of 2.4 GHz PHY coding scheme
 - Use of O-QPSK / I/Q modulation
- Confirmed by TG4b task group in May 2004 meeting – Discussion / review found unanimously that “**nothing that is presented here is against the PAR**” (minutes in IEEE 15-04-0272-00-004b)
 - Basis for this statement was a comparison presented and discussed based on the March presentations of PSSS (IEEE 15-04-121-03-004b) and Halfrate
- BPSK/ASK option proposed is based on OEM / chip requirement
 - Reduction of complexity and cost due to single radio core
- If we interpret “**derivative**” as “**identical at half the clock rate**” we likely miss the market opportunity with TG4b and open for competition
 - Only Halfrate fulfills “**narrow**” interpretation – but cannot be used in Europe
 - We need to fulfill the PAR *and* the requirements to build a successful standard

Summary

- The proposed parallel reuse of the 2.4 GHz 802.15.4 modulation technology in PSSS offers highly attractive performance improvement increasing market opportunities
 - Higher data rate and multiple channels possible in both current *and* upcoming European band and certainly also in 915 MHz band
- Significantly stronger multipath fading robustness in PSSS – up to 2 μ s
 - Visibly higher range in many attractive, high volume target areas
- 7.5x higher spectral efficiency through PSSS compared to the current PHY for 868/915 MHz – 8x higher vs. Halfrate proposal
 - Enables higher data rates for lower power consumption
 - Turns duty cycle limits in Europe into protection against interference
 - More efficient use of spectrum and resulting better coexistence
- Very easy backward compatibility to the 2.4 GHz PHY, also easy adaptation to current 868/915 MHz designs
 - PSSS is derivative superset of current 2,4 GHz PHY technology
 - Automatic fallback to current 15.4 868/915Mhz standard easily possible



Only proposal that fulfills all key OEM requirements