Project	**IEEE 802.16j Mobile Multihop Relay Task Group**
Title	**Rate Compatibility and Incremental Redundancy HARQ for 802.16j LDPC**
Date	**2006-11-06**
Source(s)	Wataru Matsumoto Toshiyuki Kuze Mitsubishi Electric Corp 5-1-1 Ofuna Kamakura, Kanagawa 2478501, Japan Voice: +81-467-41-2074 Fax: +81-467-41-2136 Matsumoto.Wataru@aj.MitsubishiElectric.co.jp Kuze.Toshiyuki@ah.MitsubishiElectric.co.jp Koon Hoo Teo, Jinyun Zhang Mitsubishi Electric Research Lab 201 Broadway Cambridge, MA 02139 USA Voice: 617-621-7527, 617-621-7595 Fax: 617-621-7550 {teo, jzhang}@merl.com
Re:	Response to the call for proposal of the 802.16j relay TG (i.e., IEEE 802.16j-06/027, “Call for Technical Proposals regarding IEEE Project P802.16j”, October 15, 2006).
Abstract	This contribution describes an enhancement to the current IEEE 802.16e LDPC.
Purpose	To enhance the current IEEE 802.16e LDPC as suggested in this contribution.
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Rate Compatibility and Incremental Redundancy HARQ for 802.16j LDPC

Wataru Matsumoto ,Toshiyuuki Kuze
Mitsubishi Electric Corp
5-1-1 Ofuna Kamakura, Kanagawa
2478501, Japan

Koon Hoo Teo, Jinyun Zhang
Mitsubishi Electric Research Lab
201 Broadway
Cambridge, MA 02139 USA

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Wataru Matsumoto ,Toshiyuuki Kuze
Mitsubishi Electric Corp
5-1-1 Ofuna Kamakura, Kanagawa
2478501, Japan

Koon Hoo Teo, Jinyun Zhang
Mitsubishi Electric Research Lab
201 Broadway
Cambridge, MA 02139 USA

1. Introduction

One of the most important advantages of LDPC is its higher decoding efficiency compared to Turbo codes. Therefore, a high throughput link such as BS-RS or RS-RS could be achieved with lower hardware cost. Unfortunately, current 802.16e LDPC is not rate compatible and does not support 1/3 code rate. In addition, the current LDPC only support HARQ with chase combining but not incremental redundancy (IR).

1/3 code rate and IR HARQ are known to improve reliability or robustness in links with hostile channel conditions.

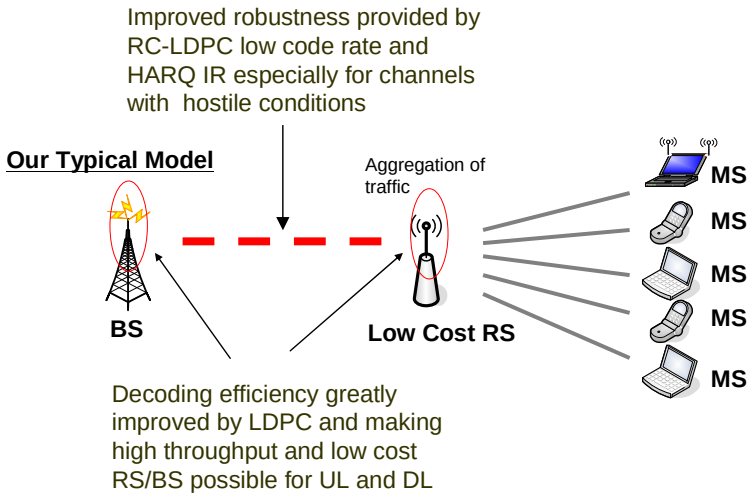

Figure 1: The merits of LDPC and RC-LDPC

We proposed an enhanced version of 802.16 LDPC using the current 802.16e LDPC as the baseline. This enhanced LDPC shown in Figure 1, which we called rate compatible RC-LDPC will support 1/3 rate code and also

provide the mean to support HARQ with incremental redundancy to provide the BS-RS and RS-RS links operating in hostile channel condition, with high throughput, improved robustness and increased decoding efficiency.

2. Summary of Proposal

We proposed the construction of an extended parity-check matrix of the RC(Rate-Compatible)-LDPC codes to achieve good performance for wide range of code word length and code rate. The parity-check matrix construction method can support code rates ranging from 1/3 to 4/5 and codeword lengths ranging from 288 bits to 2304bits. The RC-LDPC codes are constructed using a code-rate 1/2 parity-check matrix for code-rate greater than or equal to 1/2. For code rate smaller than ½ an additional parity check matrix is being extended to the ½ parity-check matrix.

The proposed RC-LDPC uses the current 802.16 LDPC as the baseline matrix. It also uses the same four sub-packets protocol for its HARQ operation. The proposal provide some small additions and require no change to the current 802.16e LDPC.

3. Performance Results

	LDPC	TC	Complexity of LD / Complexity of TC
Algorithm	LBP Min-Sum+Offset	Max Log Map +extrinsic scaling	
Number Iterations	20	8	
Total cost (R=1/3)	38.5K x 20 = 770K	171K x 8 = 1368K	56%
Total cost (R=1/2)	28.8K x 20 = 576K	171K x 8 = 1368K	42%
Total cost (R=3/4)	20.6K x 20 = 412K	171K x 8 = 1368K	30%

Table 1:Operations count comparison of sub-optimal decoders LDPC and TC decoders

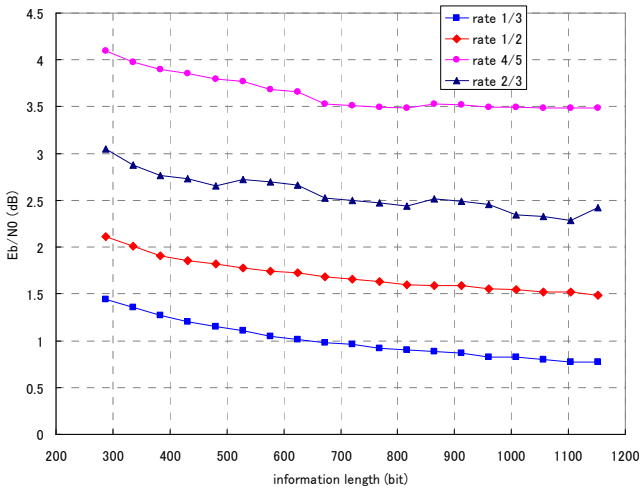

Figure 2: Performance for RC LDPC codes based on the 16e LDPC codes

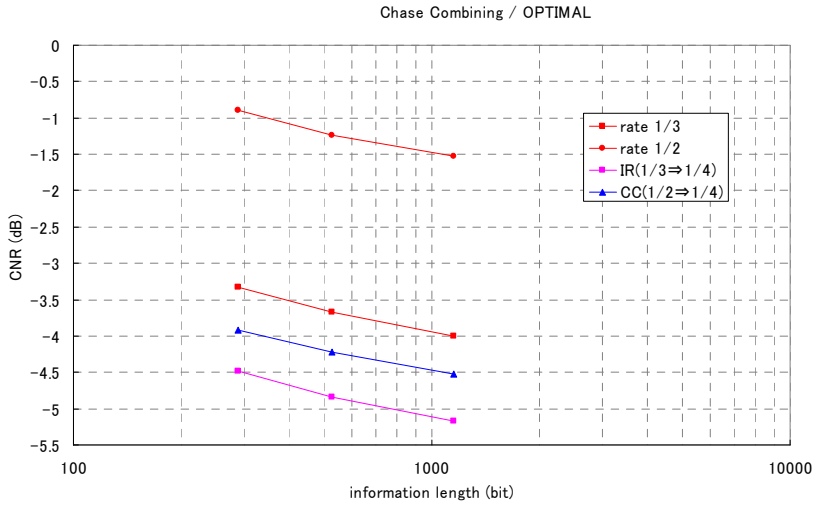

Figure 3: Performance of RC LDPC codes based on the 16e LDPC

4. Proposed Additions

6.3.17 No change necessary

6.3.17.1 No change necessary

6.3.17.2 No change necessary

6.3.17.3 No change necessary

8.4.9.2.5.1 Code description (add in)

We propose the parity check matrix for rate-compatible LDPC(RC-LDPC) codes using the parity-check matrix for rate-1/2 specified in the 802.16e as the following Figure 4.

Extend for Code Rate=1/3

−1	94	73	−1	−1	−1	−1	−1	55	83	−1	−1	7	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	27	−1	−1	−1	22	79	9	−1	−1	−1	12	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	24	22	81	−1	33	−1	−1	−1	0	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
61	−1	47	−1	−1	−1	−1	−1	65	25	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	39	−1	−1	−1	84	−1	−1	41	72	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	−1	46	40	−1	82	−1	−1	−1	79	0	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	95	53	−1	−1	−1	−1	−1	14	18	−1	−1	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	11	73	−1	−1	−1	2	−1	−1	47	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
12	−1	−1	−1	83	24	−1	43	−1	−1	−1	51	−1	−1	−1	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	−1	−1	94	−1	59	−1	−1	70	72	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	7	65	−1	−1	−1	−1	39	49	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
43	−1	−1	−1	−1	66	−1	41	−1	−1	−1	26	7	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	−1	−1	17	−1	9	−1	−1	−1	20	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	36	−1	−1	−1	−1	−1	−1	7	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	5	−1	−1	−1	−1	−1	−1	5	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	−1	−1	23	−1	11	−1	−1	−1	23	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1
−1	−1	−1	−1	−1	5	−1	32	−1	−1	−1	38	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1
−1	−1	7	−1	−1	−1	−1	−1	−1	19	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1
−1	−1	−1	−1	−1	31	−1	23	−1	−1	−1	48	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1
−1	−1	−1	−1	−1	29	−1	37	−1	−1	−1	7	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1
−1	−1	6	−1	−1	−1	−1	−1	−1	3	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1
−1	−1	1	−1	−1	−1	−1	−1	−1	2	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1
−1	−1	−1	−1	−1	37	−1	26	−1	−1	−1	8	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0
−1	−1	3	−1	−1	−1	−1	−1	−1	6	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	−1	0

Figure 4 Parity check matrix for rate compatible LDPC codes

Let $\mathbf{u}$ and $\mathbf{r}$ be information bits as $\mathbf{u}=(u_1 \quad u_2 \quad \cdots \quad u_K)$ and parity bits as $\mathbf{r}=(r_1 \quad r_2 \quad \cdots \quad r_M)$, respectively. And Let $\mathbf{v}$ be a systematic codeword such that:

$\mathbf{v} \coloneqq (u_1 \quad u_2 \quad \cdots \quad u_K \quad r_1 \quad r_2 \quad \cdots \quad r_M)$. satisfying $\mathbf{H}_M \cdot \mathbf{v}^T = \mathbf{0}$.

The RC-LDPC encoder consists of a common LDPC encoder and a puncturing device. The decoder for RC-LDPC codes is the same as an ordinary LDPC decoding algorithm with received LLR=0 for puncturing bits.
A set of code rates and un-puncturing bits set $\hat{\boldsymbol{r}}$ for RC-LDPC codes can be represented by:

For the number of un-puncturing bits $i(\leq M/2)$, $\hat{\mathbf{r}} = \{\hat{r}_l\}$,

$\boldsymbol{q} = \{q_y : 8,4,6,2,7,3,5,1\}$;

$x = q_0$, $y = 0$;

For $l = 1$ to i

If $x \leq M/2$ then $\hat{r}_l = r_x$, $x = x + 8$;

Else $x = q_y$, $y = y + 1$;

Endif

End for

For the number of un-puncturing bits $i(> M/2)$, $\hat{\boldsymbol{r}} = \{\boldsymbol{r}_l\}$, for $M/2 \leq l \leq i$.

8.4.9.2.5.3.1 Packet encoding for HARQ (insert)

The reordered codeword for RC-LDPC codes are defined such as

$$\overline{\mathbf{v}} := (\overline{v}_1 \quad \overline{v}_2 \quad \cdots \quad \overline{v}_{K+M}) = (u_1 \quad u_2 \quad \cdots \quad u_K \quad \hat{r}_1 \quad \hat{r}_2 \quad \cdots \quad \hat{r}_M).$$

8.4.9.2.5.4 Subpacket generation for LDPC (insert)

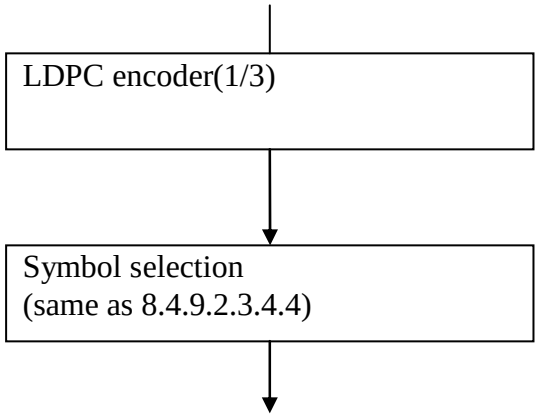

Figure 5: Block diagram of subpacket generation

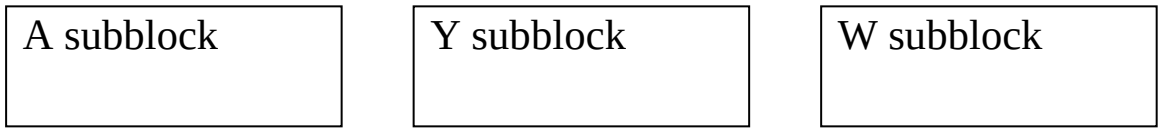

Figure 6: Subblocks for RC-LDPC codes

8.4.9.2.5.4.1 Symbol separation (insert)

All of the encoded symbols shall be demultiplexed into three subblocks denoted A, Y, and W.

A, Y, and W subblocks are defined as

$$\mathbf{A} := (u_1 \quad u_2 \quad \cdots \quad u_K), \mathbf{Y} := (\hat{r}_1 \quad \hat{r}_2 \quad \cdots \quad \hat{r}_{M/2}), \text{and } \mathbf{W} := (\hat{r}_{M/2+1} \quad \hat{r}_{M/2+2} \quad \cdots \quad \hat{r}_M).$$

8.4.9.2.5.4.2 Symbol selection (insert)

same as 8.4.9.2.3.4.4

8.4.15 Optional HARQ support

8.4.15.2.2 Optional IR HARQ for LDPC (insert)

The following optional modes exist for HARQ.

Incremental redundancy for LDPC codes –specified in section 8.4.9.2.5.4

5. Conclusions

LDPC support high throughput with less hardware complexity and lower cost compared to Turbo Codes. Our RC-LDPC is an enhanced version of the current 802.16e LDPC. It uses the 802.16e LDPC as a baseline. RC-LDPC is rate compatible and can provide 1/3 code rate and Hybrid ARQ with incremental redundancy. For operation in very hostile channel conditions as shown in Figure 7, such as those encountered by mobile RS or non-LOS fixed RS and nomadic RS, RC-LDPC would be able to provide improved robustness to the BS-RS or RS-RS links.

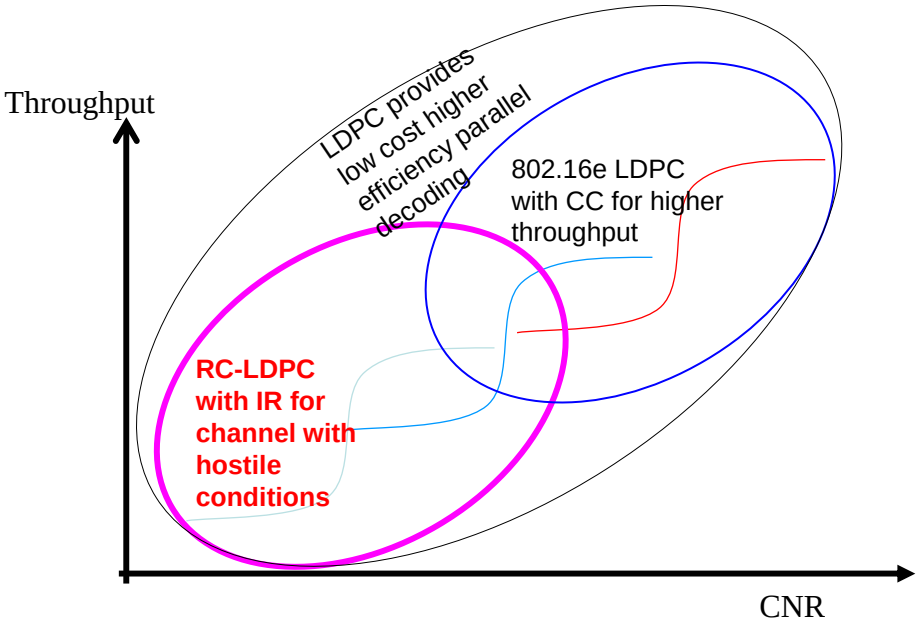

Figure 7: RC-LDPC is best for hostile channel conditions