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Re:	This is a response to a Call for Contributions on Frequency Synthesizer Model Parameters IEEE 802.16.1p-00/10, 2000-07-13.
Abstract	Parameters and a simulation model for a frequency synthesizer are proposed.
Purpose	This contribution is offered IEEE 802.16 group as a means for understanding different aspects of the frequency synthesizer.
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Frequency Synthesizer Model Parameters

The frequency synthesizer is an important part of any communication equipment and especially in the microwave frequency area it can be considered a critical component in many respects. The design and implementation solutions will have a heavy impact on the overall performance and cost. It is therefore justified to pay attention to the modeling and simulation of the synthesizer. The cost of a synthesizer is often also a significant part of the total cost of RF components and thus a careful selection of the system parameters can make it possible to realize a low cost frequency synthesizer.

This document tries to describe different frequency synthesizer properties and what kind of parameter values are needed to achieve the design specifications optimized for 4-QAM and 16-QAM modulation. It is noted that many of the design requirements are contradictory and in practice some compromises must be made. A synthesizer phase noise model is given and a simulation method to numerically generate phase noise samples according to the given parameters. The purpose of this document is to assist IEEE 802.16. It is offered as a basis for discussion and is not binding.

1 System parameters affecting the frequency synthesizer implementation

1.1 Transmit/receive switching time

In a Half FDD system the frequency needs to be changed between transmit and receive periods and the time allowed for this operation sets a requirement for the phase locked loop (PLL) switching and settling time.

To make the PLL faster, the loop bandwidth need to be wider, which has a practical limit due to limited speed/bandwidth of the components used in the PLL e.g. operational amplifiers in active loop filters, phase comparators etc. Also the cost of faster components are often higher.

The switching time is also limited by the reference frequency, which is proportional to the frequency step, if the raster is coarse the settling time will also be small.

A big jump in frequency can also be limited due to the voltage controlled oscillator (VCO) tuning time i.e. when a step voltage change in the VCO tuning input takes place, a certain time is still required for the VCO output frequency to change to another frequency.

If the switching time requirement can not be fulfilled with one synthesizer, two parallel synthesizers have to be used and only the output of the synthesizers will be switched. This will double the cost of the components in the synthesizer and there can be difficulties in avoiding crosstalk of the two synthesizers.

1.2 Frequency band and channel allocation

A wide tuning bandwidth drives the technology chosen for the VCO, good phase noise performance and wide tuning bandwidth are often contradictory requirements. To realize a wide tuning bandwidth with low cost usually means that the phase noise performance can not be optimized.

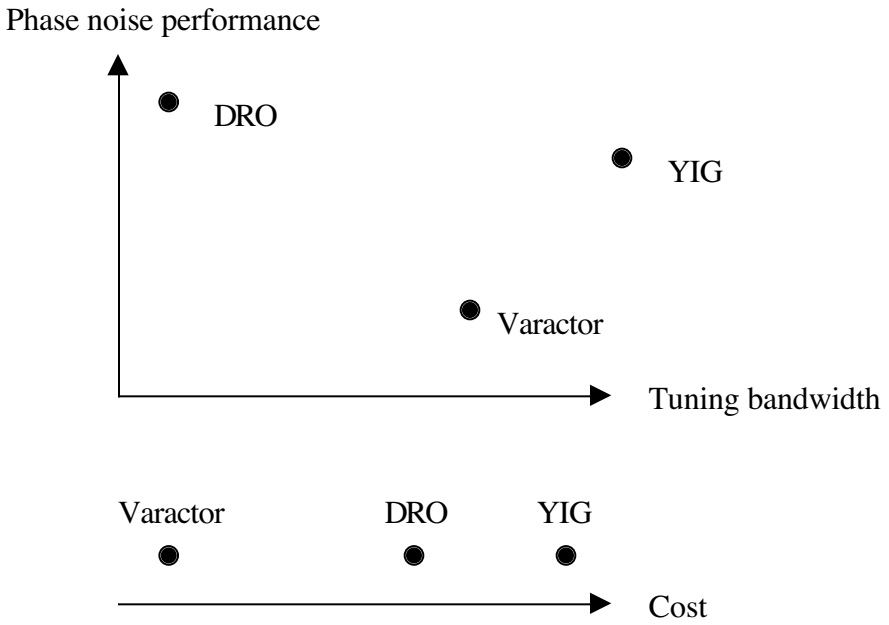
Typically the PLL loop bandwidth is made as wide as practically is possible to optimize the switching speed and overall phase noise (phase noise integral). To make this possible there should not be a requirement to set any other frequency than those that will be in the center of the channels used, also the raster should remain constant i.e. the offset between up and downlink bands should be a multiple of channel bandwidths.

To simplify the PLL, the center frequency of the first channel should also be a multiple of the channel spacing. This way there would be no need to use an offset oscillator in the PLL, the needed frequencies could be directly generated from a single crystal oscillator.

1.3 Phase noise

Phase noise performance is very important in a radio system, in a digital radio system this parameter is the main contributor to the lowest achievable BER performance of the system.

However, in practice this parameter can not be selected independently of other parameters and thus below is a comparison of some typical VCO technologies used at millimeter wave frequencies.



Technically the best solution would be based on a YIG resonator, which provides very wide bandwidth and good phase noise performance, but this requires bulky electromagnet for tuning and the cost is very high.

A DRO provides very good phase noise performance, but with very limited electrical tuning range. In practice, many frequency variants of the final product should be used and/or manual tuning of the VCO should be made possible. In a low cost product this approach is out of a question.

A varactor based microstrip resonator is a good compromise in this optimization problem, it gives a wide enough tuning bandwidth with moderate phase noise performance, and most importantly, the cost is only a fraction of the implementation cost compared to a DRO or YIG.

To enable a low cost approach the phase noise requirement should not be made too stringent by requiring of receiving higher order of modulation than 16 QAM.

1.4 The effect of multiplication

A fundamental problem with higher frequency systems is the increase of the phase noise at same carrier offset by a factor of n^2, where n is the multiplication factor. In other words, when the frequency is doubled, the phase noise increases by 6 dB. The demodulator, however, works at baseband and suffers from higher phase noise, when the carrier frequency is increased. This issue should be noted especially at millimeter wave bands.

1.5 Relation between channel width and symbol rate

In order to keep the phase noise low, the relationship between the channel width and symbol rate should be defined by a small rational number.

1.6 Parameters

The following parameter values are suggested for a frequency synthesizer optimized for 802.16.1 equipment.

Frequency range GHz	3 GHz
Frequency raster MHz	20 – 30 MHz
Raster offset MHz	0
Tx/Rx switching time/accuracy Switching time from upstream to downstream frequency range (important for half-duplex terminals)	50 us 50 us
Channel switching time/accuracy	50 us
Power output dBm	-10
Harmonics suppression dBc	-20
Spurious response dBc	-55
Reference leakage dBc	-55
Single Side Band Phase Noise dBc/Hz at frequency offsets 10k 100k 1M 10M	 -58 -71 -98 -118
Noise Floor dBc	-140
Integrated phase noise dBc Total integrated phase noise from 0 Hz to infinity, in radians squared, and multiplied by two	-31 0.028 rad
Reference Frequency	

Table 1. Parameter table

Justication of the parameter values:

- Frequency range: According to the system requirements an 802.16.1 system operates in the vicinity of 30 GHz, but generally in the range from 10 GHz to 66 GHz. Using 30 GHz as the reference frequency area a 3 GHz tuning range is considered reasonable.
- Frequency raster: The 802.16.1 does not specify a channel width, but the system is required to provide a peak capacity of upto 155 Mbps so the synthesizer should be able to work with channel widths between 20 and 30 MHz.

- Frequency raster: In order to simplify the frequency synthesizer it is suggested that there is no raster offset.
- Tx/Rx switching time/accuracy: If the switching time is longer, there will be a significant reduction in maximum capacity.
- Switching time from upstream to downstream frequency range: If the frequency allocation is not symmetrical there might be a need to switch the frequency almost across the whole band in half FDD mode.
- Power output: The frequency synthesizer will be driving frequency up- and downconverters.
- Harmonics suppression: the output of the harmonics should be low enough to avoid additional filtering.
- Spurious responses: spurious signals of all terminals will sum up as a interference from all terminals within a sector.

2 Phase noise simulation model for the frequency synthesizer

Phase noise will always be present at the output of the frequency synthesizer. It degrades the signal quality and is a major issue in receiver design. It can be controlled by proper parameter selection and it can be verified in advance by simulation. Simulation can be used to verify the frequency synthesizer by numerically generate the phase noise. The phase noise generator should be included in the receiver simulator in order to precisely dimension the carrier phase control loop.

In this paper we chose to propose a transform based simulation method. The major advantages of this method the are following:

- Uses well known mathematical tools
- Works with any phase noise model independently of the shape of the phase noise mask
- Easy to generate
- Easy to include spurious responses as well

2.1 Overview of the transform method

The principal phase noise block-diagram is shown in the Figure 1 below. The main noise signal is generated by a IFFT of a given frequency response. This frequency-domain signal is computed from the phase noise parameters. The parameters corner point frequencies f_1, f_2 and their corresponding values of attenuation describe the desired frequency response. The additional White Gaussian Noise signal with the corresponding flat (but time dependent) frequency response must be transformed into a frequency domain signal. The multiplication of both signal paths result in a time dependent phase noise spectrum. The IFFT of the signal is a good approximation of the wanted phase noise signal.

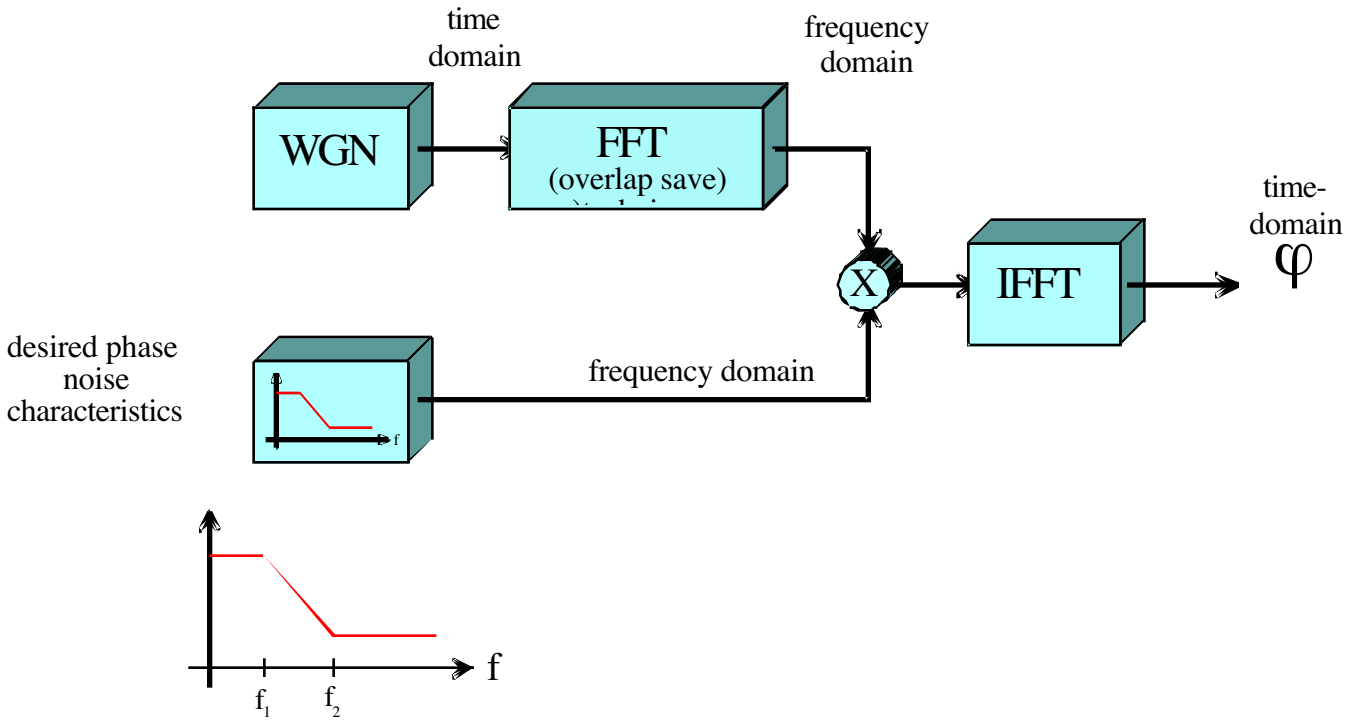


Figure 1. Transform based phase noise simulation model

This method is straight forward for generating phase noise for burst mode transmissions but for the case of continuous transmission an overlap and save method must be used to insure a continuos output signal.

As an example of this method we use the phase noise requirement to generate phase noise for a low cost frequency synthesizer suitable for upto 16-QAM modulation.

Offset, kHz	10	100	1000	10000
SSB phase noise dBc/Hz	-58	-71	-98	-118

Table 2. Low cost frequency synthesizer phase noise characteristics. 16-QAM modulation assumed.

In the simulation we have used a symbol rate of 20 Msym/s, the four corner points from table 2 and 1024 points describing the phase noise for approximately 50 us.

It is noted that a low cost frequency synthesizer generates relatively strong phase noise in the time domain. The phase noise must be canceled by the carrier phase control loop in the receiver.

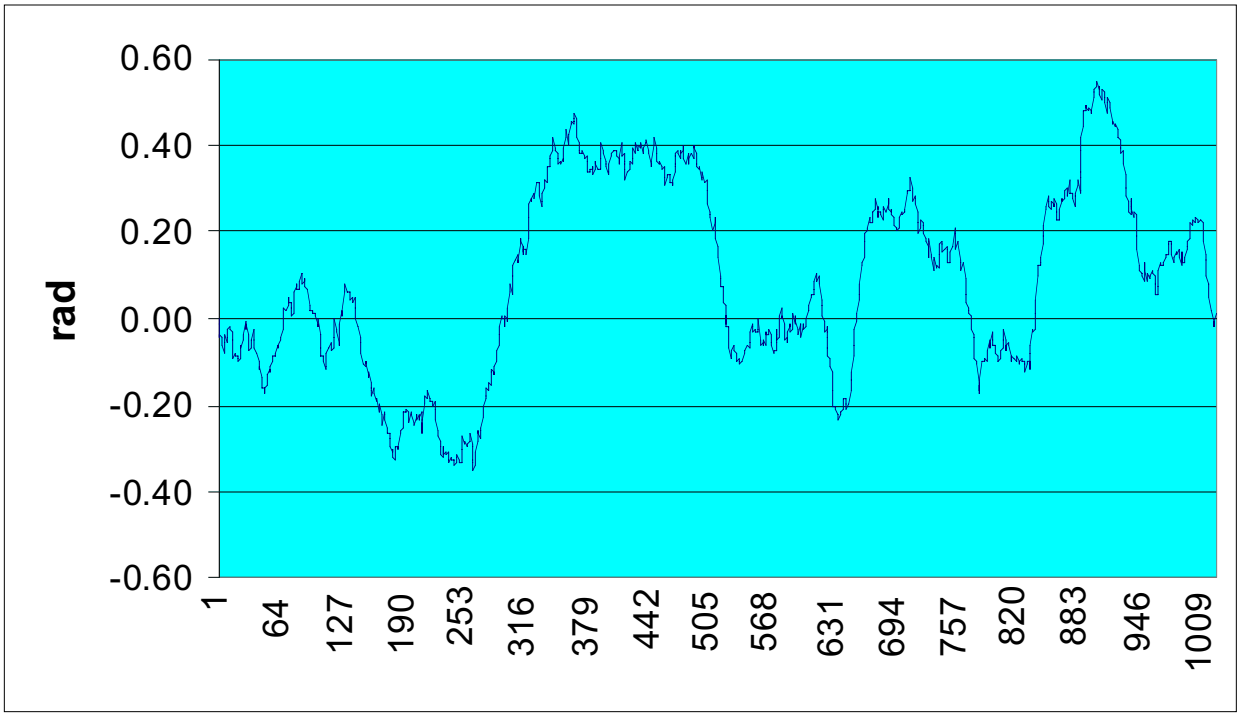


Figure 2. Generated phase noise according to table 2.

Conclusions

A realistic set of parameters suitable for a low cost microwave frequency synthesizer have been proposed for the IEEE 802.16.1. The parameters are believed to be achievable with low cost solutions and the performance can be verified with the proposed simulation model.

With the proposed parameters the frequency synthesizer can be used with 16-QAM modulation. It is believed that for 64-QAM the SSB phase noise requirement should be about 10 dBs lower.

References

[1] IEEE 802.16.1 Functional Requirements

[2] D. Falconer, T. Kolze, Y. Leiba, J. Liebetreu: Proposed System Impairment Models, IEEE 802.16.1pc-00/15.