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Re:	This document is intended for discussion on PHY open issues regarding parameters of the FEC mandatory schemes for burst communication.
Abstract	See above
Purpose	See above
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FEC Parameterization for Control Channel information

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This paper analyzes forward error correction (FEC) schemes suitable for control channel like information specifically the bandwidth allocation maps. An important thing to note is that the FEC performance and selection criterion for control information is somewhat different from that for the user data as there is a need for higher reliability. Also, the control information needs to be used almost immediately, thus requiring very low decoding latency. Currently the FEC proposal for user's data allows for flexible FEC schemes providing trade off of coding gain Vs code rate to cope with high capacity/low coverage and low capacity/high coverage scenarios. This implies that the system will need to work with different C/N. For the simplicity of network installation it is important to have a fixed FEC scheme for the control information. Thus the FEC should provide acceptable performance at the minimum possible C/N of the BWA system. In brief, any FEC scheme which meets the required performance (in terms of block error rate) at the minimum C/N with acceptable decoding latency is a candidate. Also, it is desirable that the FEC for the map is compatible with the FEC for data field so that encoder and decoder hardware can be shared. A FEC scheme which meets all of the above requirements with maximum coding efficiency should be selected. We list the desirable features of the FEC scheme for the control channel:

(1) Fixed

(2) Achieves the specified reliability at the minimum operating C/N using QPSK modulation (Note that the control channel information always uses QPSK modulation.)

(3) Acceptable decoding delay

(4) Compatible with data FEC schemes

(5) Maximum possible efficiency

For example, the size of a BW allocation map range from 20 to 400 bytes, 40 bytes being the typical number. To minimize the decoding delay the code word size is recommended to be around 20 bytes. This number will be used for all the performance analysis, which follows. Let us assume that the minimum C/N is 5.45 dB. Assuming a 1 mSec frame and one uncorrectable block event per month in allocation map field as acceptable performance criterion, the desired frame error rate is approximately $10^{-10}(1/(2*1000*60*60*24*30))$. Hence the requirements are summarized as follows.

(1) Block size 20 bytes

(2) Operating C/N 5.45 dB

(3) Target block error rate 10^{-10}.

In this paper we will evaluate the performance of the following candidates.

(1) Multiple copies with CRC

(2) RS code

(3) RS code concatenated with soft parity code

(4) RS code concatenated with (24,16) code

(5) RS code concatenated with (32,16) code

Most of the above codes (except one) are part of the current IEEE 802.16.1 draft. Option (1) is included for the reason that it is the minimum latency solution. Although option (5) is not currently included in the draft it is the "mother code" of option (4) meaning it reuses the same hardware/software implementation.

We will evaluate the performance of each of the above schemes. We will obtain expressions for block error rate and code rate for each of the above schemes for given C/N and block size K.

Multiple copies with CRC

Let us assume that m copies each with k bytes of CRC for error detection is used. The probability that a copy contains an error is given by

$$P_{copy\_err} = 1 - \left(1 - Q\left(\sqrt{\frac{C}{N}}\right)\right)^{8(K+k)}$$

The block is not recoverable if all m copies contain errors. Hence the block error rate is given by

$$P_{block\_err}^{(1)} = \left(P_{copy\_err}\right)^m$$

And efficiency (code rate) of this scheme is given by the following expression

$$rate^{(1)} = \frac{K}{m(K+k)}$$

RS code

Before we present the performance of this scheme, we want to point out that for a small code word size, the RS decoding delay is not a problem. The decoding delay through RS decoder is 2N+R clock cycles, where N is the length of RS code word (K+R) and R is the redundancy. Since the map uses QPSK modulation, assuming baud clock is used for RS decoder, the decoding delay is (2N+R)/4 bytes which would be less than a block. The decoding delay can further be reduced to half if twice the baud clock which is always available from the modem is used for RS decoder. Thus as long as we have minimum of two RS code words in the allocation map, the decoding delay through RS decoder is not a problem for TDM application. Typical size of the map is expected to be around 40 bytes. In case where map is only 20 bytes, padding can be used. Thus the use of RS code meets the decoding delay requirements for the map data.

The probability of an erroneous byte is given by

$$P_{byte} = 1 - \left(1 - Q\left(\sqrt{\frac{C}{N}}\right)\right)^8$$

The block error rate and efficiency are given by the following expressions.

$$P_{block\_error}^{(2)} = \sum_{i=\lfloor R/2 \rfloor + 1}^{K+R} \binom{K+R}{i} (P_{byte})^i (1 - P_{byte})^{K+R-i}$$

$$rate^{(2)} = \frac{K}{(K+R)}$$

RS code concatenated with soft parity code

The probability of an erroneous byte from a soft decision parity code decoder is upper bounded by

$$P_{byte}^{\ parity} < \sum_{d=d_{\min}}^{8} a_d Q\left(\sqrt{2rd\frac{E_b}{N_0}}\right) = \sum_{d=d_{\min}}^{8} a_d Q\left(\sqrt{d\frac{C}{N}}\right)$$

where d_{min} is 2 the weight distribution a_d for the (m+1,m) parity code is given by

$$a_d = \binom{m}{d-1} + \binom{m}{d}$$

and $\binom{m}{k} = \frac{m!}{k!(m-k)!}$.

As found from the simulation and shown in the figure 1, the first term in the above summation is a good approximation for P_{byte}.

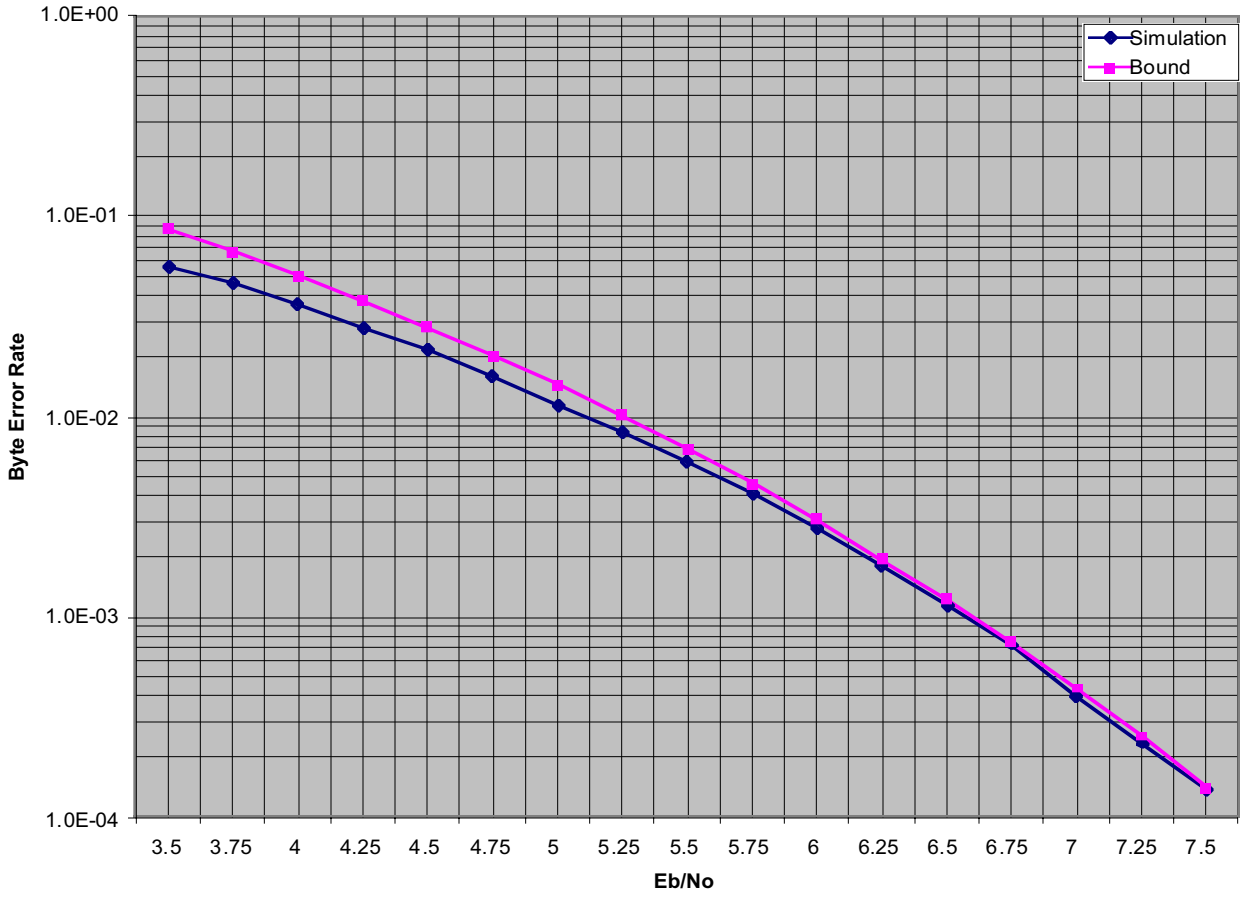


Figure 01. Performance of (9,8) Parity Code with Soft Decoding for QPSK

The block error rate and efficiency are given by the following expressions.

$$P_{block\_error}^{(3)} = \sum_{i=\lfloor R/2 \rfloor+1}^{K+R} \binom{K+R}{i} (P_{byte}^{parity})^i (1 - P_{byte}^{parity})^{K+R-i}$$

$$rate^{(3)} = \frac{8}{9} \frac{K}{(K+R)}$$

RS Code concatenated with (24,16) code

Let P_{byte1} and P_{byte2} denote the probabilities of one byte and two byte errors, respectively, when the inner code decoding fails. P_{byte1} and P_{byte2} are given by the following upper bounds

$$P_{byte1} < \sum_{d=d_{\min}}^{21} a_d Q\left(\sqrt{d \frac{C}{N}}\right)$$

$$P_{byte2} < \sum_{d=d_{\min}}^{21} b_d Q\left(\sqrt{d \frac{C}{N}}\right)$$

The weight distribution a_d and b_d for (24,16) code have been found using computer and are given in table 1 for d = d_{min} to d = d_{min}+5.

Table 01. Weight Distribution of (24,16) Code

d	d_{min} =3	4	5	6	7
a_d	8	24	56	76	84
b_d	0	10	112	460	1260

As found from the simulation and shown in the figure 2, the first two terms in the above summation is a good approximation for P_{byte1} and P_{byte2}. The block error rate and efficiency are given by the following expressions.

$$P_{block\_err}{}^{4} = \sum_{\substack{w+2x>t \\ w+x\le N \\ 0\le w,x\le N}} \binom{N}{w}\binom{N-w}{x} P_{byte1}{}^{w} P_{byte2}{}^{x} (1 - P_{byte1} - P_{byte2})^{N-w-x}$$

$$rate^{(4)} = \frac{2}{3}\frac{K}{N}$$

where t = floor(R/2), N = (K+ R)/2.

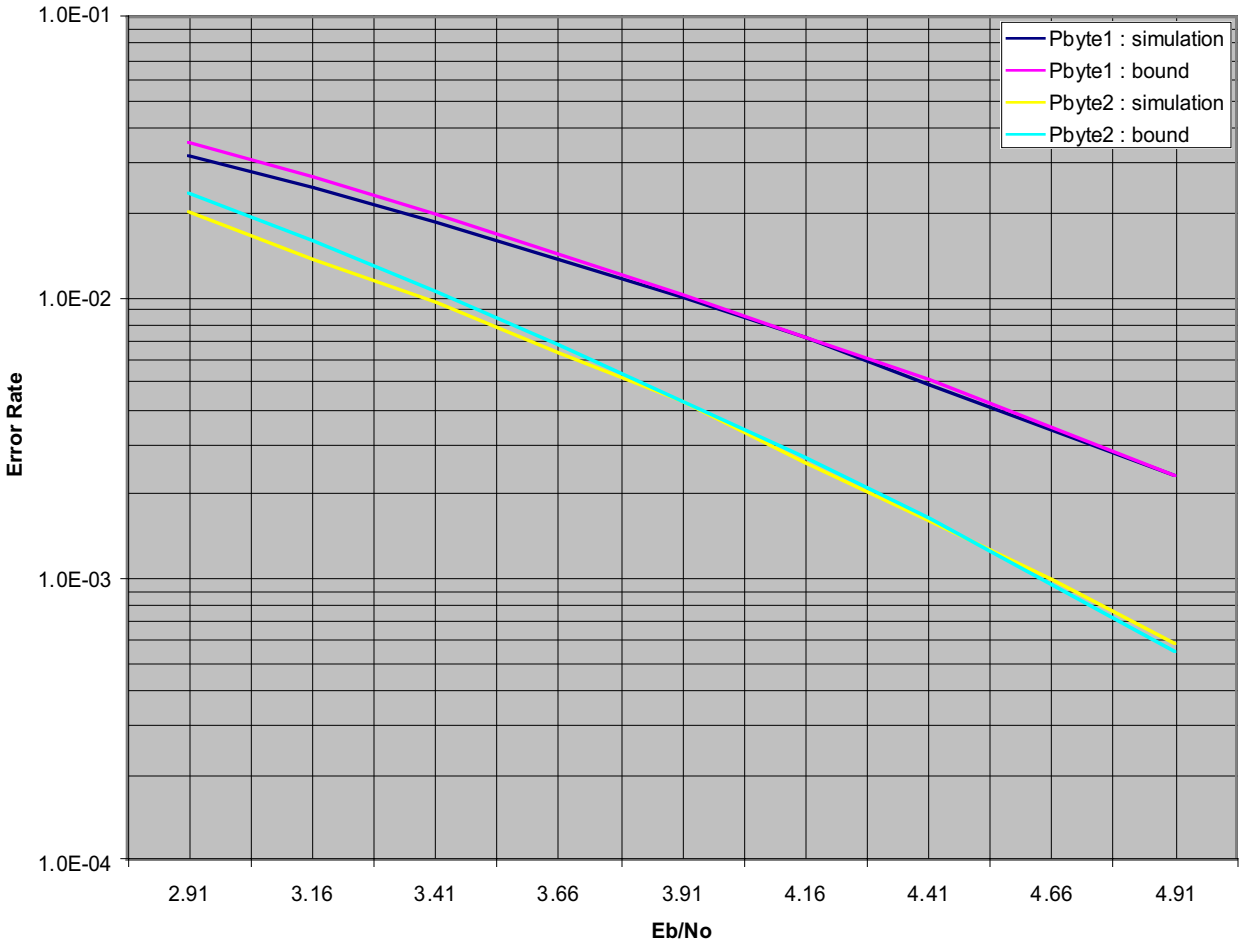


Figure 02. Error Performance of (24,16) Code with Soft Decoding for QPSK

RS Code Concatenated with (32,16) code

With the weight distribution given in table 02, the performance analysis of this scheme is identical to the previous scheme.

Table 02. Weight Distribution of (32,16) Code

d	$d_{min}=5$	6	7	8	9
a_d	16	26	40	56	64
b_d	0	6	24	74	256

As found from the simulation and shown in the figure 3, the first two terms in the summation is a good approximation for P_{byte1} and first three terms is a good approximation for P_{byte2}. The block error rate and efficiency are given by the following expressions.

$$P_{block\_err}^{\ 5} = \sum_{\substack{w+2x>t \\ w+x\le N \\ 0\le w,x\le N}} \binom{N}{w}\binom{N-w}{x} P_{byte1}^{\ w} P_{byte2}^{\ x} (1 - P_{byte1} - P_{byte2})^{N-w-x}$$

$$rate^{(5)} = \frac{1}{2}\frac{K}{N}$$

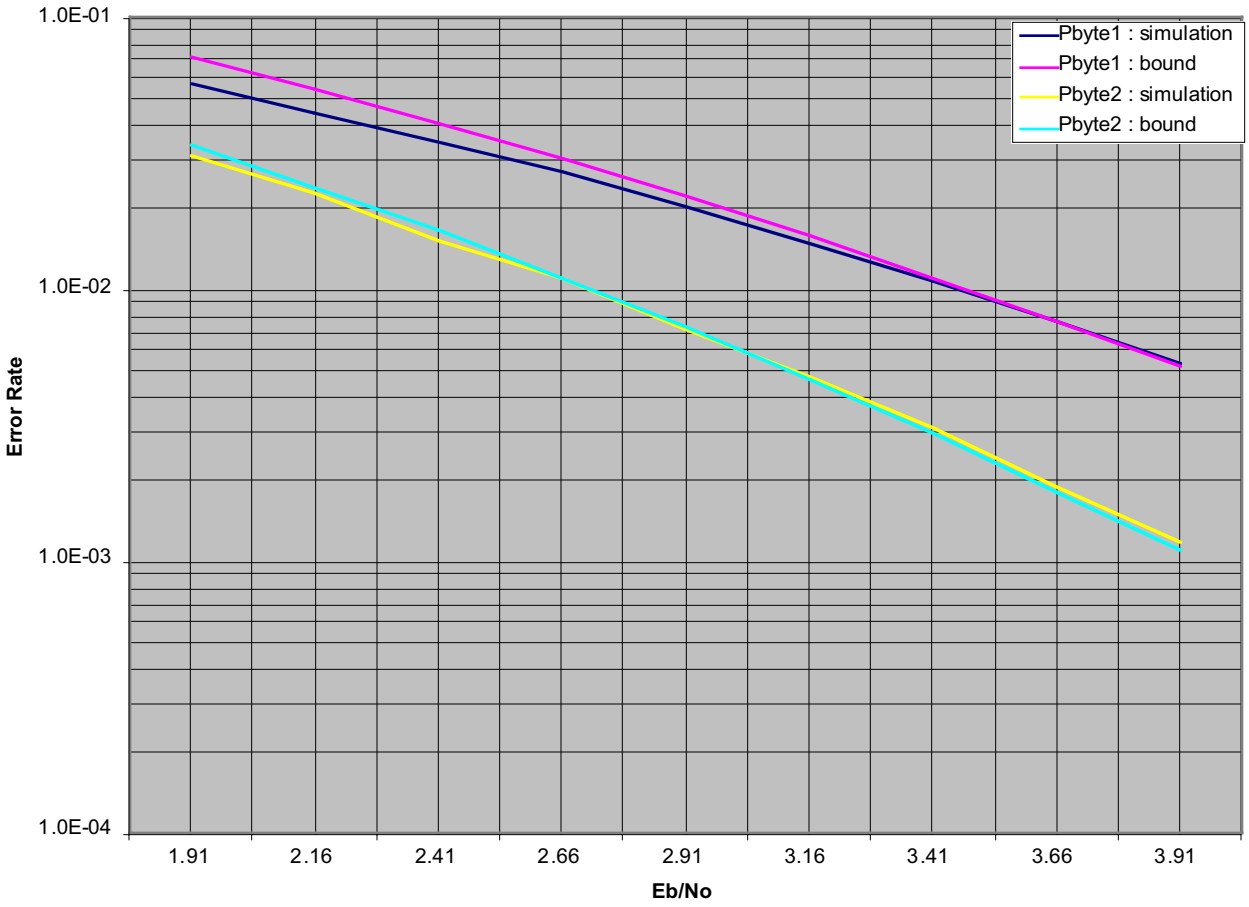
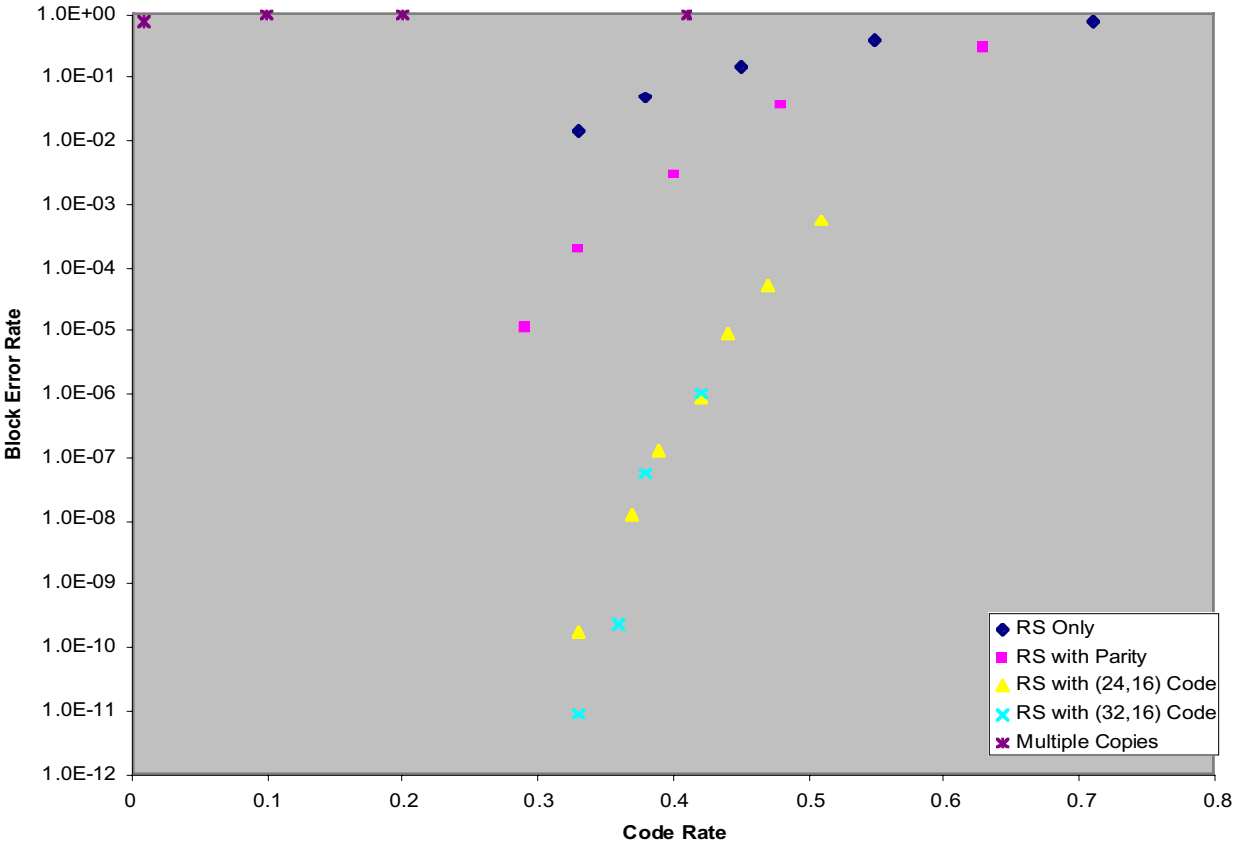


Figure 03. Error Performance of (32,16) Code with Soft Decoding for QPSK

The code rate Vs block error rate for K = 20 bytes, C/N = 5.45 dB is plotted is figure 4 for all of the above schemes. Both the options number (4) and (5) meet the performance requirements with reasonable code rate (around 0.33), with option number (5) being the best choice in terms of smaller RS decoding delay and better performance for the same rate. The miss-correction probability for this code is $1.27*10^{-7}$.



Conclusions And Recommendation

A RS code with 20 bytes of message concatenated with either (24,16) or (32,16) inner code meets specified block error rates requirements with decoding delay of less than a single block.

Although the (32,16) code is not included in the draft it uses the same hardware/software implementation and has slightly better performance. A 5 error correcting RS code concatenated with (32,16) inner code provides output block error rate of $8.95*10^{-12}$ with the aggregate code rate of 0.33 at the C/N of 5.45 dB. Also, the miss-correction probability of the code is $1.27*10^{-7}$, which is sufficiently low. Note that efficiency of the control channel coding scheme has a negligible effect on the overall efficiency as most of the bandwidth is consumed by user data.