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Title	Symbol clock requirements for the SS	
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Re:	Handling corrections to P802.16-REVd/D5	
Abstract	Errata to 802.16-2004	
Purpose	Correction of inconsistencies in 802.16-2004	
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Symbol clock requirements for the SS

1 Statement of the problem

According to 8.3.12, the SS must synchronize and lock to the BS with a maximum tolerance of 2% of the subcarrier spacing.

This requirement is sufficient in frequency, because such a frequency error brings little degradation, and subsequent frequency corrections can be commanded by the BS. A first issue is that the precision of the implementation of the frequency correction by the SS is not specified.

In terms of timing, this precision is not acceptable, because it could result in a drift of up to 16 samples per second in typical conditions (20 MHz bandwidth, 2.5 GHz carrier frequency), making numerous periodic rangings necessary (typically every 250 ms) to stay in the specified limit of ± 4 samples. Note that we assume in this calculation that the same relative correction is made on the sampling frequency clock (i.e. $\Delta T_s/T_s$) than on the carrier frequency (i.e. $\Delta f_{carrier}/f_{carrier}$), and that the 2% subcarrier spacing constraint applies to the carrier frequency.

2 Proposed solution

2.1 Application of a frequency correction

The BS must know what the precision of the SS is in terms of applying the frequency correction. We suggest 10 Hz as being a reasonable constraint on the SS.

2.2 Symbol clock frequency precision

The above example has shown that the existing requirement is not sufficient for proper operation of the system. We suggest specifying a maximum timing jitter of 1 sample for the SS over a period of 10 seconds, independently of the absolute error that will be corrected by the ranging process. Also, it should be specified that the precision of the applied command by the SS is 1 sample.

3 Specific text changes

In section 8.3.12, change the text as following:

At the BS, the transmitted center frequency, receive center frequency and the symbol clock frequency shall be derived from the same reference oscillator. At the BS the reference frequency tolerance shall be better than $\pm 8 \cdot 10^{-6}$ in licensed bands up to 10 years from the date of equipment manufacture.

At the SS, both the transmitted center frequency and the symbol clock frequency shall be synchronized and locked to the BS ~~with a tolerance of maximum 2% of the subcarrier spacing.~~ The maximum tolerance of the transmitted center frequency shall be 2% of the subcarrier spacing, and corrections shall be applied by the SS with a precision of 10 Hz. Clock timing error (with the mean error subtracted out) relative to the BS master clock must be less than 1 sampling time ($1/F_s$) over a 10-second measurement interval, and corrections shall be applied by the SS with a precision of 1 sampling time ($1/F_s$).

For Mesh capable devices, all device frequencies shall be accurate to within $\pm 20 \times 10^{-6}$ and achieve synchronization to its neighboring nodes with a tolerance of maximum 3% of the subcarrier spacing.

During the synchronization period, the SS shall acquire frequency [and timing](#) synchronization within the specified tolerance before attempting any uplink transmission. During normal operation, the SS shall track the frequency changes and shall defer any transmission if synchronization is lost.

All SSs shall acquire and adjust their timing such that all uplink OFDM symbols arrive time coincident at the Base-Station to a accuracy of $\pm 50\%$ of the minimum guard-interval or better.