Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**Algebraic Low-Density Parity-Check Codes for OFDMA PHY Layer**
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Source(s):	Nina Burns, Aleksandar Purkovic, Sergey Sukobok, Brian Johnson Nortel Networks 20410 Century Blvd Gaithersburg, MD 20874 USA Voice: 1-301-528-3255 Fax: 1-301-528-3298 nburns@nortelnetworks.com
Re:	Contribution in conjunction with comments to IEEE 802.16e
Abstract	This contribution describes construction and encoding of optional LDPC codes for 802.16e OFDMA
Purpose	Support of the comments
Notice	
Release	
Patent Policy and Procedures	

Note to editor: add the following sections and text adjusting the numbering as required. The appendix of this document is not part of the text proposal.

8.4.9.2.4 Algebraic Low-Density Parity-Check Code (optional)

This document describes Nortel Networks' contribution towards inclusion of Low-Density Parity-Check (LDPC) codes in the 802.11e standard.

We describe a particular algebraic construction of a parity check matrix which specifies the LDPC code and outline the encoding procedure for such codes. Frame Error Rate (FER) results are also included for comparison purposes. In addition, we discuss the potential benefits that a structured code may have in hardware implementation.

8.4.9.2.4.1 LDPC Parity Check Matrix Description

8.4.9.2.4.1.1 Base Parity Check Matrix Specification

The LDPC matrix is constructed in two steps, based on the information block size (K) and desired code rate, R=K/N, where N equals the codeword length. In the first step the base matrix is generated whereas in the second step the base matrix is expanded, if necessary.

The base LDPC matrix has the size MxN, where M is the number of check equations, and can be represented in the form:

$$H = [H^p \mid H_1^d \mid H_2^d \mid H_3^d]$$

All of the component sub-matrices, H^p, H_1^d, H_2^d, H_3^d are square matrices of the size MxM. The modular structure of this matrix is used to generate codes with a series of code rates: 1/2, 2/3 and 3/4. This is illustrated below, where only a portion of the whole matrix is used (outlined in bold letters) for rates less than 3/4:

R = 1/2: $\boldsymbol{H} = [\boldsymbol{H}^{\boldsymbol{p}} | \boldsymbol{H}_{\boldsymbol{1}}^{\boldsymbol{d}} \mid H_2^d \mid H_3^d]$

R = 2/3: $\boldsymbol{H} = [\boldsymbol{H}^{\boldsymbol{p}} | \boldsymbol{H}_{\boldsymbol{1}}^{\boldsymbol{d}} \mid \boldsymbol{H}_{\boldsymbol{2}}^{\boldsymbol{d}} \mid H_3^d]$

R = 3/4: $\boldsymbol{H} = [\boldsymbol{H}^{\boldsymbol{p}} | \boldsymbol{H}_{\boldsymbol{1}}^{\boldsymbol{d}} \mid \boldsymbol{H}_{\boldsymbol{2}}^{\boldsymbol{d}} \mid \boldsymbol{H}_{\boldsymbol{3}}^{\boldsymbol{d}}]$

Matrix H^p is in a "dual diagonal" form. There is always only one sub-matrix H^p in the parity check matrix H, corresponding to the parity check bits of the codeword.

Matrices H_i^d, $i = 1,2,3$ are constructed by using a modification of the π-rotation technique, originally described in [1]. Each of the matrices H_i^d can be represented in the following form:

$$\boldsymbol{H}_{\boldsymbol{i}}^{\boldsymbol{d}} = \begin{bmatrix} \pi_{A,i}\pi_{B,i}\pi_{C,i}\pi_{D,i} \\ \pi_{B,i}\pi_{C,i}\pi_{D,i}\pi_{A,i} \\ \pi_{C,i}\pi_{D,i}\pi_{A,i}\pi_{B,i} \\ \pi_{D,i}\pi_{A,i}\pi_{B,i}\pi_{C,i} \end{bmatrix} \boldsymbol{i} = 1,2,3$$

Figure 1. Structure of the matrix H_i^d

$\pi_{A,i}$ is a 24x24 permutation matrix. $\pi_{B,i}, \pi_{C,i}$, and $\pi_{D,i}$ are obtained by 90°, 180°, and 270° counterclockwise rotations of the permutation matrix $\pi_{A,i}$, respectively. The variable m=24 is used to describe the size of the permutation matrices. It follows that 4m=M.

As one can see, each H_i^d is fully specified by $\pi_{A,i}$ which in turn is described by a length-24 vector. Therefore the entire LDPC matrix is fully specified by three length-24 vectors from which the component sub-matrices are generated:

A,1 = *[6 5 10 24 8 7 17 23 11 12 22 2 14 18 15 4 19 21 20 1 9 16 13 3]*

A,2 = *[20 19 24 5 9 7 17 12 4 13 21 11 15 23 16 8 6 14 2 10 22 3 18 1]*

A,3 = *[21 19 7 3 11 14 20 4 18 13 5 23 16 12 22 10 9 6 8 17 1 24 2 15]*

Mapping between the permutation vector ***A,i*** and the permutation matrix $\pi_{A,i}$ is as follows: the first element of the row vector ***A,i*** specifies the position of a "1" in the first column of $\pi_{A,i}$, (counting from the bottom), the second element of the row vector ***A,i*** specifies the position of a "1" in the second column of $\pi_{A,i}$, and so on. An example of deriving the permutation matrix $\pi_{A,1}$ from the vector ***A,1*** is shown in Figure 2. The matrices $\pi_{A,2}$ and $\pi_{A,3}$ are derived in a similar manner and rotated to form the corresponding $\pi_{B,i}$, $\pi_{C,i}$ and $\pi_{D,i}$ matrices (i=2,3). These matrices are concatenated as explained previously to form the base matrix.

$\pi_{A,1} =$

0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Figure 2. Structure of the matrix $\pi_{A,1}$

8.4.9.2.4.1.2 Expansion of the Base Parity Check Matrix

If there is a need to accommodate a larger block size, the base parity check matrix may be expanded by an integer factor *L*, where *L* is an integer between 1 and 12.

Expansion of H^p is done by replacing each "0" element by an *L*x*L* zero matrix, $\mathbf{0}_{LxL}$, and each "1" element by an *L*x*L* identity matrix, $\mathbf{I}_{LxL}$.

Expansion of $\boldsymbol{H}^{\boldsymbol{d}}$ is done by replacing each "0" element by an *L*x*L* zero matrix, $\mathbf{0}_{LxL}$, and each "1" element by a rotated version of an *L*x*L* identity matrix, $\mathbf{I}_{LxL}$. The rotation order, *s* (number of circular shifts to the right, for example) can be determined by using a simple rule: $s = (r * c)_{\text{mod } L}$, where *r* and *c* correspond to the row and column index of the particular "1" element, respectively. Row indices, r, are in the range [1,M] and column indices, c, are in the range [M+1,N].

8.4.9.2.4.2 Encoding

The described structure of the LDPC parity check matrix enables a simple encoding algorithm. In general, by the definition of the parity check matrix, the following holds:

$\mathbf{H}_{MxN}\mathbf{c}_{Nx1}=\mathbf{0}_{Mx1}$,

where **H** is the parity check matrix, $\mathbf{0}_{Mx1}$, an all-zero Mx1 vector, and **c** is a codeword vector given by:

$\mathbf{c} = [p_1,p_2,\ldots,p_M,d_1,d_2,\ldots,d_K]^T$

In the expression above, $p_1,p_2,\ldots,p_M$ represent parity bits (redundancy part) whereas $d_1,d_2,\ldots,d_K$ represent information bits (systematic part). Due to the dual diagonal structure of the sub-matrix H^p, parity bits can be computed recursively as:

$p_M = \sum_{n=1}^{4q} h_{M,M+k_n^M} d_{k_n^M}$, where $\mathrm{M}+k_n^M$ is the index of the column in which row M contains a "1"

$p_{M-1} = p_M + \sum_{n=1}^{4q} h_{M-1,M+k_n^{M-1}} d_{k_n^{M-1}}$, where $\mathrm{M}+k_n^{M-1}$ is the index of the column in which row M-1 contains a "1"

…

$p_1 = p_2 + \sum_{n=1}^{4q} h_{1,M+k_n^1} d_{k_n^1}$, where $\mathrm{M}+k_n^1$ is the index of the column in which row 1 contains a "1"

where $\boldsymbol{k}_{\boldsymbol{n}}^1, \boldsymbol{k}_{\boldsymbol{n}}^2, \ldots, \boldsymbol{k}_{\boldsymbol{n}}^{\boldsymbol{M-1}}, \boldsymbol{k}_{\boldsymbol{n}}^{\boldsymbol{M}}$ and $h_{r,c}$ are non-zero elements (=1) of the parity check matrix in the portion corresponding to H_i^d's. Therefore, the encoding operation can be performed by using only simple AND and XOR circuits.

For the cases when the information block size is greater than 144, 192 and 216 bytes for R=1/2, 2/3 and 3/4, respectively, concatenation of the code words is employed. Based on the rate and number of information bytes to be sent, the required number of code words is calculated. The amount of zero padding (or shortening) is divided as equally as possible among the total number of code word blocks. This way, each code word block has the same effective rate that approaches the desired rate.

Appendix A

A.1 Performance

In this section we present our simulation results obtained using the consensus criteria: AWGN channel, BPSK modulation, using a generic floating point sum-product decoding with a maximum of 50 iterations. Results are presented for rates 1/2, 2/3, and 3/4. For each rate, results for all supported block lengths are presented. Table 1 summarizes the supported rates and block lengths.

LDPC code block size support

N: encoder output
Nsch: number of subchannels to be mapped
K: encoder input (bytes)

QPSK (N in bits is a multiple of 48x2)

N (bytes)	N (bits)	Nsch	K (R=1/2)	K (R=2/3)	K (R=3/4)	Expansion factor L		
24	192	2	12	16	18	1		
36	288	3	18	24	27		1	
48	384	4	24	32	36	2		1
60	480	5	30	40	45			
72	576	6	36	48	54	3	2	
84	672	7	42	56	63			
96	768	8	48	64	72	4		2
108	864	9	54	72	81		3	
120	960	10	60	80	90	5		
132	1056	11	66	88	99			
144	1152	12	72	96	108	6	4	3
156	1248	13	78	104	117			
168	1344	14	84	112	126	7		
180	1440	15	90	120	135		5	
192	1536	16	96	128	144	8		4
204	1632	17	102	136	153			
216	1728	18	108	144	162	9	6	
228	1824	19	114	152	171			
240	1920	20	120	160	180	10		5
252	2016	21	126	168	189		7	
264	2112	22	132	176	198	11		
276	2208	23	138	184	207			
288	2304	24	144	192	216	12	8	6

16-QAM (N in bits is a multiple of 48x4)

N (bytes)	N (bits)	Nsch	K (R=1/2)	K (R=2/3)	K (R=3/4)			
24	192	1	12	16	18	1		
48	384	2	24	32	36	2		1
72	576	3	36	48	54	3	2	
96	768	4	48	64	72	4		2
120	960	5	60	80	90	5		
144	1152	6	72	96	108	6	4	3
168	1344	7	84	112	126	7		
192	1536	8	96	128	144	8		4
216	1728	9	108	144	162	9	6	
240	1920	10	120	160	180	10		5
264	2112	11	132	176	198	11		
288	2304	12	144	192	216	12	8	6

64-QAM (N in bits is a multiple of 48x6)

N (bytes)	N (bits)	Nsch	K (R=1/2)	K (R=2/3)	K (R=3/4)			
36	288	1	18	24	27		1	
72	576	2	36	48	54	3	2	
108	864	3	54	72	81		3	
144	1152	4	72	96	108	6	4	3
180	1440	5	90	120	135		5	
216	1728	6	108	144	162	9	6	
252	2016	7	126	168	189		7	
288	2304	8	144	192	216	12	8	6

Table 1. Supported information lengths and rates. The shaded portions of the leftmost table correspond to the lengths and rates that are required for comparison. The lighter shaded portions of the center table correspond to the combinations supported by the proposed code. The darker shaded portions of the center table indicate the overlap between the left and right tables. The rightmost table shows which expansion factor was applied.

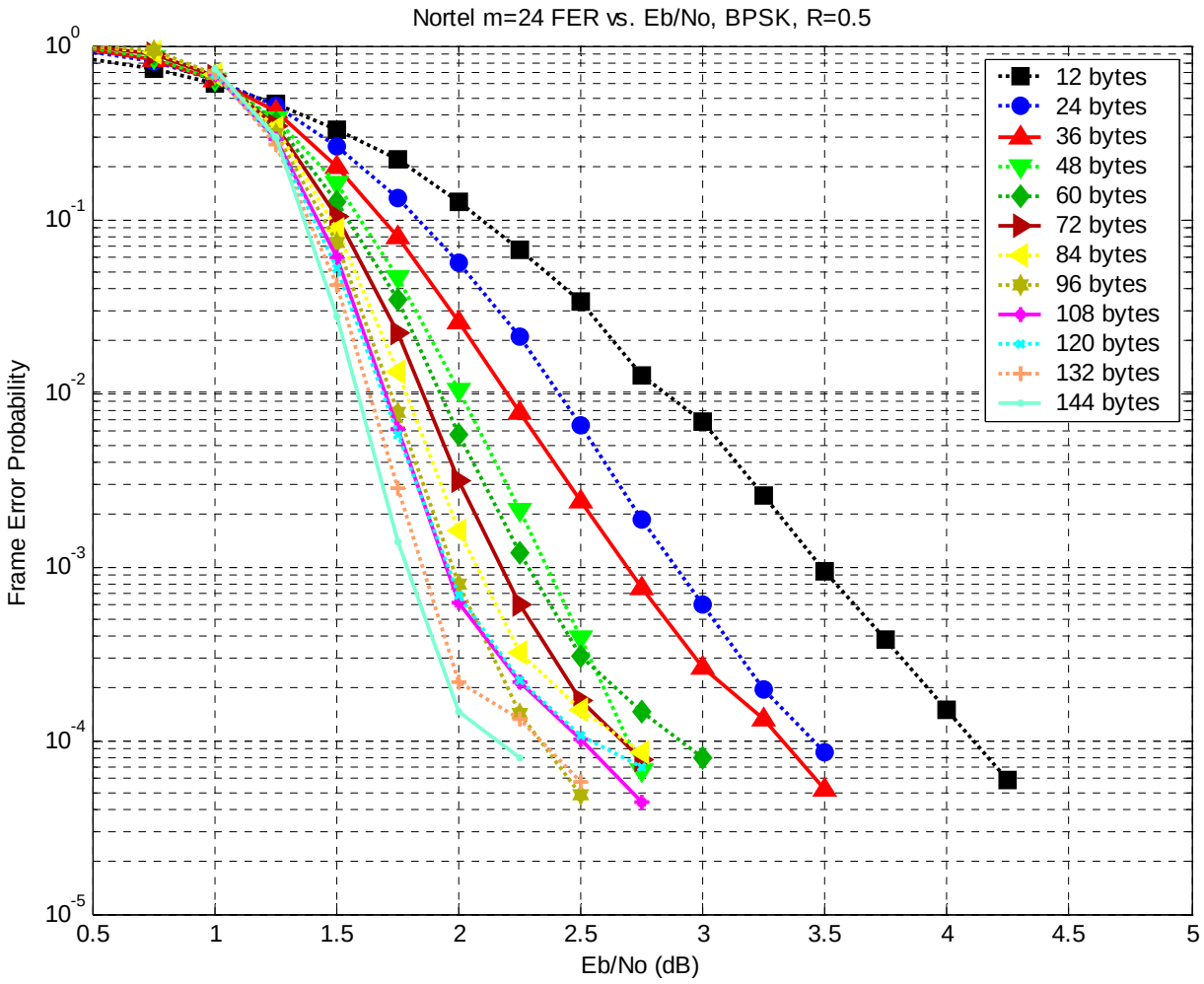


Figure 3. FER vs. Eb/No, AWGN R=1/2. Information lengths are in bytes.

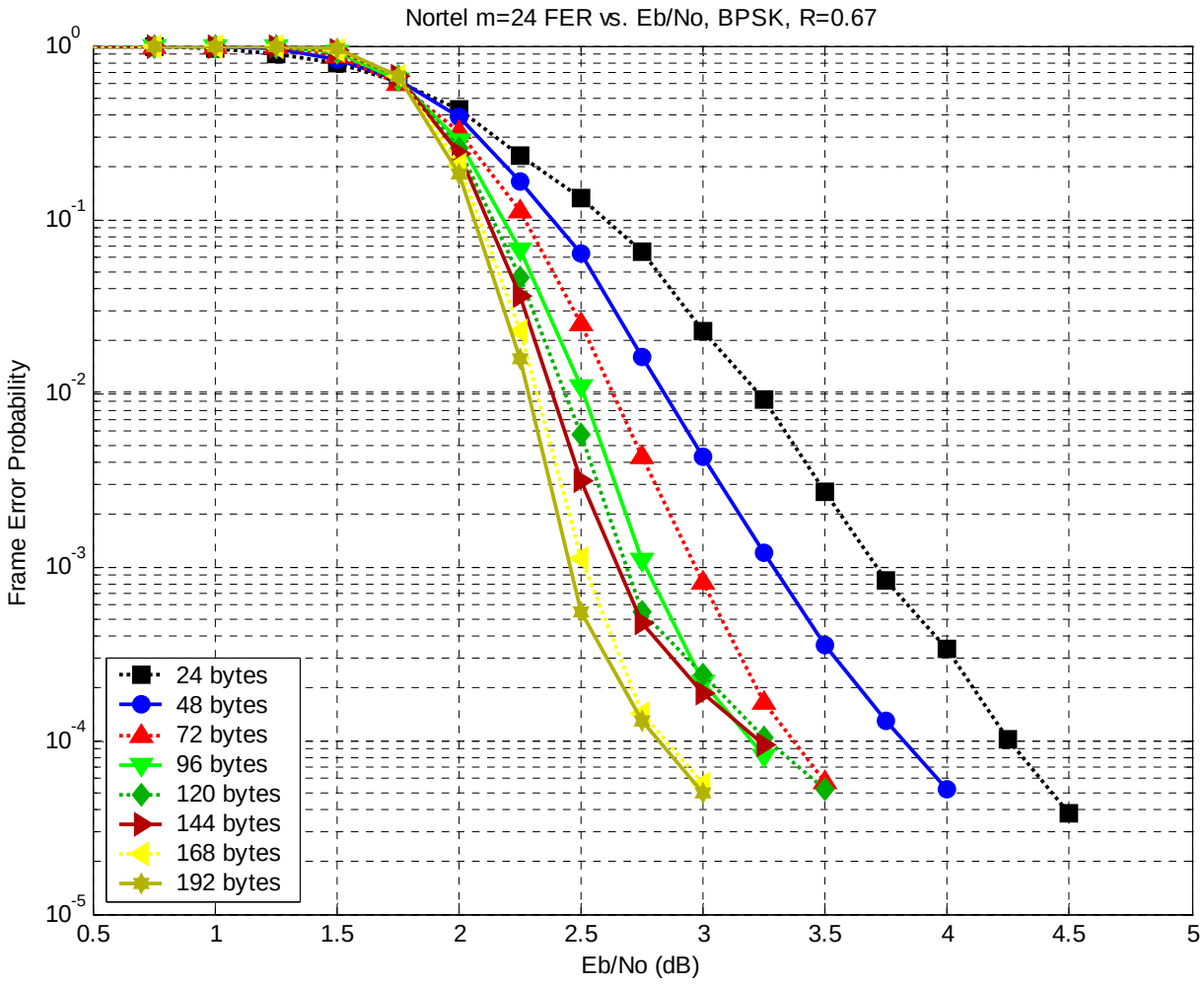


Figure 4. FER vs. Eb/No, AWGN R=2/3. Information lengths are in bytes.

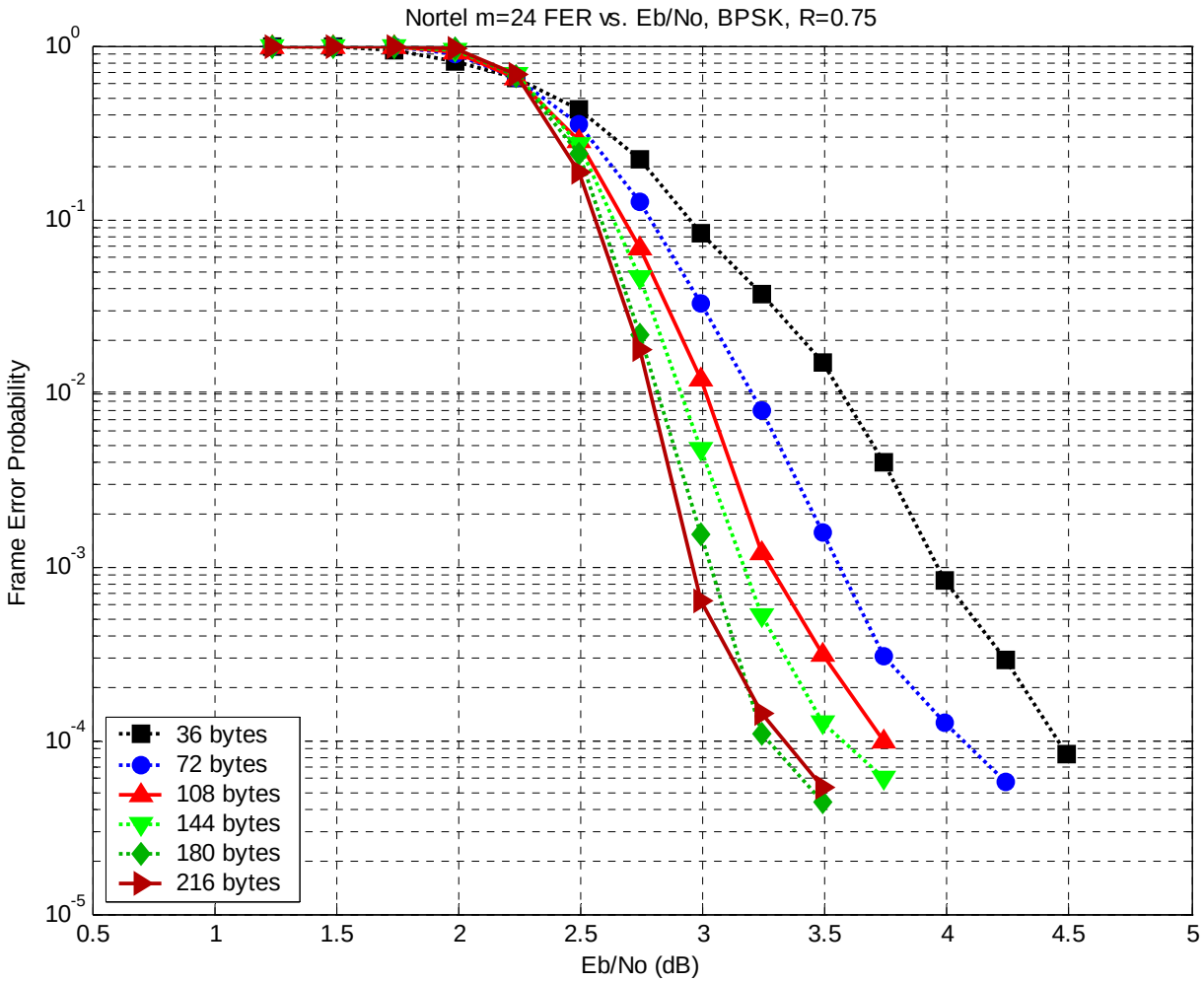


Figure 5. FER vs. Eb/No, AWGN R=3/4. Information lengths are in bytes.

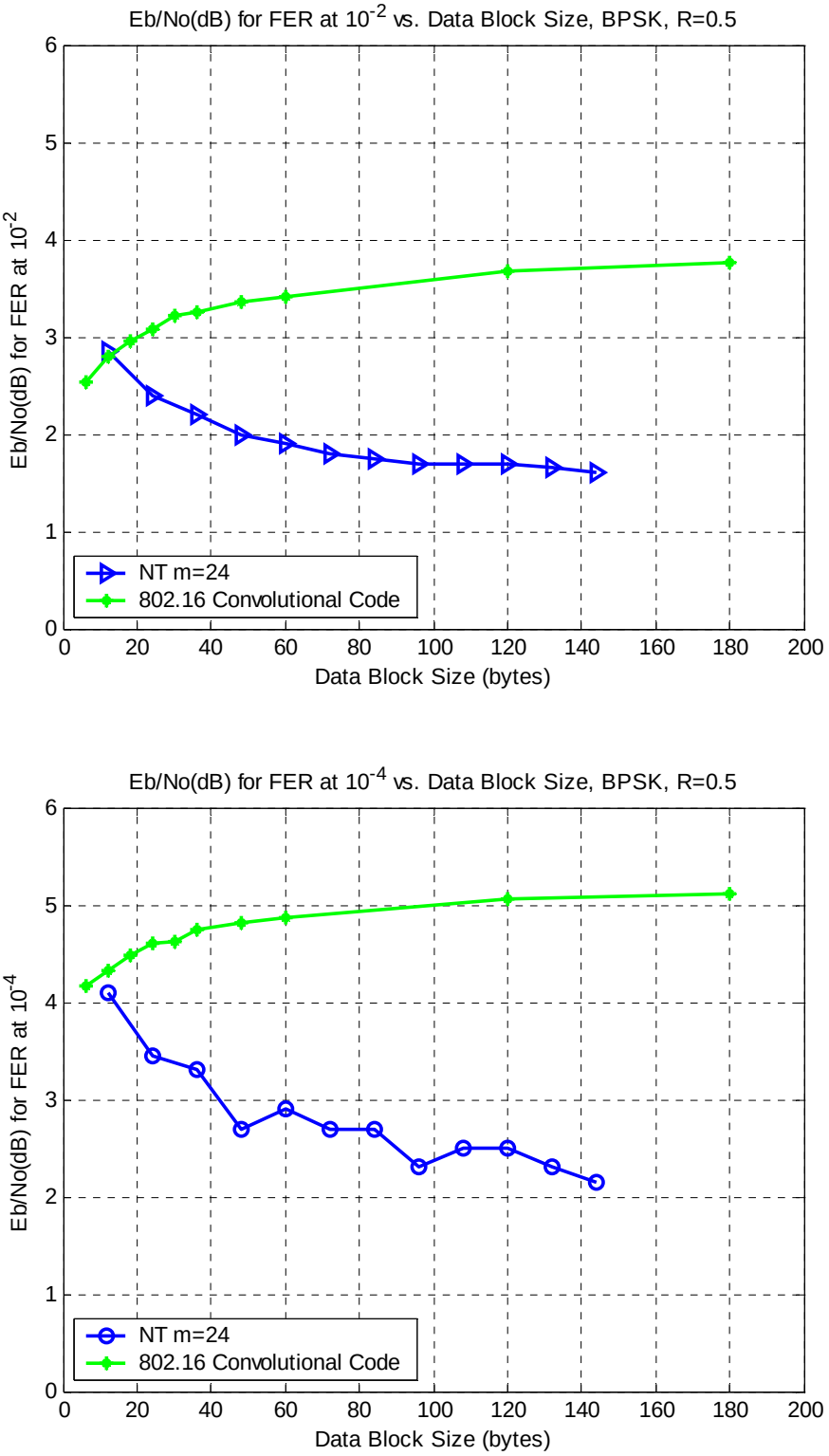


Figure 6. SNRs for FER=10^{-2} and 10^{-4} vs. information length, R=0.5

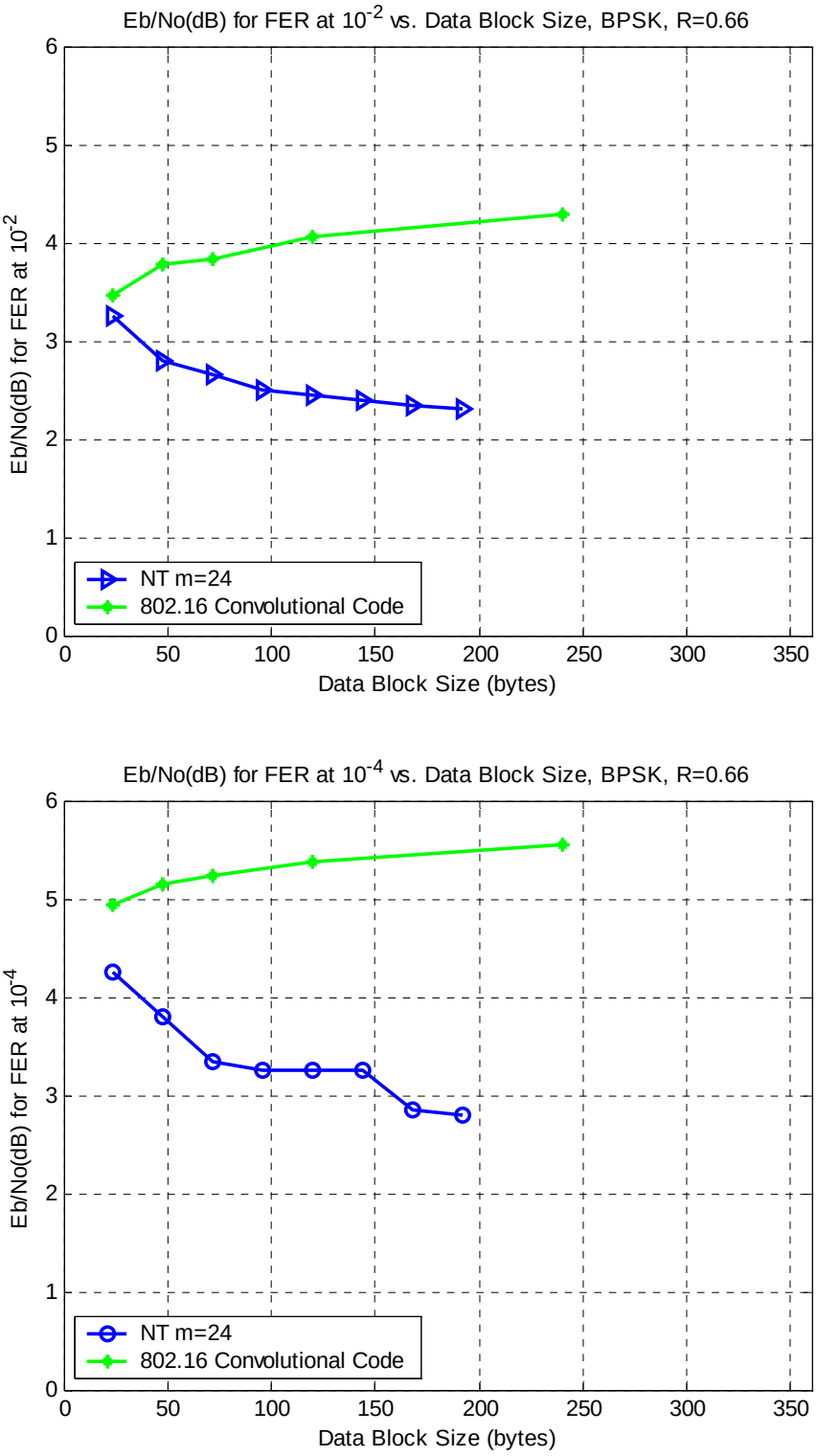
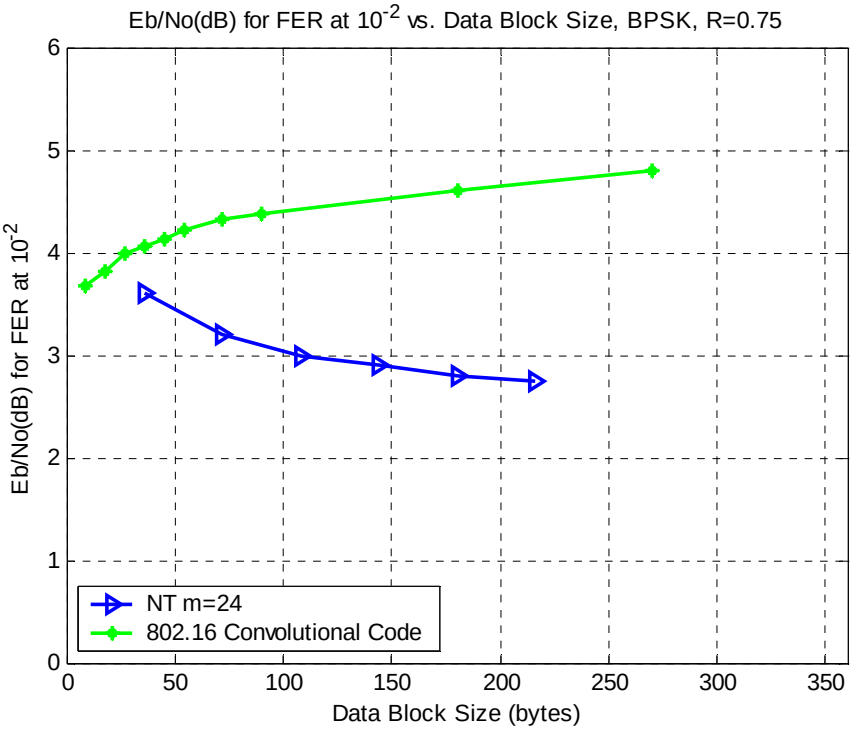


Figure 7. SNRs for FER=10^{-2} and 10^{-4} vs. information length, R=0.66



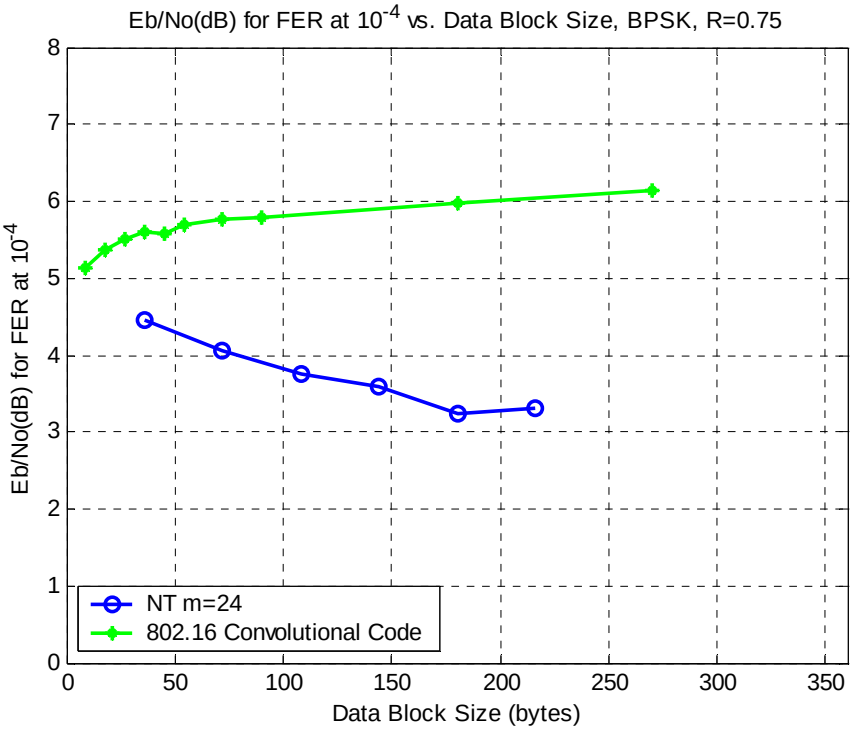


Figure 8. SNRs for FER=10^{-2} and 10^{-4} vs. information length, R=0.75

A.2 Hardware Implementation Considerations

The main features of the proposed LDPC code are its performance *and* its deterministic structure. In general randomized, irregular matrices outperform regular, structured matrices [2]. But with careful design and searching, we have found codes with competitive performance that also lend themselves to simpler hardware implementations. Specifically, the construction based on permutation matrices reduces the wiring and routing requirements. In addition, the pi-rotation structure offers the following:

- further simplified encoding circuits
- more straightforward fixed-point implementation
- possibility of hardware re-use among portions of the matrix

The following is a description of the encoder and decoder hardware simplifications.

A.2.1 Encoder Complexity Reduction

This technique was first described in [1] and we describe it here for ½-rate matrices for simplicity. The codeword $\boldsymbol{c}$ can be represented in systematic form corresponding to the parity check matrices as $\boldsymbol{c}=[\boldsymbol{p} \mid \boldsymbol{d}]$ and consists of the parity vector $\boldsymbol{p}$ and the source vector $\boldsymbol{d}$. Assuming a systematic code we define projection vector $\boldsymbol{v}$ from the equations below.

$$\boldsymbol{H}^{p} \cdot \boldsymbol{p} = \boldsymbol{H}^{d} \cdot \boldsymbol{d} = \boldsymbol{v} \qquad \text{(A.2.1)}$$

Now the encoding process can be split into two steps:

- Calculation of the projection vector
- Calculation of the parity bits

Note that once the projection vector is calculated, the parity bits are computed using the back-substitution method. Representing the information vector $\boldsymbol{d}$ as four sub-vectors (or segments of length $m=24$) $\boldsymbol{[d_1\ d_2\ d_3\ d_4]}$, we can write the following equation:

$$\begin{bmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \\ \boldsymbol{v}_3 \\ \boldsymbol{v}_4 \end{bmatrix} = \begin{bmatrix} \pi_{\mathrm{A}} & \pi_{\mathrm{B}} & \pi_{\mathrm{C}} & \pi_{\mathrm{D}} \\ \pi_{\mathrm{B}} & \pi_{\mathrm{C}} & \pi_{\boldsymbol{D}} & \pi_{\mathrm{A}} \\ \pi_{\mathrm{C}} & \pi_{\mathrm{D}} & \pi_{\mathrm{A}} & \pi_{\mathrm{B}} \\ \pi_{\mathrm{D}} & \pi_{\mathrm{A}} & \pi_{\mathrm{B}} & \pi_{\mathrm{C}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{d}_1 \\ \boldsymbol{d}_2 \\ \boldsymbol{d}_3 \\ \boldsymbol{d}_4 \end{bmatrix} \qquad \text{(A.2.2)}$$

Now we can derive an equation for each segment of $\boldsymbol{v}$ as follows:

$$\begin{aligned} \boldsymbol{v}_1 &= \pi_{\boldsymbol{A}} * \boldsymbol{d}_1 + \pi_{\boldsymbol{B}} * \boldsymbol{d}_2 + \pi_{\boldsymbol{D}} * \boldsymbol{d}_3 + \pi_{\boldsymbol{C}} * \boldsymbol{d}_4 \\ \boldsymbol{v}_2 &= \pi_{\boldsymbol{B}} * \boldsymbol{d}_1 + \pi_{\boldsymbol{C}} * \boldsymbol{d}_2 + \pi_{\boldsymbol{D}} * \boldsymbol{d}_3 + \pi_{\boldsymbol{A}} * \boldsymbol{d}_4 \\ \boldsymbol{v}_3 &= \pi_{\boldsymbol{C}} * \boldsymbol{d}_1 + \pi_{\boldsymbol{D}} * \boldsymbol{d}_2 + \pi_{\boldsymbol{A}} * \boldsymbol{d}_3 + \pi_{\boldsymbol{B}} * \boldsymbol{d}_4 \\ \boldsymbol{v}_4 &= \pi_{\boldsymbol{D}} * \boldsymbol{d}_1 + \pi_{\boldsymbol{A}} * \boldsymbol{d}_2 + \pi_{\boldsymbol{B}} * \boldsymbol{d}_3 + \pi_{\boldsymbol{C}} * \boldsymbol{d}_4 \end{aligned} \qquad \text{(A.2.3)}$$

The projection vector can then be calculated by sequentially shifting the info sub-segments d_i clockwise around a single permutation matrix. Figure 9 depicts this in a diagram.

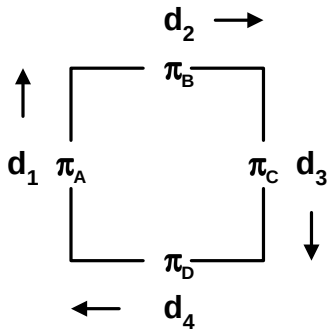


Figure 9. Description of π-rotation encoding.

The circuit complexity is reduced by using the symmetries of the π–rotation structure. The efficiency of the encoding process can be increased using a pipelined encoder architecture.

A.2.2 Decoder Complexity Reduction

The challenges in implementation of a sum-product decoder lie in the circuit representation of the parity check matrix. A fully randomized parity check matrix must incorporate a wiring network that can connect any bit node to any check node and vice-versa. However, a parity matrix built from permutation matrices such as the one we propose can reduce the complexity of the interconnect by *O(n)* [3]. Let m represent the square size of permutation matrices, as in our proposed code. Since each row of the permutation matrices $H_{d,i}$ has a single nonzero element, only m:1 instead of N:1 multiplexers are needed to implement connectivity. This is also true for the de-multiplexers in the reverse direction.

The pi-rotation structure of our matrix consists of repeated permutation matrices within individual $H_{d,i}$'s (Figure 10). We suggest that this repetition may be an advantage when designing circuitry for implementation.

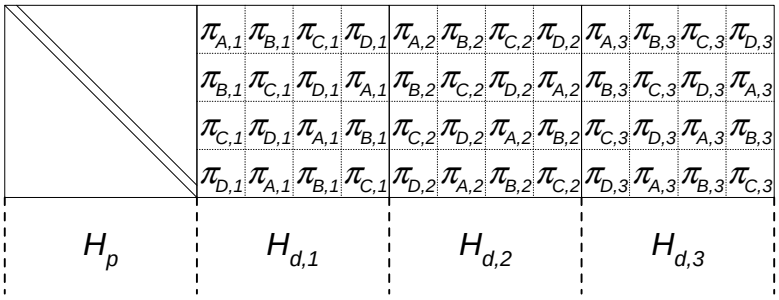


Figure 10. Diagram of parity check matrix showing repeated permutation matrices in its structure.

Also noteworthy is the regular row and column weights of our proposed matrix. With the exception of 1 row and column in our base matrix, all column weights are 2 or 4 and all row weights are 6 (for the ½ rate code). The sum-product algorithm requires summations over the number of column and row weights. If the number of addends vary widely, the circuitry must use wider accumulators to prevent overflow for those cases. Having a limited number row and column weights allows for a more efficient and straightforward implementation.

A.3 References

[1] R. Echard et al, “The π-rotation low-density parity check codes,” In Proc. GLOBECOM 2001, pp. 980-984, Nov. 2001.
[2] T. J. Richardson, M. A. Shokrollahi and R. L. Urbanke, “Design of Capacity-Approaching Irregular Low-Density Parity Check Codes”,IEEE Trans. Info. Theory, Vol. 47, No. 2, February 2001.
[3] M.M.Mansour and N.R.Shanbhag, “High-Throughput LDPC Decoders,” IEEE Trans. On VLSI Systems, vol. 11, No 6, pp. 976-996, December 2003.

A.4 Informative Example

The following matrix description is provided as a construction reference. The matrix is in the standard distribution format and represents the proposed matrix (R=3/4) with expansion factor L=2.

```
768 192
1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
2 2 2 2 2 2 2 2 2 2 2 2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
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