

Project	<b>IEEE 802.16 Broadband Wireless Access Working Group</b> < <a href="http://ieee802.org/16">http://ieee802.org/16</a> >	
Title	<b>Correction of inconsistencies for 802.16e D5 OFDMA symbol clock frequency tolerance</b>	
Date Submitted	<b>2004-11-04</b>	
Source(s)	Juergen Otterbach Joerg Schaepperle Roland Muenzner Torsten Fahldieck Alcatel SEL AG	Voice: +49-711-821-32255 Fax: +49-711-821-32453 <a href="mailto:juergen.otterbach@alcatel.de">juergen.otterbach@alcatel.de</a>
Re:	802.16e D5 September 2004	
Abstract	Correction of inconsistencies for 802.16e D5 OFDMA	
Purpose	Modification of symbol clock tolerances for OFDMA in 802.16e-D5	
Notice	This document has been prepared to assist IEEE 802.16. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.	
Release	The contributor grants a free, irrevocable license to the IEEE to incorporate material contained in this contribution, and any modifications thereof, in the creation of an IEEE Standards publication; to copyright in the IEEE's name any IEEE Standards publication even though it may include portions of this contribution; and at the IEEE's sole discretion to permit others to reproduce in whole or in part the resulting IEEE Standards publication. The contributor also acknowledges and accepts that this contribution may be made public by IEEE 802.16.	
Patent Policy and Procedures	The contributor is familiar with the IEEE 802.16 Patent Policy and Procedures < <a href="http://ieee802.org/16/ipr/patents/policy.html">http://ieee802.org/16/ipr/patents/policy.html</a> >, including the statement "IEEE standards may include the known use of patent(s), including patent applications, provided the IEEE receives assurance from the patent holder or applicant with respect to patents essential for compliance with both mandatory and optional portions of the standard." Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair < <a href="mailto:chair@wirelessman.org">mailto:chair@wirelessman.org</a> > as early as possible, in written or electronic form, if patented technology (or technology under patent application) might be incorporated into a draft standard being developed within the IEEE 802.16 Working Group. The Chair will disclose this notification via the IEEE 802.16 web site < <a href="http://ieee802.org/16/ipr/patents/notices">http://ieee802.org/16/ipr/patents/notices</a> >.	

# Correction of inconsistencies in 802.16e D5 OFDMA symbol clock frequency tolerance

Juergen Otterbach / Joerg Schaepperle / Roland Muenzner / Torsten Fahldieck  
Alcatel SEL AG

## 1 Statement of the problem

In section 8.4.14.1 "Center frequency and symbol clock frequency tolerance" of IEEE802.16-2004 it is stated that the symbol clock frequency of the subscriber station (SS) "shall be synchronized to the BS with a tolerance of maximum 2% of the subcarrier spacing". This specification is misleading.

The subcarrier spacing is defined as follows:

$$\Delta f = F_s / N_{FFT}$$

$$\text{with } F_s = \text{floor}(n * BW / 8000) * 8000$$

$$F_s = \text{sampling frequency, } n = \text{sampling factor} = \frac{8}{7}, BW = \text{nominal channel bandwidth}$$

$$\text{and } N_{FFT} = \text{number of points for FFT}$$

In the case of  $BW = 10 \text{ MHz}$ ,  $N_{FFT} = 1024$ , a subcarrier spacing of

$$\Delta f = \text{floor}(n * BW / 8000) * 8000 \div N_{FFT} = 11.156 \text{ kHz}$$

results. Two percent of this value corresponds to 223.1 Hz.

According to this tolerance the SS is allowed to transmit OFDMA symbols with differences in duration as shown in Figure 1 where a Cyclic Prefix (CP) time of 1/4 of the "useful" symbol time is assumed. The symbol time extension by the CP is  $1024/4 = 256$  samples. The whole symbol is equivalent to 1280 samples that correspond to  $T_s = 112.044 \mu\text{sec}$  nominal.

nominal symbol duration of 112.044μsec maximum symbol duration of 114.285μsec minimum symbol duration of 111.799μsec



Figure 1: Possible differences in the OFDMA symbol duration

An UL OFDMA symbol with maximum symbol duration of  $114.285 \mu\text{sec}$  is  $2.241 \mu\text{sec}$  longer than the expected 1280 samples with nominal  $112.044 \mu\text{sec}$  which corresponds to 25.6 samples. A performance degradation in the OFDMA receiver will result.

## 2 Estimation of the Required Frequency Accuracy

A mismatch of the sampling frequencies of different SSs causes interference between subcarriers due to different subcarrier spacings. Assuming that

- the frequency synchronization removes the frequency offset at the center frequency

- all subcarriers except the distorted one are interferers and have the same sampling frequency offset (worst case scenario)
- the distorted subcarrier is either that with the highest or that with the lowest frequency (worst case due to highest frequency offset at that positions)
- data on different subcarriers are uncorrelated

the worst case signal-to-interference ratio (SIR) due to this sampling frequency mismatch can in good correspondence with simulations be approximated by the expression

$$\text{SIR} = 10 \log \frac{24}{\pi^2 \delta^2} \text{ dB}$$

where  $\delta$  is the absolute sampling frequency error divided by the subcarrier spacing. This relationship is shown in Figure 2.

A tolerance for the sampling clock will be transformed to a symbol clock accuracy. The relation between sampling frequency and OFDM symbol clock ( $1/T_s$ ) is given by the following formula depending on the applied FFT size:

$$\frac{1}{T_s} = \frac{1}{(1+G) \cdot N_{FFT}} \cdot F_s$$

The specified cyclic prefix values  $G$  are 1/4, 1/8, 1/16 and 1/32. Worst case for this consideration is the maximum CP duration ( $G= 1/4$ ) resulting in:

$$\frac{1}{T_s} = \frac{1}{1.25 \cdot N_{FFT}} \cdot F_s = \frac{0.8}{N_{FFT}} \cdot F_s$$

As an indication Figure 2 shows the resulting SIR values in function of the tolerance for the sampling clock frequency for a range of values, that still would leave some margin to the SNR requirement of 24.4 dB for 64 QAM.

A symbol clock frequency tolerance of 2 % of the subcarrier spacing on the other hand, as currently required in 802.16-REVd/D5, results due to the above relation between the symbol clock and the sampling clock frequency in a much higher tolerance for the sampling clock frequency. Therefore this requirement on the symbol clock frequency is not sufficient.

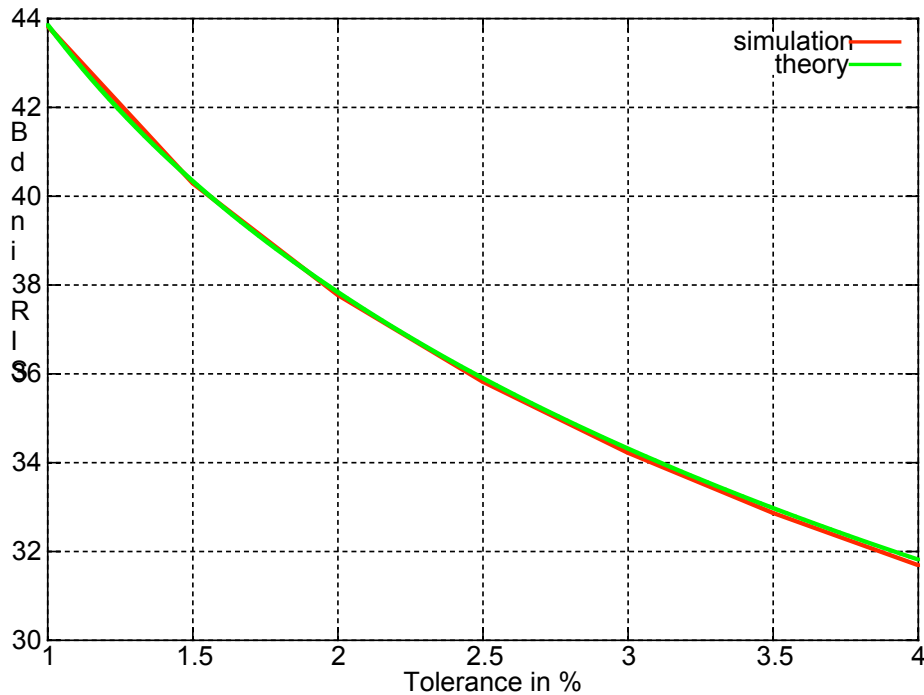


Figure 2: Signal-to-interference ratio (SIR) as a function of the absolute tolerance of the sampling clock  $F_s$  in percent of the subcarrier spacing  $\Delta f$

Even though a tolerance of the symbol clock frequency accuracy derived from the range of values for the sampling clock frequency shown in Figure 2 could be sufficient, there is a more direct means to guarantee a still higher accuracy exploiting the requirement that the symbol clock frequency and the center frequency are derived from a single reference at the BS and thus have a fixed and predefined ratio within the system.

### 3 Proposed solution

The above inconsistencies could be solved and a sufficient accuracy for the symbol clock frequency at the SS could be achieved by explicitly stating that the accuracy of the symbol clock frequency at the SS is guaranteed by its locking to center frequency at the SS, thereby exploiting the fact that through the requirement, that the symbol clock frequency and the center frequency are derived from a single reference at the BS, they have a fixed and predefined ratio.

### 4 Specific text changes

[Change the second paragraph in §8.4.14.1 as follows:]

#### 8.4.14.1 Center frequency and symbol clock frequency tolerance

At the SS, the transmitted center frequency ~~and the symbol clock frequency~~ shall be synchronized and locked to the BS with a tolerance of maximum 2% of the subcarrier spacing. Additionally the symbol clock frequency at the SS shall be locked to the center frequency at the SS which guarantees a tolerance for the symbol clock frequency at the SS of maximum 2% of the subcarrier spacing divided by the center frequency.