Project	IEEE 802.16 Broadband Wireless Access Working Group <**http://ieee802.org/16**>
Title	Improved CTC Performance
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Re:	IEEE P802.16e/D6, sponsor ballot
Abstract	This contribution demonstrates that the convolutional turbo code (CTC) interleavers for block sizes 120 bytes and above have performance deficiencies. By selecting different interleaver parameters for these block sizes, the deficiencies can be corrected. The performance improvement in AWGN at 10^{-4} FER with the new parameters is at least 0.5 dB and in some cases up to 1.3 dB.
Purpose	To provide improved CTC channel coding interleaver parameters when supporting H-ARQ.
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Procedures	include the known use of patent(s), including patent applications, provided the IEEE receives assurance from the patent holder or applicant with respect to patents essential for compliance with both mandatory and optional portions of the standard." Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair <mailto:chair@wirelessman.org> as early as possible, in written or electronic form, if patented technology (or technology under patent application) might be incorporated into a draft standard being developed within the IEEE 802.16 Working Group. The Chair will disclose this notification via the IEEE 802.16 web site <http://ieee802.org/16/ipr/patents/notices>.

Current CTC Performance

The convolutional turbo code (CTC), a parallel concatenation of two duo-binary tail-biting recursive systematic codes, is an optional error control coding mode in 802.16-2004. The CTC interleaver, defined in 8.4.9.2.3.1 and 8.4.9.2.3.2, uses an "almost regular" permutation (ARP) [1],

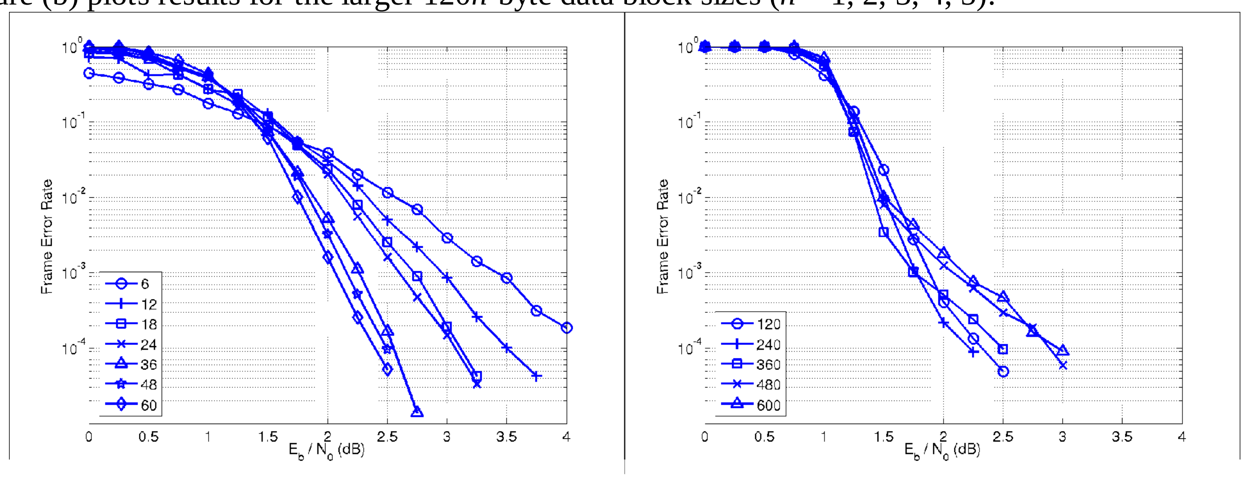
$$\pi(i) = (iP_0 + d(i)) \bmod N \qquad (1)$$

where $0 \le i \le N-1$ is the sequential index, $\pi(i)$ is the permuted index, N is the information block size in bit couples, P_0 is a number that is relatively prime to N, and $d(i)$ is a "dither" vector. For all 802.16 block sizes, $d(i)$ assumes the form

$$d(i) = \begin{cases} 1, & i \bmod 4 = 0 \\ 1 + N/2 + P_1 & i \bmod 4 = 1 \\ 1 + P_2 & i \bmod 4 = 2 \\ 1 + N/2 + P_3 & i \bmod 4 = 3 \end{cases} \qquad (2)$$

for $0 \le i \le N-1$. The values of P_0, P_1, P_2, and P_3 depend on N, and are listed in Tables 326 and 327. Henceforth, this document only considers block sizes contained in Table 327.

Figure 1Figure 1 plots the simulated frame error rate (FER) versus E_b/N_0 using the current 802.16 CTC interleaver specification. The results assume a rate-1/2 code, binary modulation over a static additive white Gaussian noise (AWGN) channel, 7.5 decoding iterations, and perfect "genie" knowledge by the decoder of the encoder circulation states. Sub-figure (a) plots results for 6*n*-byte data block sizes (*n* = 1, 2, 3, 4, 6, 8, 10), and sub-figure (b) plots results for the larger 120*n*-byte data block sizes (*n* = 1, 2, 3, 4, 5).



(a) 6*n*-byte block sizes, *n* = 1, 2, 3, 4, 6, 8, 10 (b) 120*n*-byte block sizes, *n* = 1, 2, 3, 4, 5

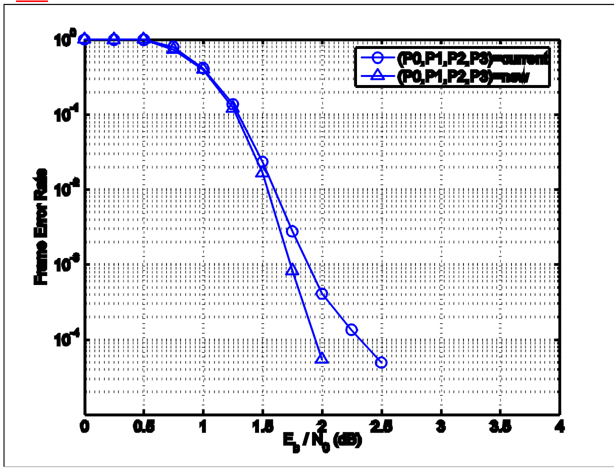
Figure 1. FER performance for currently specified CTC interleavers.

The performance of the 6*n*-byte block sizes displays the expected turbo code behavior of improving performance with increasing block size. Furthermore, no error floor is discernable down to a FER of 10^{-4}. However, the performance of the 120*n*-byte block sizes displays the opposite. Here, the performance degrades with increasing block size (above 240-byte) and a distinct error floor is present.

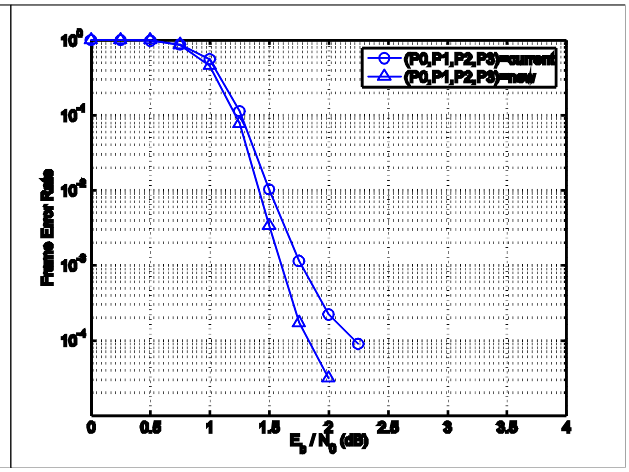
CTC Performance with New Interleaver Parameters

A new set of CTC interleaver parameters was designed to correct the performance deficiencies of the 120*n*-byte block sizes. The new parameters were selected according to guidelines prescribed in [1]. The FER performance (rate-1/2, binary modulation, static AWGN channel, 7.5 decoding iterations, and "genie" circulation state knowledge) with the new parameters is plotted in Figure 2Figure 2. The figure shows that the new parameters

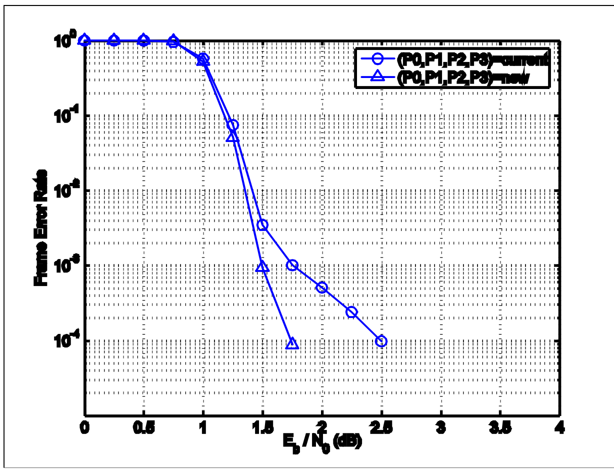
correct the performance deficiencies of the current parameters. At FER = 10^{-4} the performance with the new parameters is at least 0.5 dB and in some cases up to 1.3 dB better than with the current parameters.
The proposed interleaver parameters have been independently tested by Nortel in comparison to the existing parameters. Their results in Figure 3 further support the significant improvement achieved by the proposed parameters.
In addition, a search conducted by France Telecom showed that the proposed parameters are among the best that could be found.



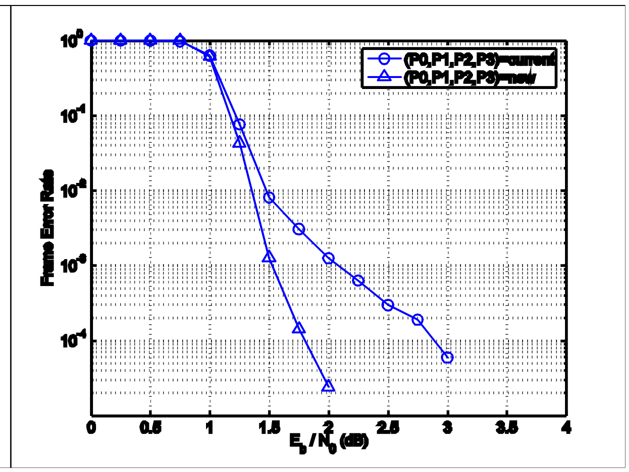
(a) 120-byte block



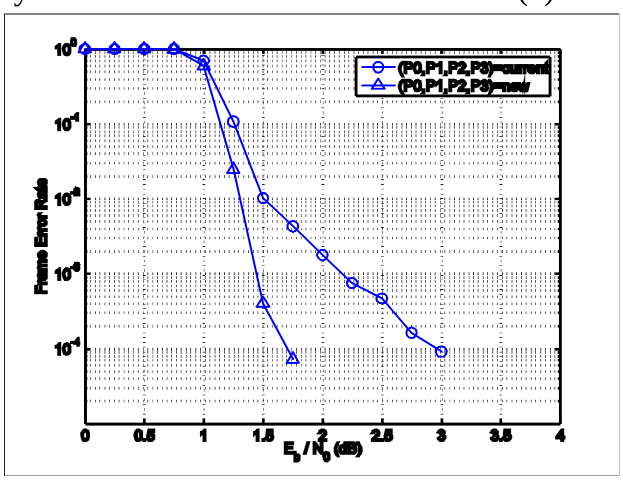
(b) 240-byte block



(c) 360-byte block



(d) 480-byte block



(e) 600-byte block

Figure 2. Performance with new CTC interleaver parameters.

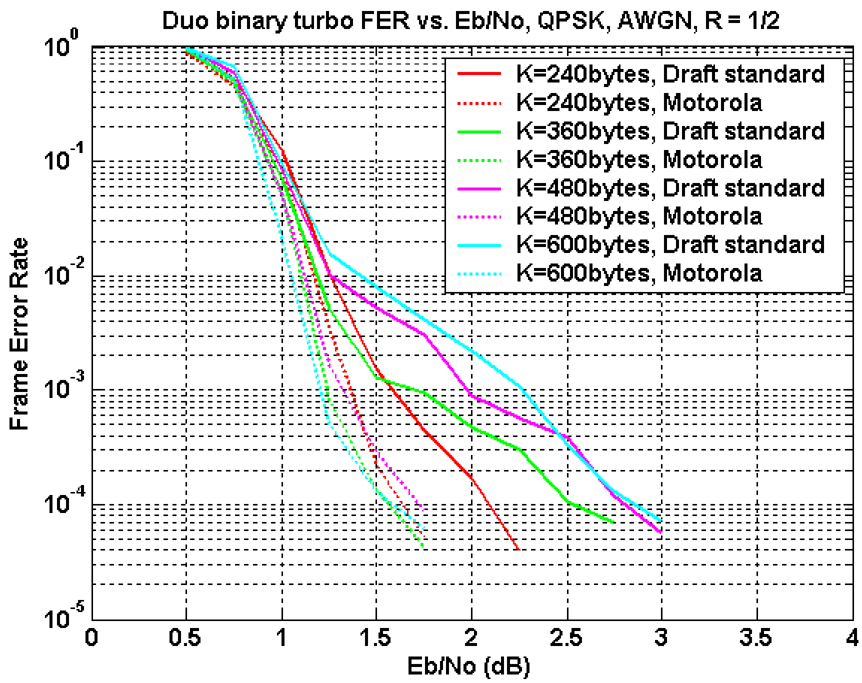


Figure 3. Cross simulation provided by Nortel on the existing and new CTC interleaver parameters.

References

[1] C. Berrou *et al*., "Designing good permutations for turbo codes: towards a single model," in *Proceedings of the 2004 IEEE International Conference on Communications*, vol. 1, pp. 341-345.

Recommended Text Changes:

Make the following changes to IEEE 802.16e/D6 (February 2005), adjusting the numbering as required.

<Insert the following section heading, text, and table on p. 443 line 63.>
8.4.9.2.3.1
[Insert text before table 326]
Table 328 shows alternate code parameters for HARQ.
[Insert table 328 after table 327]

Table 328 – Optimal CTC channel coding per modulation when supporting H-ARQ (alternate).

Data block size (bytes)	**N**	P0	P1	P2	P3
6	24	5	0	0	0
12	48	13	24	0	24
18	72	11	6	0	6
24	96	7	48	24	72
36	144	17	74	72	2
48	192	11	96	48	144
60	240	13	120	160	180
120	480	53	62	12	2
240	960	43	64	300	824

360	1440	43	720	360	540
480	1920	31	8	24	16
600	2400	53	66	24	2

<Revise the table in section 11.8.3.7.2, OFDMA MS demodulator, as follows. Underlined text is new.>

Type	Length	Value	Scope
151	variable	Bit #0: 64-QAM Bit #1: BTC Bit #2: CTC Bit #3: STC Bit #4: AAS Diversity Map Scan Bit #5: HARQ Chase Bit #6: HARQ CTC_IR Bit #7: HARQ with SPID=0 only Bit #8: HARQ CC IR Bit #9: LDPC Bit #10: CTC (alternate H-ARQ) Bits #~~10~~11-15: *Reserved*; shall be set to zero.	SBC-REQ (see 6.3.2.3.23) SBC-RSP (see 6.3.2.3.24)

<Revise the table in section 11.8.3.7.3, OFDMA MS modulator, as follows. Underlined text is new.>

Type	Length	Value	Scope
152	variable	Bit #0: 64-QAM Bit #1: BTC Bit #2: CTC Bit #3: STC Bit #4: AAS Diversity Map Scan Bit #5: HARQ Chase Bit #6: HARQ CTC IR Bit #7: HARQ with SPID=0 only. Bit #8: HARQ CC IR Bit #9: LDPC Bit #10: CTC (alternate H-ARQ) Bits #~~10~~11-15: *Reserved*; shall be set to zero.	SBC-REQ (see 6.3.2.3.23) SBC-RSP (see 6.3.2.3.24)
153	1	The number of HARQ ACK Channel	SBC-REQ (see 6.3.2.3.23) SBC-RSP (see 6.3.2.3.24)