Project	**IEEE 802.16 Broadband Wireless Access Working Group** <http://ieee802.org/16>
Title	**Reduce CTC decoder complexity and enhance error rate performance by the bit-level interleaving**
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Re:	IEEE 802.16m-07/040 - Responds to Call for Contributions on Project 802.16m System Description Document (SDD)
Abstract	This contribution compares the bit-level and symbol-level interleaving. The bit-level interleaving not only provides better error rate performance but also decreases the decoder performance comparing with the symbol-level interleaveing
Purpose	For 802.16m discussion and adoption
Notice	
Release	
Patent Policy	

Reduce CTC decoder complexity and enhance error rate performance by the bit-level interleaving

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Summary

The bit-level interleaving outperforms the symbol-level interleaving and the decoder complexity can further decrease. This contribution recommends adopting the bit-level interleaver for CTC encoder.

Proposed Text

----------------------------*Begin Proposed Text* --

x.x.x CTC interleaver

A bit-level inner-interleaver will be considered.

---------------------------***End of Text Proposal*** ---

1. Introduction

This contribution evaluates the error rate performance and decoder complexity for the bit-level and symbol-level interleaver of CTC encoder in IEEE 802.16e. The bit-level interleaver reduces the decoder complexity in memory storage of the extrinsic part by 33% comparing to the symbol-level interleaver. The bit-level interleaver outperforms the symbol interleaver by at most 0.2dB at frame error rate (FER)=10^{-2}. Since the decoder architecture is still the same, the backward compatibility is achieved. Therefore the bit-level interleavier should be included in the IEEE 802.16 m system. This contribution proposes adopt the text.

2. Double binary turbo code encoder and decoder

Fig. 1 plots the double binary turbo code [1]. The constituent code is the double binary convolutional code and the input symbol is composed of two bits. Since there are two input bits, the CTC interleaver defined in IEEE DRAFT P802.16 [1] is the symbol-level interleaver which composed of two steps: intra-symbol permutation and inter-symbol permutation.

The symbol-level interleaver maintains the information generated by the symbol-based MAP decoding algorithm [2] when the turbo decoder performs interleaving. Fig. 2 plots the turbo decoder in which APP decoder 1 and APP decoder 2 apply the symbol-based MAP decoding algorithm to generate the extrinsic information $L_{ex}(S_i)$ for the other APP decoder the a priori information $L_{prior}(S_i)$. CTC interleaver and de-interleaver perform intra-symbol permutation and inter-symbol permutation on the generated extrinsic information. The intra-symbol permutation switches the alternate odd couples of the input sequences, e.g. (0,0)? (0,0), (0,1)? (1,0), (1,0)? (0,1) and (1,1)? (1,1). This permutation remaps these symbols and the decoder remaps the generated extrinsic information to the associated couple. The inter-symbol permutation repermutes these repermuted couples and the decoder reorders the remapped couples. Since both permutations perform the remapping and reordering of the symbol, there is no information loss coming from the symbol-based interleaving and the generated information can be permuted to the other APP decoder without information loss.

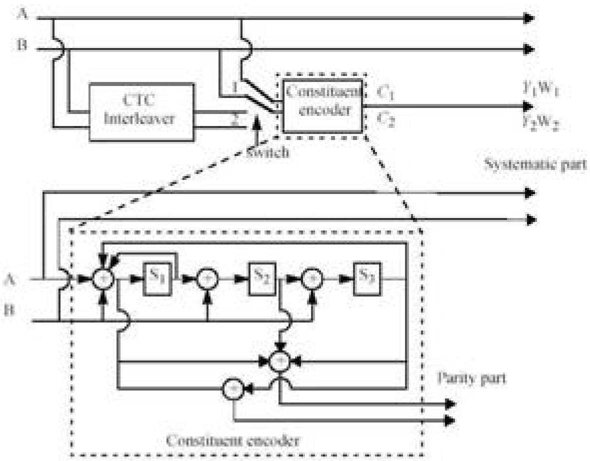

Fig. 1: Double binary turbo code.

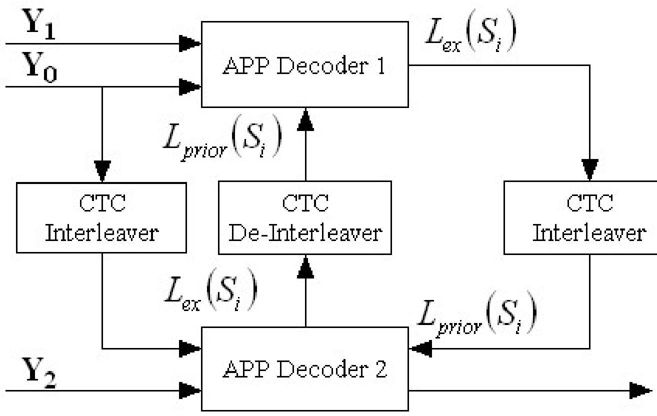

Fig. 2: Turbo decoder

3. Bit-level interleaving and the modification on the decoding algorithm

Bit-level interleaving saves the storage of the extrinsic information and the a priori information. The CTC interleaver can be replaced by the bit-level interleaver which permutes bits instead of symbols or couples. Since the bits are permuted, the generated extrinsic information is also on the bit-level and each symbol only necessitates two log-likelihood ratios $L_{ex}(b_i) = \log \frac{P(b_i = 0)}{P(b_i = 1)}$ to represent the extrinsic information of a symbol. However the storage of a symbol associated with the symbol-based interleaver necessitates three log-likelihood ratios $L_{ex}(S_i) = \log \frac{P(S_i)}{P(S_i = 0)}, S_i = 1,2,3$. Reference [3] on page 1240, column 2, paragraph 3 and also indicates that 50% more storage necessitating for the storage of the extrinsic information and a priori information. Therefore the bit-level interleaving saves the storage of the extrinsic information and the a priori information.

Bit-level interleaving induces information loss when the decoder performs interleaving, but the decoder performance does not degrade due to the compensation coming from the bit-level interleaving. In order to acquire the bit-level information, the marginalization has to be performed as $L_{ex}(b_i) = \log \frac{P(b_i = 0)}{P(b_i = 1)} = \log \frac{P(S_i = 0) + P(S_i = 1)}{P(S_i = 2) + P(S_i = 3)}$ and $L_{ex}(b_i) = \log \frac{P(b_i = 0)}{P(b_i = 1)} = \log \frac{P(S_i = 0) + P(S_i = 2)}{P(S_i = 1) + P(S_i = 3)}$. In general the marginalization induces the performance loss especially when decoding the IEEE 802.16 CTC. However, the bit-level interleaving makes one symbol can collect the a priori information from far away parts and the APP decoder can acquire more uncorrelated information corresponding to these two bits. Therefore the bit-level interleaving can compensate the information loss resulted form the marginalization and the resulting error rate performance even outperforms that of the IEEE 802.16 CTC.

4. Simulation results

This part evaluates the error rate performance for both symbol- and bit-level interleaving. The symbol-level interleaving is the same as the CTC interleaving defined in IEEE 802.16 [1]. The bit-level interleaving applies the inter-block permutation interleaver with the block interleaver defined in IEEE 802.16 [1]. Our simulation environment is AWGN channel. We compare code rate=1/2 CTC with Log-MAP decoding algorithm and 8 iterations are performed. Packet size 960, 1920, 2880, 3840 and 4800 bits are compared.

In Figs. 3-7, The bit-level interleaving outperforms the symbol-level interleaving, and the largest performance gain is 0.25 dB at FER=10^{-2}. If the CTC with symbol-level interleaver applying the marginalized extrinsic information, the performance further degrades 0.2-0.5 dB at FER=10^{-2}.

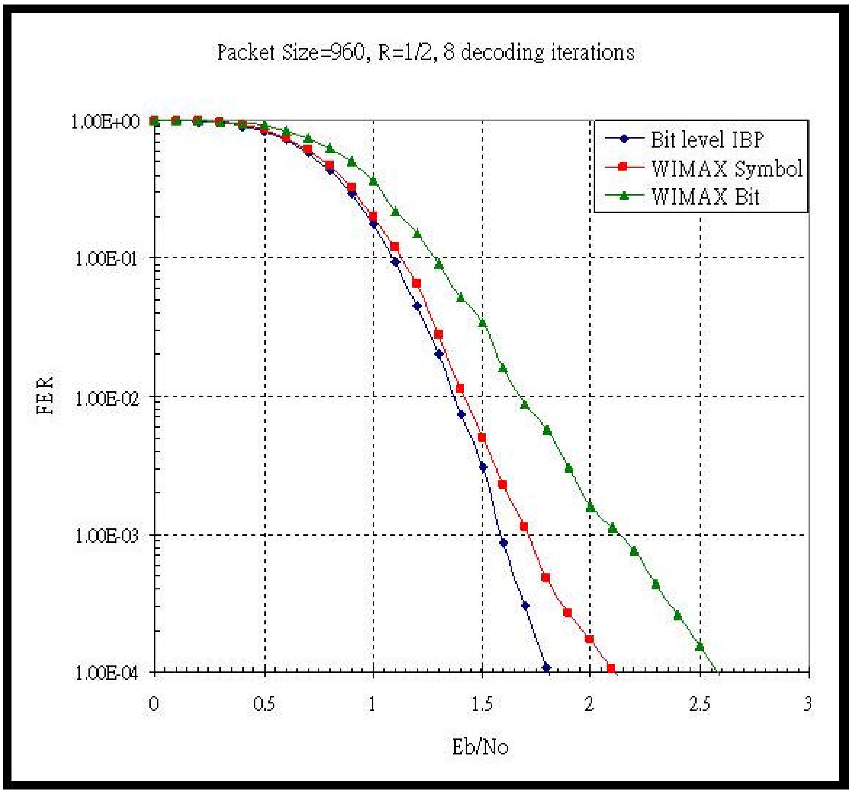

Fig. 3: Frame error rate performance with packet size 960 bits.

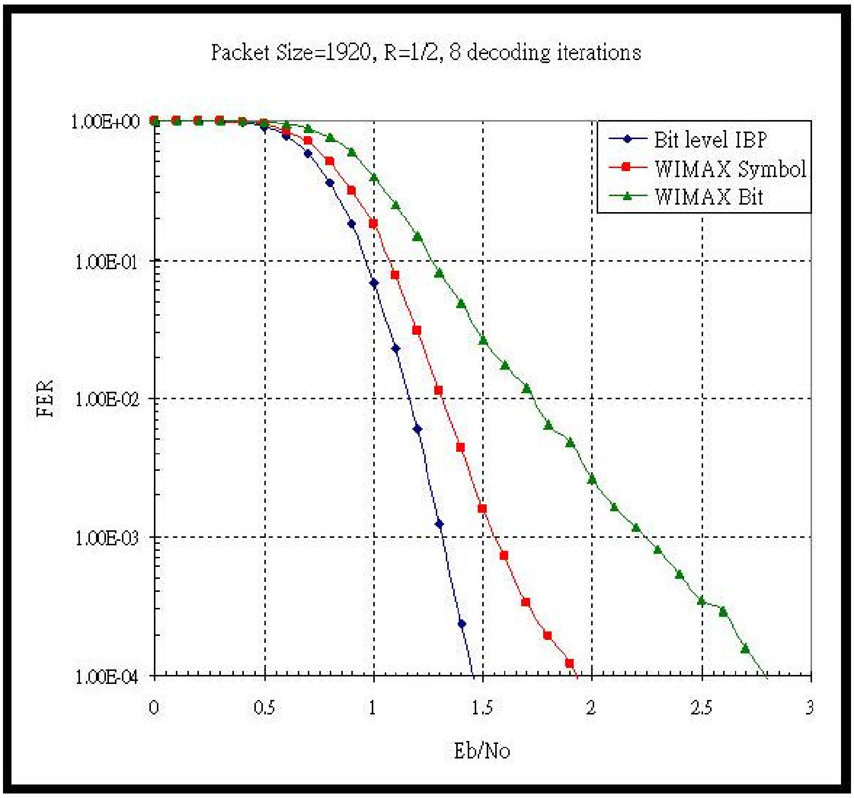

Fig. 4: Frame error rate performance with packet size 1920 bits.

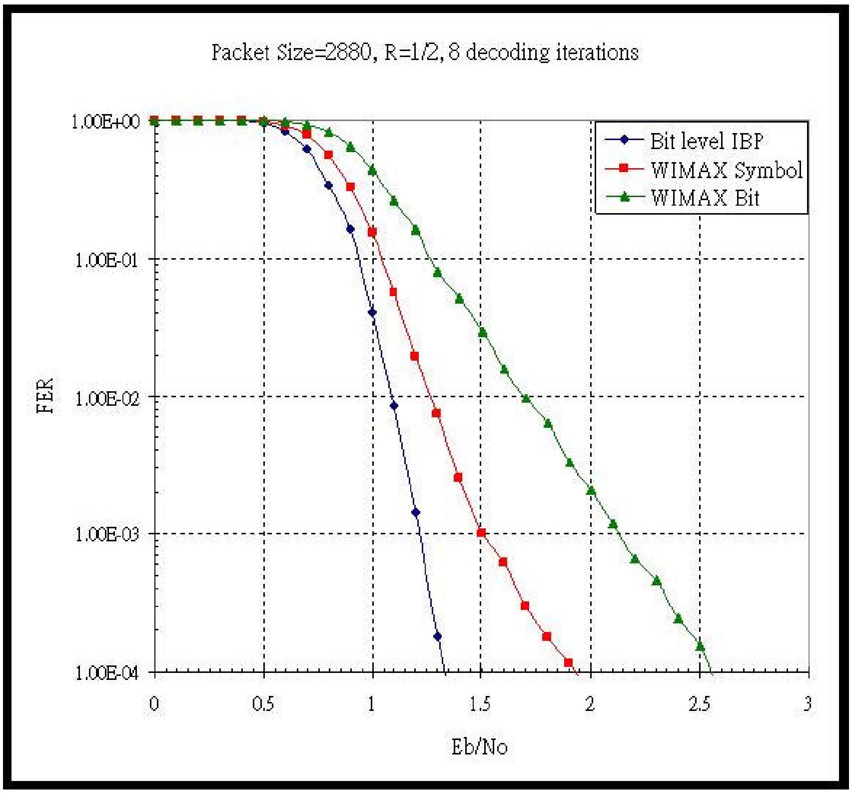

Fig. 5: Frame error rate performance with packet size 2880 bits.

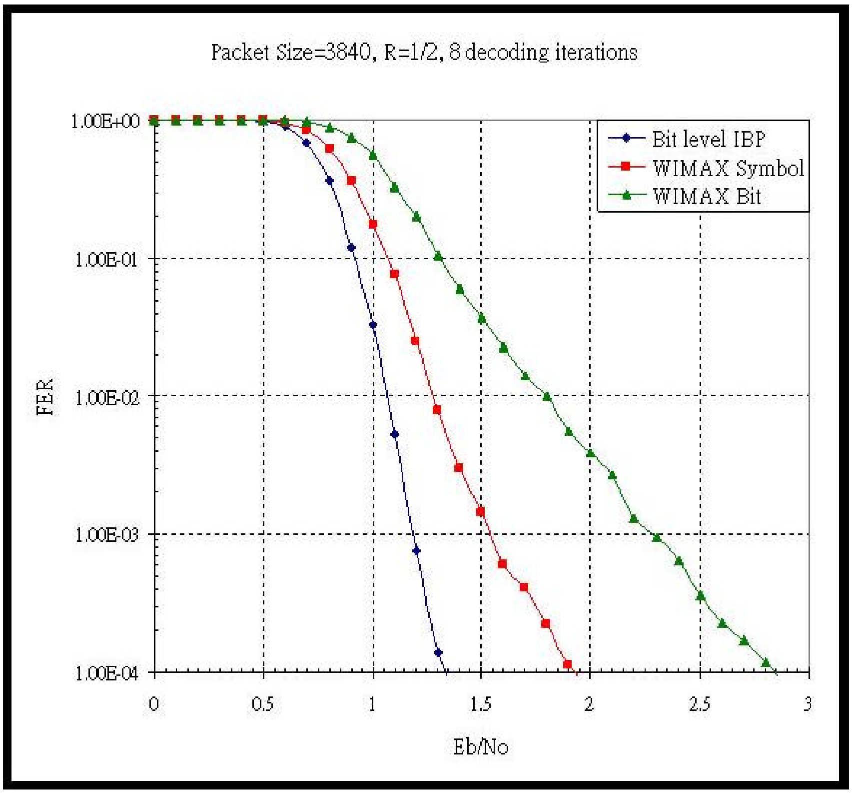

Fig. 6: Frame error rate performance with packet size 3840 bits.

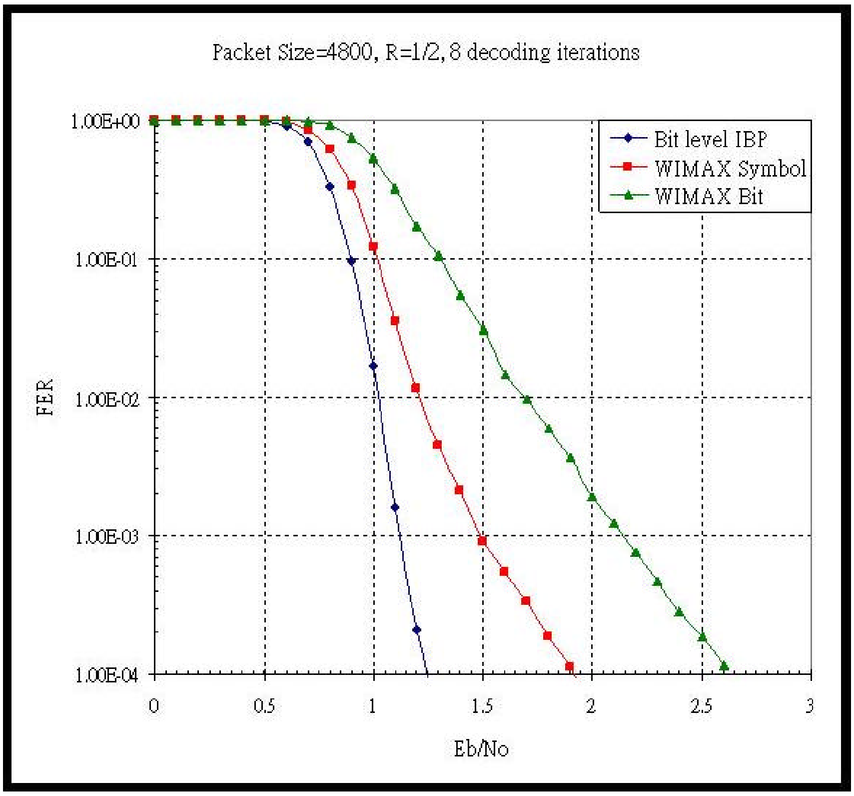

Fig. 3: Frame error rate performance with packet size 4800 bits.

5. Conclusions

The bit-level interleaving outperforms the symbol-level interleaving and the decoder complexity can further decrease. Recommended to adopt the bit-level interleaver for CTC encoder.

6. Table of contents

Channel coding

Encoding

CTC encoder

CTC interleaver

Symbol-level interleaver

Bit-level interleaver

References

[1] IEEE DRAFT P802.16, "Part 16: Air interface for fixed broadband wireless access systems," March, 2007.

[2] L. R. Bahl, J. Cocke, F. Jelinek, F. Raviv, "Optimal decoding of linear codes for minimizing symbol error rate," in *IEEE Trans. on Inform. Theory*, vol. 20, no. 2, pp. 284-287, Mar. 1974.

[3] Ken Gracie, Marie-Helene Hamon, "Turbo and turbo-like codes: principles and applications in telecommunications," in *IEEE Proceeding*, vol. 95, no. 6, pp.1228-1254, Jun. 2007.