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Title	**Corrections in the Implementation of C80216m-09/2532r1 on Four Sector Deployments (Sections 16.3.5 and 16.3.8)**
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Re:	Category: P802.16m/D3 comments for LB30b Area: Sections 16.3.5 (DL PHY Structure) and 16.3.8 (UL PHY Structure)
Abstract	Errors were made during the implementation of contribution C80216m-09/2532r1, which was accepted at Session #64 in Atlanta, GA. This contribution proposes to correct the errors so that the text is as proposed in the previously accepted contribution.
Purpose	Discuss and adopt
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Corrections in the Implementation of C80216m-09/2532r1 on Four Sector Deployments (Sections 16.3.5 and 16.3.8)

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1. Introduction

Contribution C80216m-09/2532r1 proposed changes to the DL and UL PHY structure to better support four sector deployments. The contribution was accepted at Session #64 in Atlanta, GA but was implemented with errors. This contribution proposes changes which correct the errors made in implementing the previously accepted contribution.

2. Proposed Text Changes

[Modify Table 781 (5 MHz bandwidth) on page 325 as follows:]

DFPC	Freq. Partitioning (FP_0:FP_1:FP_2:FP_3)	FPCT	FPS_0	FPS_i (i>0)
0	1:0:0:0	1	N_{PRU}	0
1	0:1:1:1	3	0	N_{PRU} * 1/3
2	1:1:1:1	4	N_{PRU} * 1/4	N_{PRU} * 1/4
3	3:1:1:1	4	N_{PRU} * 1/2	N_{PRU} * 1/6
4	9:5:5:5	4	N_{PRU} * 3/8	N_{PRU} * 5/24
5	0:1:1:0	2	0	N_{PRU} * 1/2 for i = 1, 2 0 for i = 3
6	1:1:1:0	3	N_{PRU} * 1/3	N_{PRU} * 1/3 for i = 1, 2 0 for i = 3
~~5~~ 7	*Reserved*			

[Modify the second line (to the right of the equals sign) in Equation 185 on p. 325 as follows:]

$$DFPSC \qquad i>0,\ FPCT = 4\text{~~,~~} \text{ or } DFPC = 1$$

[Modify the last two lines (to the right of the equals sign) in Equation 185 on p. 325 as follows:]

$$K_{SB\text{~~F~~}}/2 \qquad i = 1, 2,\ FPCT = 2$$
$$K_{SB\text{~~F~~}} \qquad i = 0,\ FPCT = 1$$

[Modify lines 62-65 on p. 328 and lines 1-2 on p. 329 as follows (2 changes):]

When $FPCT$ =2, $DCAS_{SB,i}$ and $DCAS_{MB,i}$ for i=1 and 2 are signaled using the $DCAS_{SB,0}$ and $DCAS_{MB,0}$ fields in the SFH. Since FP_0 and FP_3 are empty, $L_{SB\text{-}CRU,FP0} = L_{MB\text{-}CRU,FP0} = L_{DRU,FP0}$ = 0 and $L_{SB\text{-}CRU,FP3} = L_{MB\text{-}CRU,FP3} = L_{DRU,FP3} = 0$. For i=1 and 2, $L_{SB\text{-}CRU,FPi} = N_1 * DCAS_{SB,0}$ and $L_{MB\text{-}CRU,FPi}$ is obtained using the mappings in Table 782 through Table 784 for system bandwidths of 20 MHz, 10 MHz and 5 MHz, respectively.

[Modify Table 874 (5 MHz bandwidth) on page 499 as follows:]

UFPC	Freq. Partitioning (FP_0:FP_1:FP_2:FP_3)	FPCT	FPS_i (i=0)	FPS_i (i>0)
0	1:0:0:0	1	N_{PRU}	0
1	0:1:1:1	3	0	N_{PRU} * 1/3
2	1:1:1:1	4	N_{PRU} * 1/4	N_{PRU} * 1/4
3	3:1:1:1	4	N_{PRU} * 1/2	N_{PRU} * 1/6
4	9:5:5:5	4	N_{PRU} * 3/8	N_{PRU} * 5/24
5	0:1:1:0	2	0	N_{PRU} * 1/2 for i = 1, 2 0 for i = 3
6	1:1:1:0	3	N_{PRU} * 1/3	N_{PRU} * 1/3 for i = 1, 2 0 for i = 3
~~4~~ 7	*Reserved*			

[Modify the options (i.e., to the right of the large brace) in Equation 237 on p. 499 as follows:]

$$K_{SB} = \begin{cases} K_{SB} - (FPCT - 1)\cdot \sout{D}UFPSC & i = 0,\ FPCT = 4 \\ \sout{D}UFPSC & i > 0,\ FPCT = 4\sout{,}\ \text{or}\ UFPC = 1 \\ K_{SB} - (FPCT - 1)\cdot UFPSC & i = 0,\ FPCT = 3,\ UFPC \neq 1 \\ UFPSC & i = 1, 2,\ FPCT = 3,\ UFPC \neq 1 \\ K_{SB\sout{F}}/2 & i = 1, 2,\ FPCT = 2 \\ K_{SB\sout{F}} & i = 0,\ FPCT = 1 \end{cases}$$

[Modify lines 6-11 on p. 503 as follows:]

When $FPCT$ =2, $\sout{D}UCAS_{SB,i}$ and $\sout{D}UCAS_{MB,i}$ for i=1 and 2 are signaled using the $\sout{D}UCAS_{SB,0}$ and $\sout{D}UCAS_{MB,0}$ fields in the SFH. Since FP_0 and FP_3 are empty, $L_{SB\text{-}CRU,FP0} = L_{MB\text{-}CRU,FP0} = L_{DRU,FP0} = 0$ and $L_{SB\text{-}CRU,FP3} = L_{MB\text{-}CRU,FP3} = L_{DRU,FP3} = 0$. For i=1 and 2, $L_{SB\text{-}CRU,FPi} = N_1 * \sout{D}UCAS_{SB,0}$ and $L_{MB\text{-}CRU,FPi}$ is obtained using the mappings in Table 87~~0~~5 through Table 87~~4~~7 for system bandwidths of 20 MHz, 10 MHz and 5 MHz, respectively.