An Update on RPR Physical Layer Issues

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Overview

- Objectives
- Ethernet RS and PHYs (Annex C)
- SONET/SDH RS and PHYs (Annex D)
- General RS and PHY Issues
- Summary

Objectives

- Build on existing PHY proposals (Darwin PHY and 802-17-01-00118) to provide a complete description of the RPR Physical Layer as the basis for a draft standard
- Propose Gigabit Ethernet support
- Update 10 Gigabit Ethernet RS characteristics
- Clarify the characteristics of the GFP and PoS Reconciliation Sublayers
- Review several issues related to the RS electrical interfaces and Physical Layer specifications

Annex C - Add GE Support to Ethernet RS

- Add the definition for a Gigabit Ethernet (GE) Reconciliation Sublayer (RS) to Annex C:
  - Suggested in 802-17-01-00118, but has not been formally defined or added to Annex C
  - Maps the RPR P-SAP logical interface to the IEEE Standard 802.3 GMII interface
  - Operation to be consistent with the existing P-SAP and the 10 GbE RS definitions

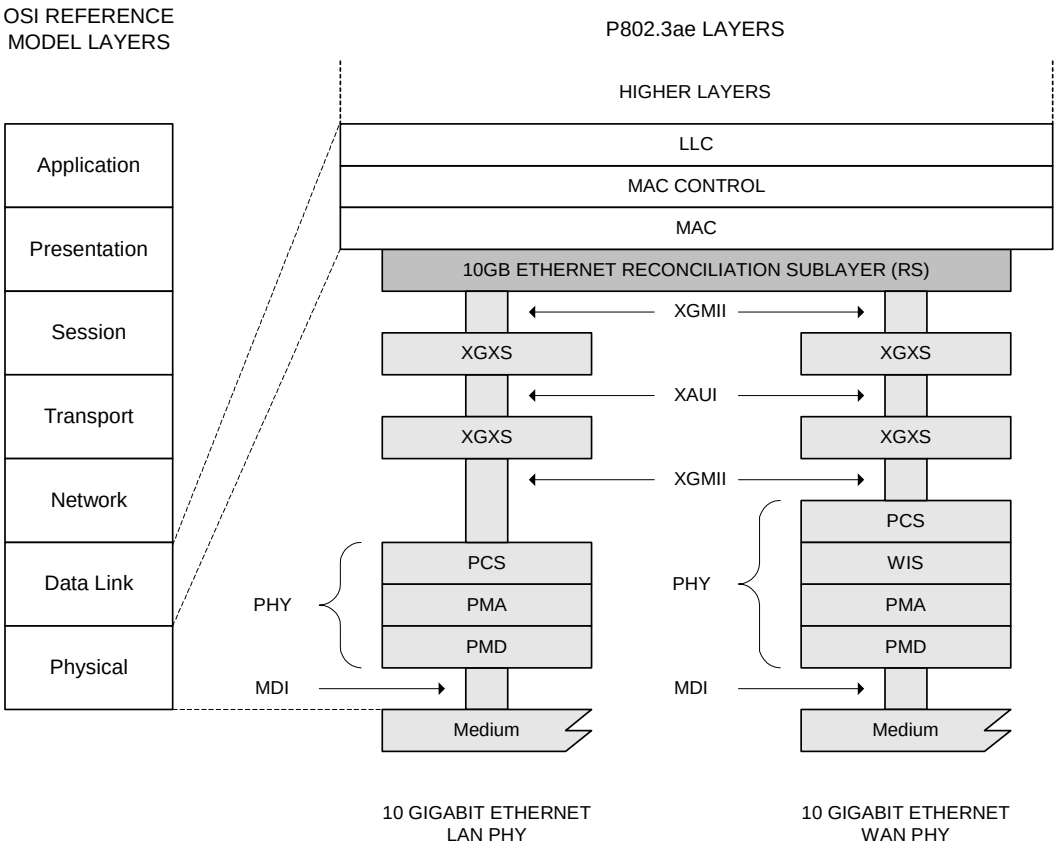
Annex C - Modify Fault Signaling Behavior

- Eliminate the dual-simplex operation proposed for the 10 GbE RS in 802-17-01-00118
  - RPR-specific link fault signaling behavior was previously proposed to allow dual-simplex link operation, but isn't needed for proposed RPR MAC
  - Eliminating simplex operation makes the RPR link fault signaling behavior consistent with the P802.3ae RS (the RS recognizes Local Fault messages and generates Remote Fault messages).

Annex C – Add XAUI as an Option to XGMII

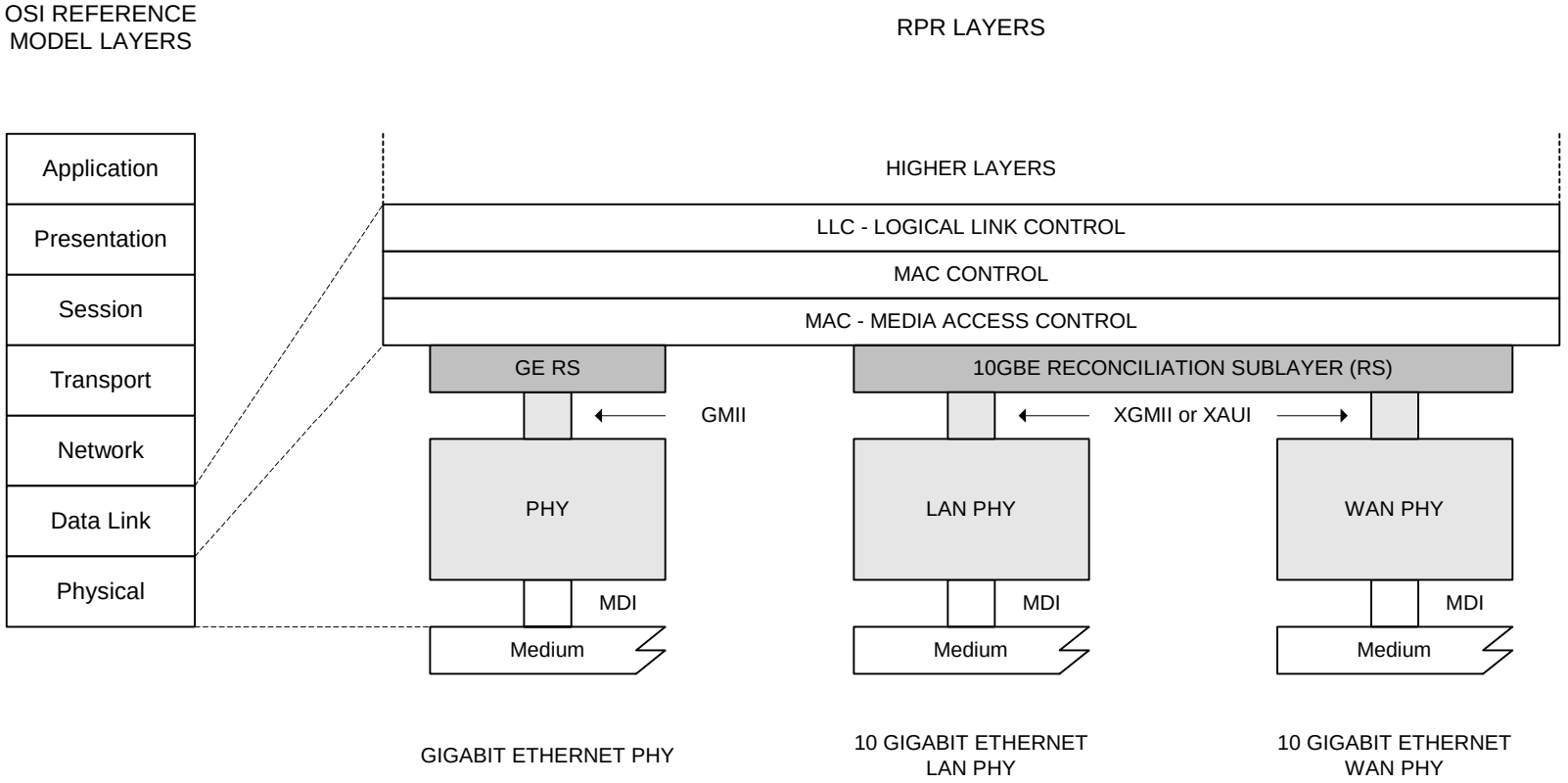
- Propose that the XGMII electrical interface is optional
- Reference the 10 GbE XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI), and provide XAUI as an alternate to XGMII
- XAUI can be used for lower pin-count and/or greater connection distances
- If omitted, an implementation must retain the functional behavior specified through the XGMII
- Propose that XAUI will be specified as an alternative compliance interface to XGMII for the RPR standard.

P802.3ae Layer Diagram



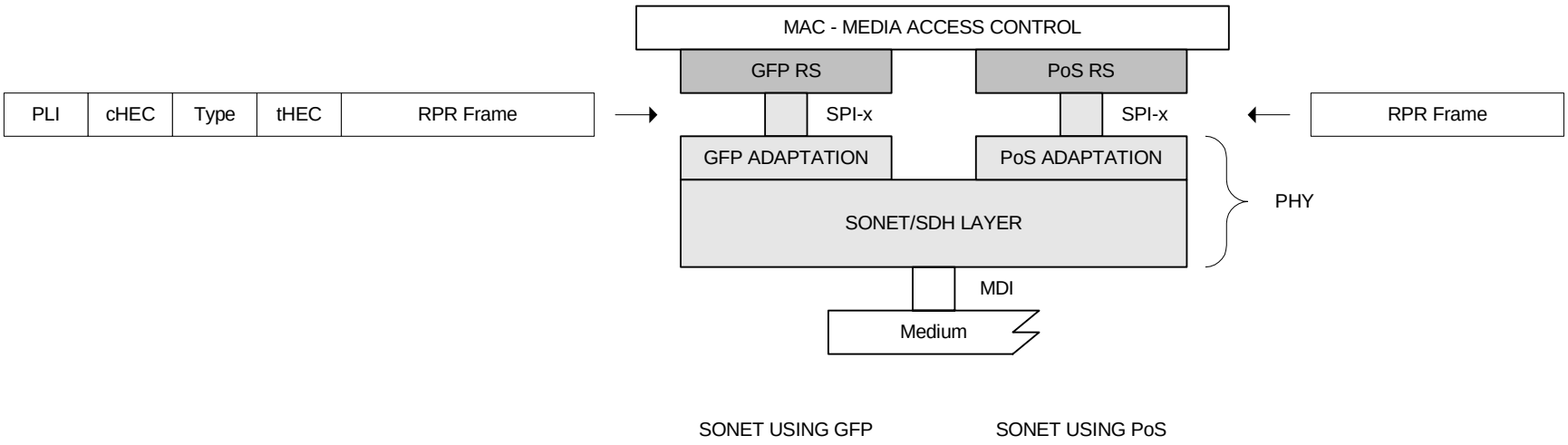
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER ENTITY
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
WIS = WAN INTERFACE SUBLAYER
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

Layer Diagram – Ethernet PHYs for RPR



Annex D – Issues with existing GRS & PRS

- Differences between the GFP Reconciliation Sublayer (GRS) and PoS Reconciliation Sublayer (PRS) are not clear—the two sublayers should present identical data on identical interfaces, except for a GFP header for the GRS
- GFP processing is split between the RS and adaptation layers
- PoS RS shouldn't be limited to only PoS usage



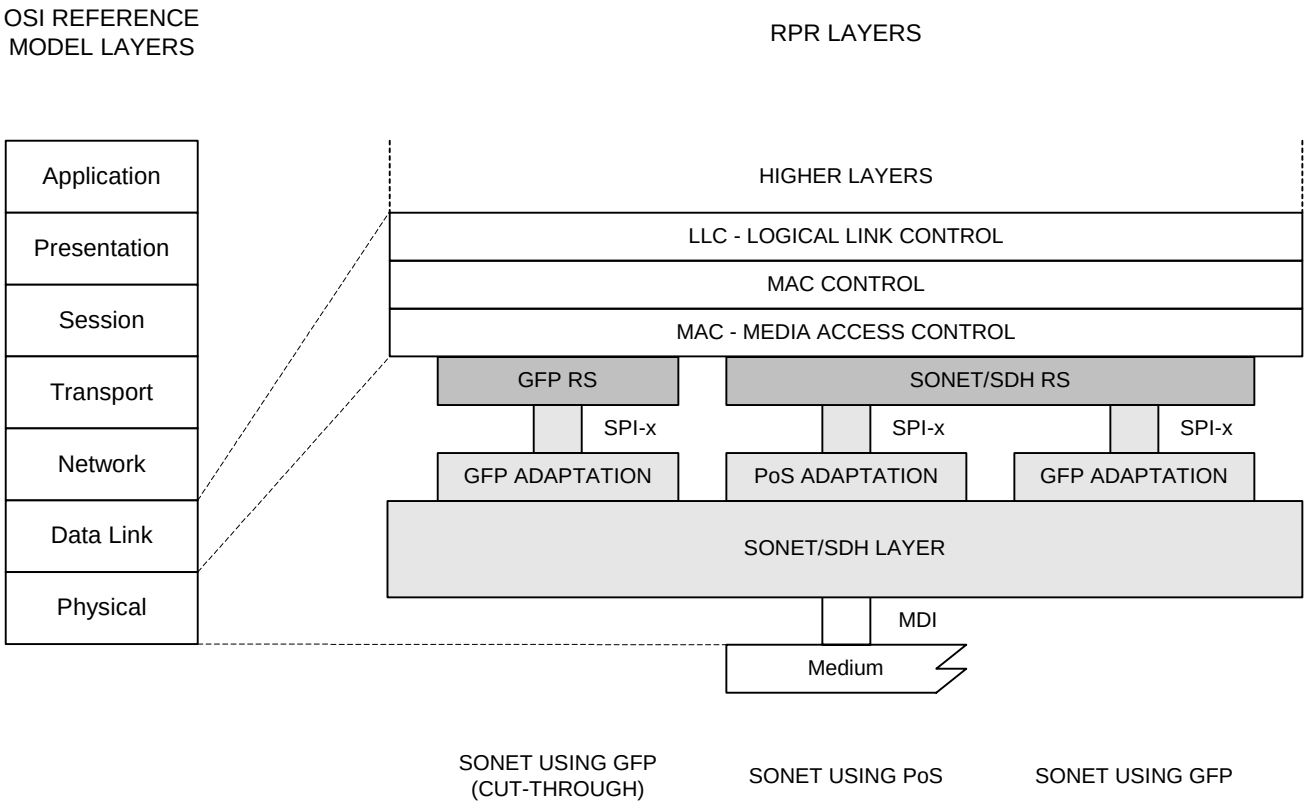
Annex D – Clarify GRS Functions

- The GRS maps the logical RPR P-SAP interface to and from several industry standard electrical interfaces:
  8 or 32-bit SPI-3, SPI-4.1 and SPI-4.2
- The GRS does not do GFP processing—it simply passes the GFP header (including PLI field) in a GFP format across the SPI interface
  - Passing length allows lower-latency cut-through operation
  - Length has already been defined as an optional parameter at the P-SAP logical interface
- An implementation that does not support the GRS has no concept of the GFP header

Annex D – SRS Functions

- The “PRS” is really a SONET/SDH Reconciliation Sublayer (SRS), since it presents generic RPR frame data on standard electrical interfaces for use with PoS, GFP (non-cut-through), or 10 GbE LAN/WAN PHY framers
- The SRS maps the logical RPR P-SAP interface to and from several industry standard electrical interfaces:
  8 or 32-bit SPI-3, SPI-4.1 and SPI-4.2 (same as the GRS)
- No PoS processing is performed by the SRS
- Layer diagram shows SRS with PoS and GFP adaptation sublayers. No 10 GbE “adaptation sublayer” defined at this time.

Layer Diagram – SONET/SDH PHYs for RPR



Annex D – Electrical Interfaces

- The proposed SONET/SDH RS implements SPI-3 or SPI-4 interfaces, but these aren't defined by open standards organizations, and cannot be referenced in an IEEE specification
- Propose that the 8 and 32-bit SPI-3, SPI-4.1 and SPI-4.2 interfaces be "re-defined" within the RPR standard
  - Creates duplicate references, but allows use within IEEE standards
  - Similarly done with SFI-4 for P802.3ae (XSBI)
  - Note that this is not a trivial effort

Annex D – RS Compliance Interface

- Propose that the SONET/SDH RS SPI-3 or SPI-4 electrical interface is a compliance interface
- In some implementations, it may be desirable to integrate PHY functions. For example, GFP processing may be included in a MAC implementation, since many existing GFP processors aren't well suited to RPR applications
- In the case of integration, the device must provide a bypass mode or other capability for access to a standard RS interface to verify compliance

Ethernet and SONET/SDH PHYs

- Draft text has single clauses that mix RS and PHY issues, which need to be distinguished
  - Clearly and fully define the Reconciliation Sublayers that are needed to interface the RPR MAC to a group of Physical Layer implementations
  - Reference the applicable Ethernet and SONET/SDH PHYs intended to be used with the Reconciliation Sublayers
  - Reference applicable specifications for the GFP and PoS adaptation layers, and specify any parameters or options needed for “standard” RPR applications
  - Add or clarify any interfaces from the RS or PHY to the Layer Management Entity.

Summary

- Update existing PHY proposals (802-17-01-00118 and Darwin) to be form a complete description of the RPR Physical Layer to be used for a draft standard
- Add Gigabit Ethernet support to Annex C
- Update 10 Gigabit Ethernet RS characteristics in Annex C
- Clarify the GRS and SRS functions, as well as the electrical interface requirements in Annex D
- Clearly define the RS, and reference PHY requirements for Ethernet and SONET/SDH Physical Layers.