Cyclic-Reservation RPR MAC Protocol with Link-Fairness

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Protocol properties

Support of:

- Link-fairness
- Service Level Agreements (SLAs)
- Heterogeneous link speeds

Performance properties:

- Control of flow-based source-destination traffic
- No HOL blocking
- Very high ring throughput
- Node throughputs approximate theoretical fairness values
- Low delays
- No losses
- No backpressure required
- Insertion buffer occupancy at most one MTU size
- Free and reserved access
- Unfairness due to free access can be corrected
- Pure free access in case of loss of fairness control packet

Assumptions

Two traffic classes with individual bottleneck-fairness control
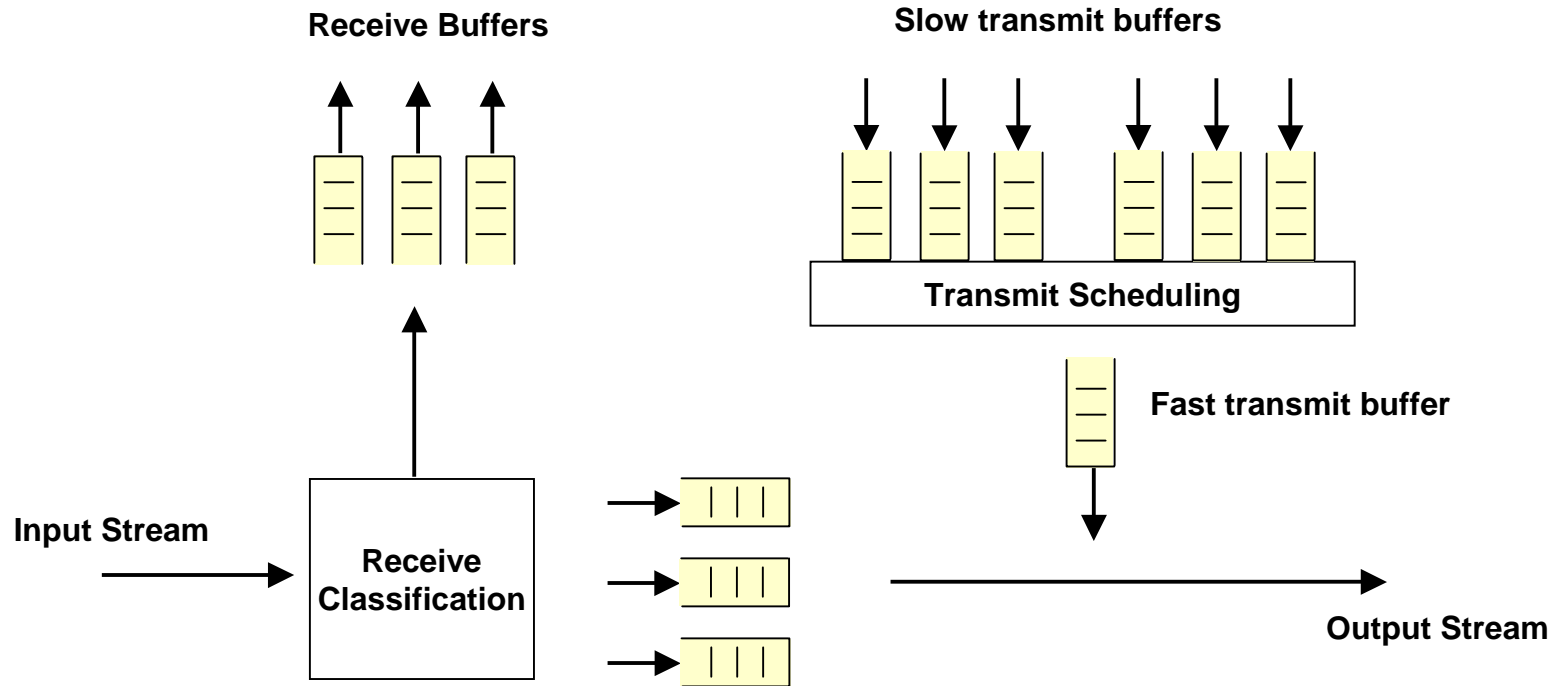
- All nodes know
  - the bit rates of all transmission links (heterogeneous links)
  - the constant bandwidth of all source-destination flows (CBR)
  - the guaranteed bandwidth of all source-destination flows (VBR)

- Information is distributed by token-based resource reservation protocol

Simultaneous Access by buffer insertion

Station A   Station B
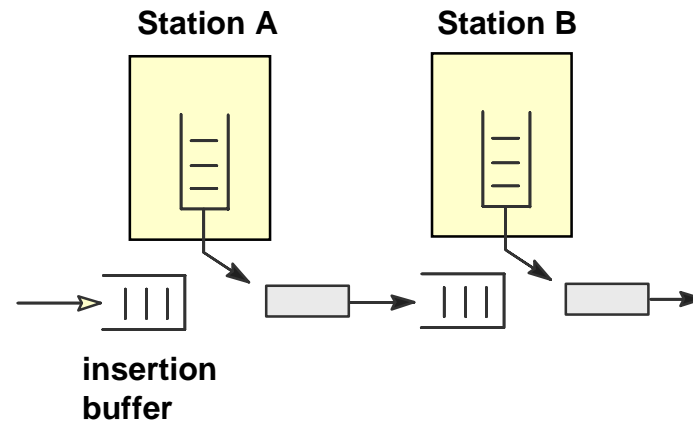
insertion
buffer

- Insertion buffer in transmit path is only used to resolve collision conflict
  during packet transmission

- Cut-through mode

- Maximum size of insertion buffer is 1 MTU

- Insertion buffers (low and high) must both be empty before medium
  access takes place

Node Structure

Receive Buffers

Slow transmit buffers

Transmit Scheduling

Fast transmit buffer

Input Stream

Receive Classification

Insertion buffers

Output Stream

- Ring priority
- Priority bypassing on ring

Access mechanism

- Insertion buffer solves only packet collision problem. Not used for scheduling.

- Transmission path is used as a pure transmission link, i.e. ring priority

- Insertion buffer must be emptied before accessing the ring

- Only medium access scheduling

Fairness

Global fairness: Fairness based on a mechanism that allows nodes to share the same amount of the transmission capacity of the ring, independently whether their traffic interfere or not

Local fairness: Fairness based on a mechanism that coordinates ring access of only those nodes that interact during their packet transfer
Therefore, all nodes that do not interfere are not throttled in their performance
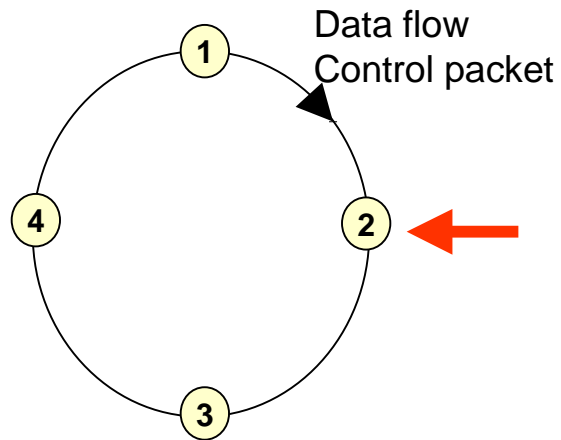
Fairness mechanism (1)

Data flow
Control packet
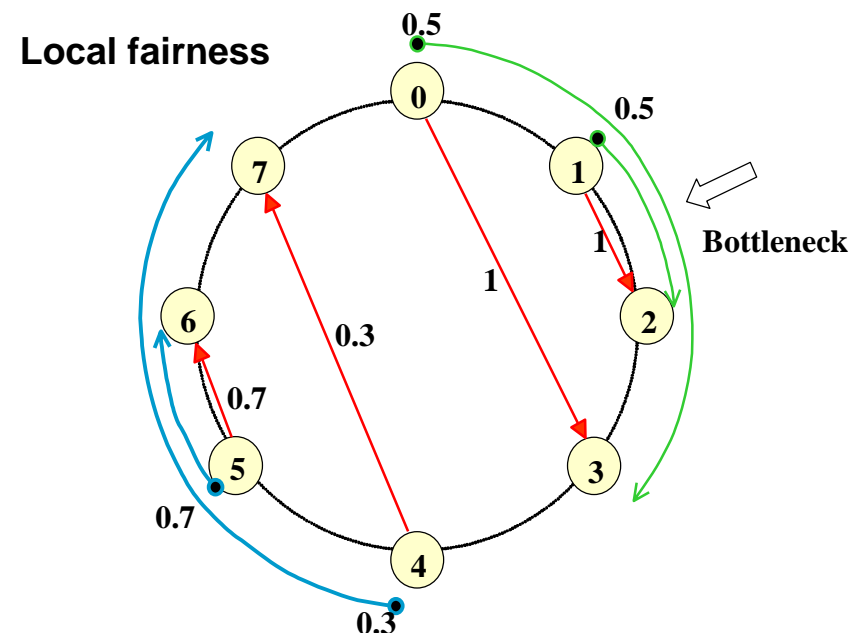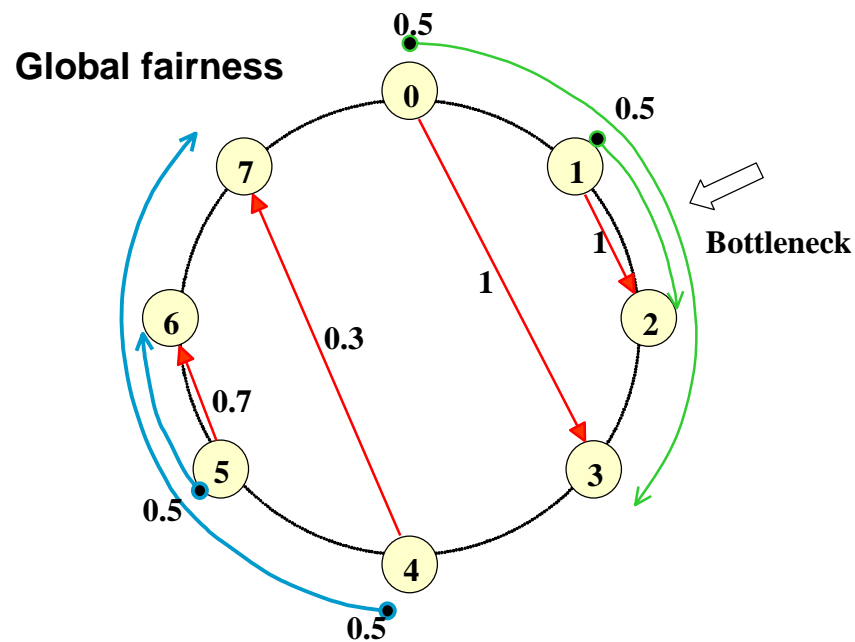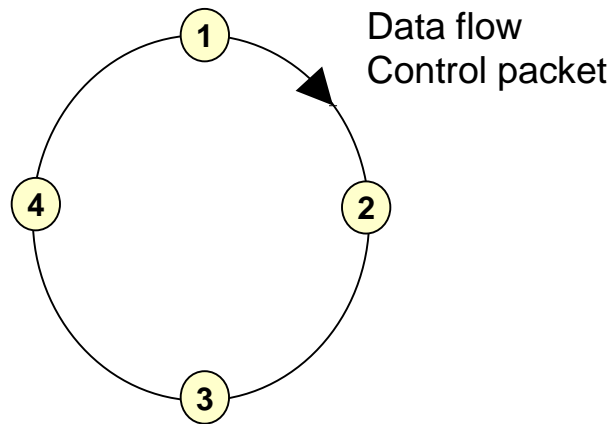
- Control packet circulates on each ring in data direction

- One entry for each traffic and for each source-destination flow

- Circulating information is based on waiting load in each node, not on old
  measurements on the links

- Circulating information is corrected for each bottleneck link

- Fairness reaction time is 1 roundtrip of the control packet

Fairness mechanism (2)

Example with single ring

Cycle i-1

Flow	High	Low
1 -> 2	H12	B12
1 -> 3	H13	B13
1 -> 4	H14	B14
2 -> 3	H23	B23
2 -> 4	H24	B24
2 -> 1	H21	B21
3 -> 4	H34	B34
3 -> 1	H31	B31
3 -> 2	H32	B32
4 -> 1	H41	B41
4 -> 2	H42	B42
4 -> 3	H43	B43

Old table in node 2

Cycle i

Flow	High	Low
1 -> 2	H12	B12
1 -> 3	H13	B13
1 -> 4	H14	B14
2 -> 3	H23	B23
2 -> 4	H24	B24
2 -> 1	H21	B21
3 -> 4	H34	B34
3 -> 1	H31	B31
3 -> 2	H32	B32
4 -> 1	H41	B41
4 -> 2	H42	B42
4 -> 3	H43	B43

New table in node 2

Data flow
Control packet

Coordinated table values
In node 2

Fairness mechanism (3)

Data flow
Control packet

Link 2

Actions in node 2:

- Determine fairness on link 2
  - Correct flows H13, H14
        H23, H24, H21, H43
  - Correct flows L13, L14
        L23, L24, L21, L43
- Determine total amount of coordinated capacity over link 2
- Write new demand of node 2 into control packet
- Send control packet to next node at the scheduled time
- Transmit coordinated flows H23, H24, H21, L23, L24, L21
- Refrain from transmission during rest of the coordinated capacity
- Transmit by immediate access according to the stored rates for each destination

Cycle i-1

Flow	High	Low	
1 -> 2	H12	H12	L12
1 -> 3	H13	H13	L13
1 -> 4	H14	H14	L14
2 -> 3	H23	H23	L23
2 -> 4	H24	H24	L24
2 -> 1	H21	H21	L21
3 -> 4	H34	H34	L34
3 -> 1	H31	H31	L31
3 -> 2	H32	H32	L32
4 -> 1	H41	H41	L41
4 -> 2	H42	H42	L42
4 -> 3	H43	H43	L43

Old table in node 2

Cycle i

Flow	High	Low	
1 -> 2	H12	H12	L12
1 -> 3	H13	H13	L13
1 -> 4	H14	H14	L14
2 -> 3	H23	H23	L23
2 -> 4	H24	H24	L24
2 -> 1	H21	H21	L21
3 -> 4	H34	H34	B34
3 -> 1	H31	H31	B31
3 -> 2	H32	H32	B32
4 -> 1	H41	H41	B41
4 -> 2	H42	H42	B42
4 -> 3	H43	H43	B43

New table in node 2

Fairness mechanism (4)
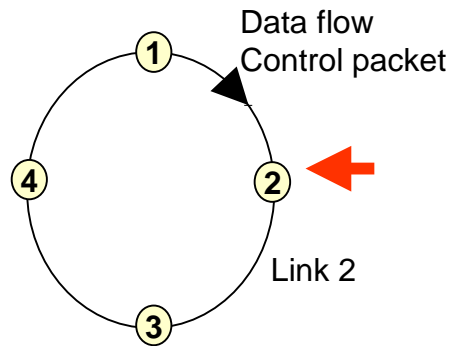
Σ L : all low-traffic flows
Σ V : all non-guaranteed high-traffic flows
Σ G : all guaranteed high-traffic flows
Σ F : all CBR traffic flows
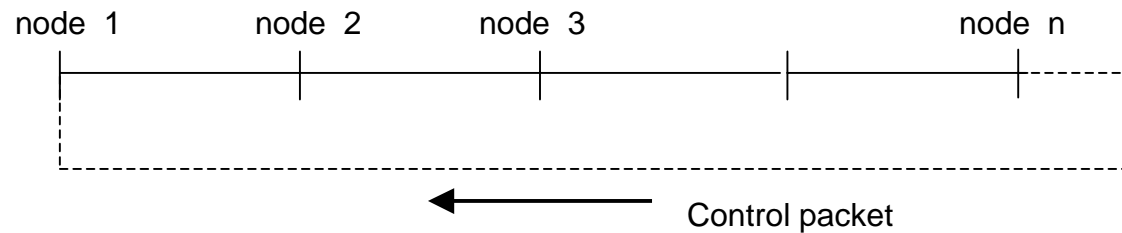$V_i = H_i - G_i$: variable part of high-priority traffic flow

Data flow
Control packet

Link 2
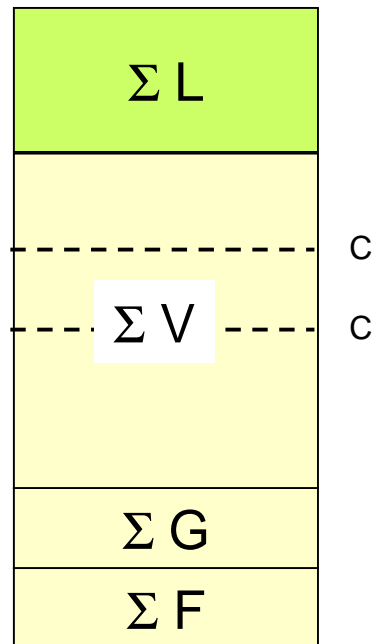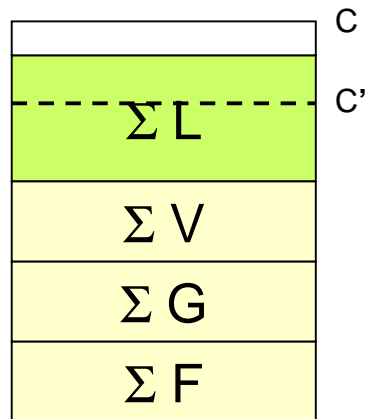
Link capacity C

C- C' is minimal capacity
for low priority when present

	C
	C'
Σ L	
Σ V	
Σ G	
Σ F	

No correction

	C
Σ L	
	C'
Σ V	
Σ G	
Σ F	

Link bottleneck
Correction required

	C
Σ L	
	C'
Σ V	
Σ G	
Σ F	

Link bottleneck
Coordinated flows
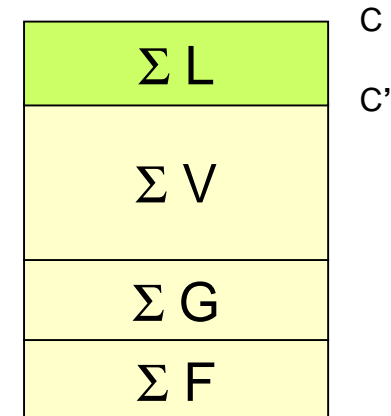
Fairness mechanism (5)

Fairness cycle

Data flow
Control packet

Link 2

node 1   node 2   node 3   node n

Control packet

Timing at node 2

Arrival of
control packet

Previous departure
of control packet
at node 2
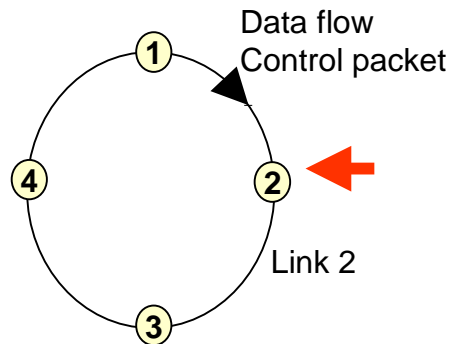
Scheduled departure
of control packet
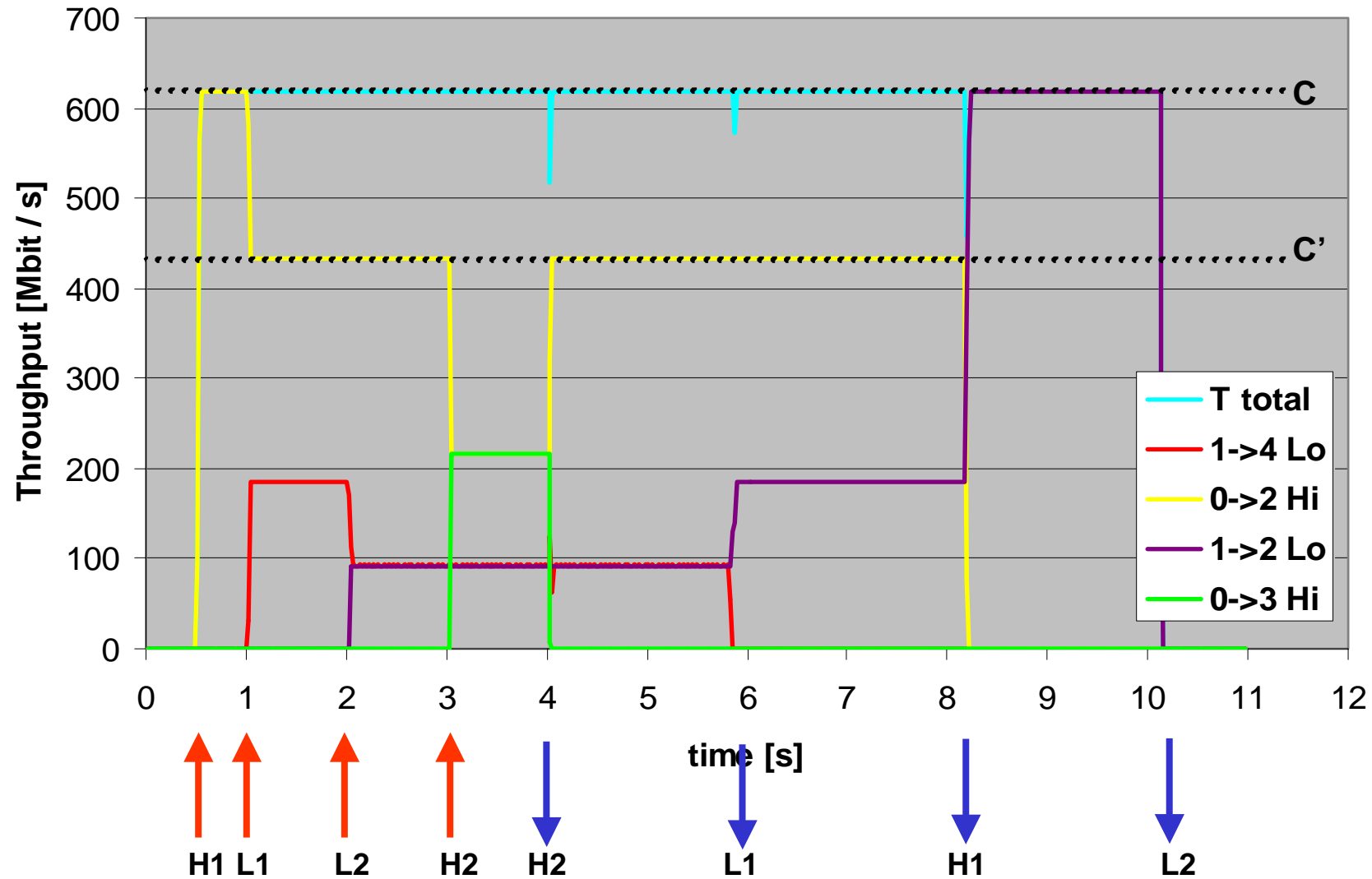at node 2
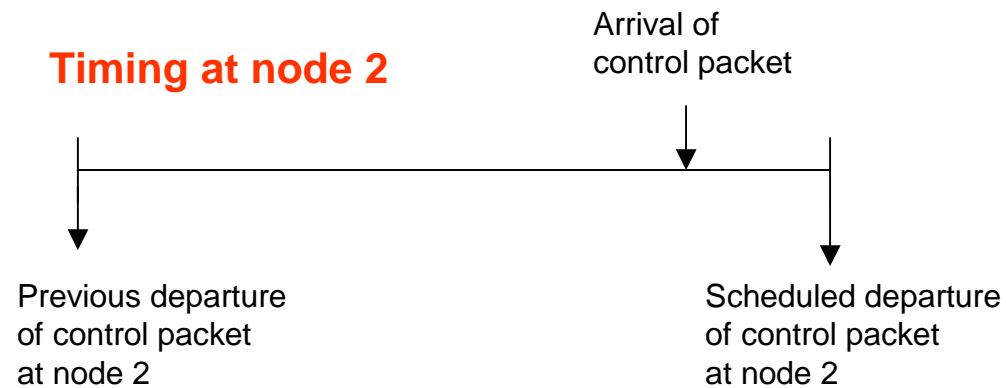
Traffic scenario
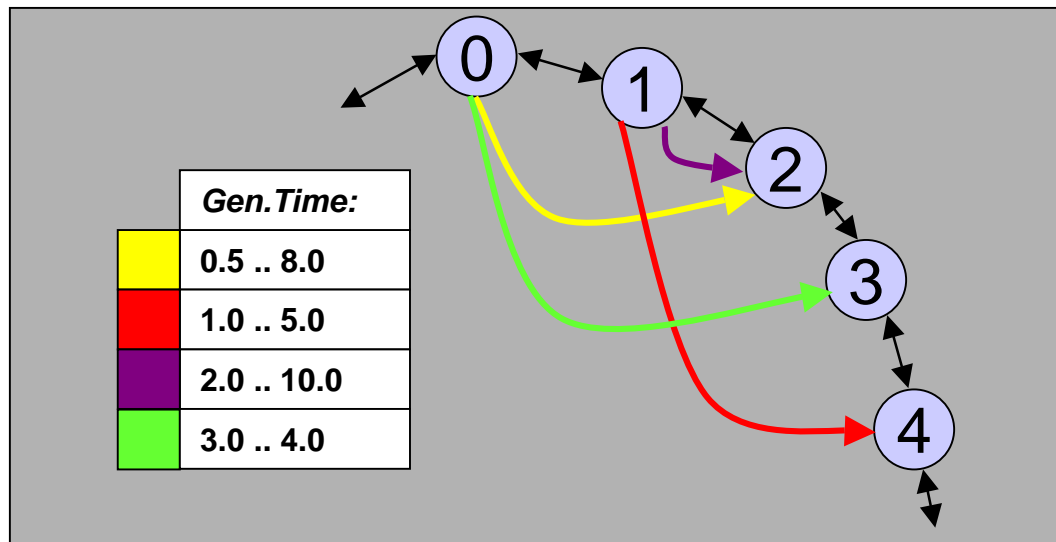
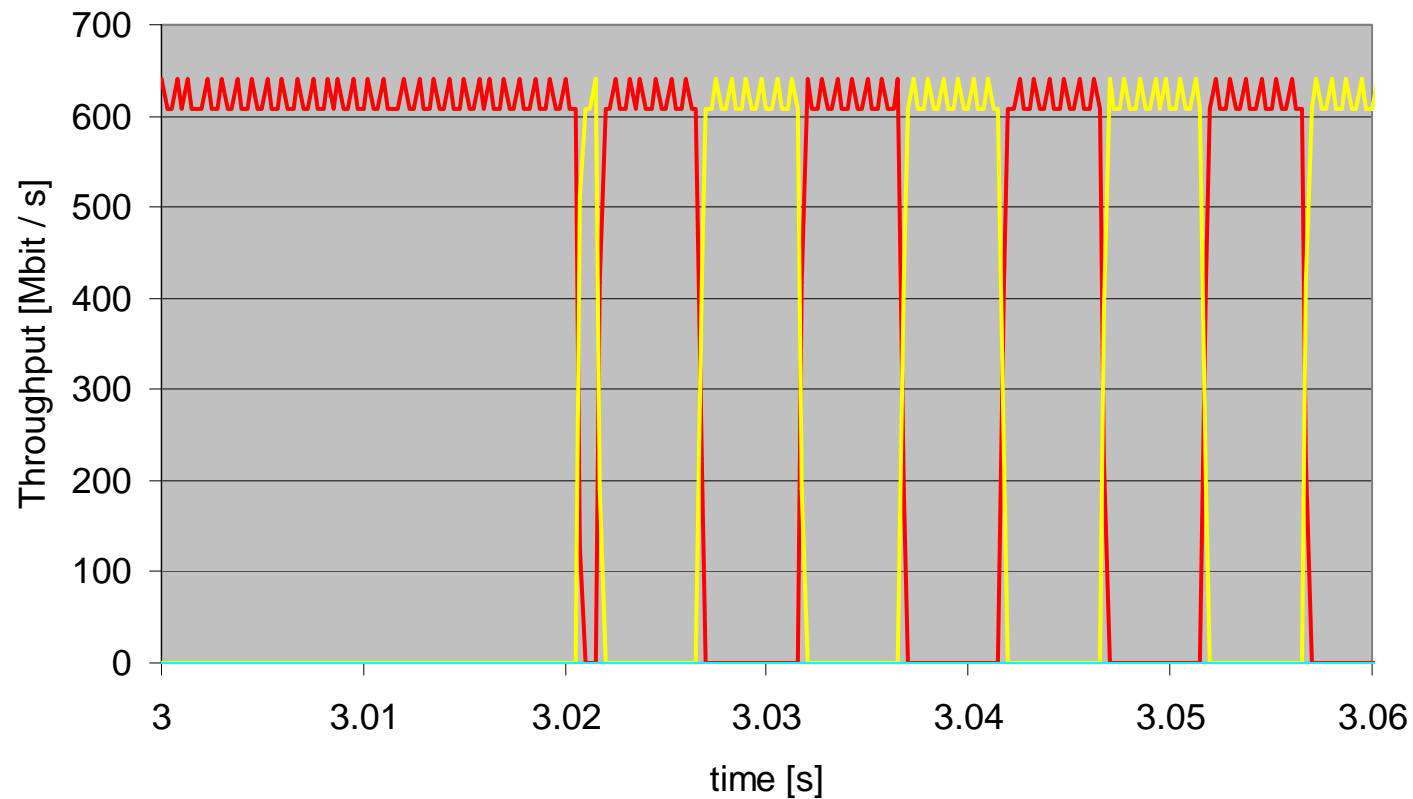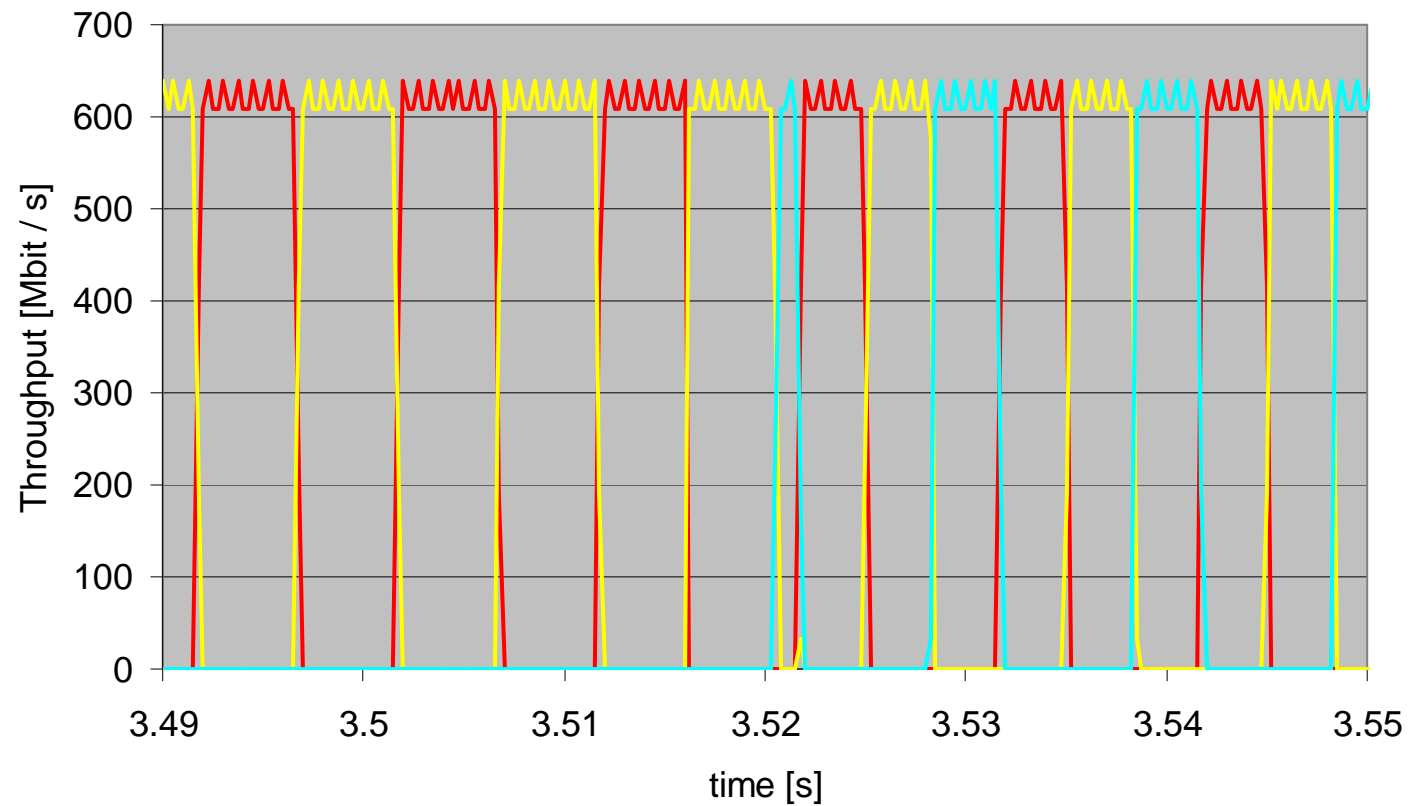# Transient throughput fairness

1→2 flows sharing a ring segment

2→3 flows sharing a ring segment

3→2 flows sharing a ring segment