100GBASE-KP4 Transmitter Characteristics Ad Hoc

24 Oct, 2012

- This call is an IEEE appointed ad hoc.
- The meeting rules apply regarding IP, cost, confidential clauses, etc.

Attendance

- If you are on the call, please send me an email
- * 6 to mute and unmute

Agenda

- IEEE patent policy reminder
  http://www.ieee802.org/3/patent.html
- Open Action Items
- Rise time vs linear fit (Charles Moore)
- 100GBASE-KP4 training frame updates for full state pinning (Adee Ran)
- Discuss next steps

Open Action Items in Ad Hoc

- First analysis of transition times from linear fit (Charles Moore)
- Training to data mode initialization with termination bits (Adee/Kent)
- Training pattern seed structure changed based on partial state to full state pinning (Adee/Kent)
- Example training frame sequence (Adee/Kent)
- Pk-pk limit approach is different from Clause 93. (TBD)
- Investigate linear fit pattern (Adee/Kent) – in 2 weeks
- Coef ratios for INITIALIZE (Kent Lusted) – in 2 weeks
- Report out discussion on overhead bits (Zhongfang Wang and Matt Brown)

Linear Fit Update – Charles Moore

- See risetime_vs_fit_pulse.pdf

Training Pattern Update

- See pages 8-15

100GBASE-KP4 Training Frame Update Goals

- Use full-state pinning termination in Draft 1.2
  - 1 PAM4 symbol (termination) with bits taken from known PRBS sequence
  - 45 PAM4 symbols precoded
- Enable locking on termination PRBS during training
  - Essential for data decoding
- Make training frame same size as PMA frame
  - Simplifies implementation
  - Use PAO for EEE ALERT frame only
- Maintain spectrally rich, DC balanced and uncorrelated lane sequences

100GBASE-KP4 Precoding changes from D1.2

- Training frame word (TFW) is still 46 UI
  - Now TFW is same size as D1.2 termination block
  - In D1.1, 1 TFW = 2 TB46
- TFW is now created from 92 bits of PRBS13 at a time (instead of 45 bits at a time in D1.1)
  - Gray coding results in 46 bit-pairs
  - First pair is used for initializing the precoder state
    - As per 94.2.2.6
  - The remaining 45 pairs fed through the precoder
    - As per 94.2.2.6

Frame size changes from D1.2

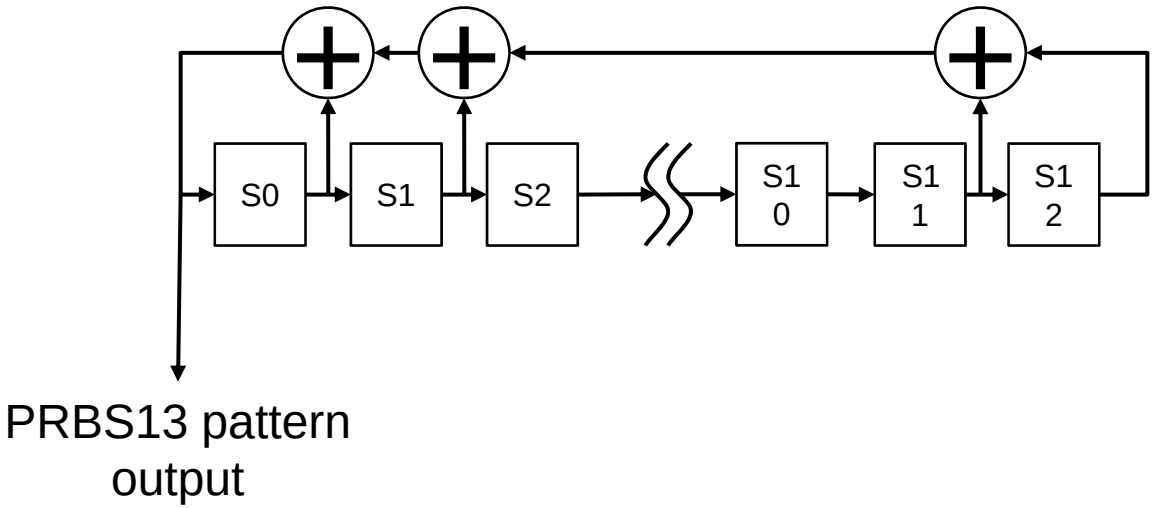
- Propose to increase training pattern length to 338 TFWs
  - Requires 338*92=31096 bits from PRBS13
  - PRBS13 full cycle is 8191 bits
  - Use 3 full cycles + 4th cycle truncated to 6523 bits
  - Bits from 2nd and 4th cycles are inverted
- Added to marker and control channel (10 TFW together), the new training frame is 348 TFWs, which is equal to the PMA frame size

Transition from training to data

- Training frame is always aligned with the PMA frame; last training frame is immediately followed by 40-bit overhead of data
  - No need for PAO field in training (only in EEE alert)
  - Countdown field still used to signal transition
  - 40-bit overhead should start with a termination symbol to be consistent; otherwise data should start with the termination symbol preceding the 40-bit overhead
- PRBS13 is re-seeded at the beginning of each training sequence during training mode, but keeps running freely in data mode
  - Termination bits get synced during training
  - PRBS always advances 92 bits per TFW in training and by 92 bits per term block in data mode

PRBS generator change

- Modified Fibonacci polynomial: $G(x)=1+x+x^2+x^{12}+x^{13}$
  - Old one was $G(x)=1+x+x^2+x^{11}+x^{13}$
  - Required to enable creating 4 DC balanced, quasi-white, non-correlated sequences



Initial outputs

- The *initial outputs* of the PRBS13 generator, right after the control channel transmission, shall be different for each of the PMD lanes, as follows (LSB transmitted first)
  - PMD lane 0: 0xCD92
  - PMD lane 1: 0x2AFB
  - PMD lane 2: 0xC3D3
  - PMD lane 3: 0xE2F6
- Generator is re-seeded to same values at the beginning of every training frame pattern

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Blue = first TFW
Green = second TFW

Initial sequences

Lane	Output of	Contents of first 2 TFWs (from left to right)
L0	PRBS	0100100110110011110001010101100001001001110111110011101000001110100110111010011100110010101111 0001111111010111011011111110100010110111110100111101100101011001110010011100001111000011010111
	Gray code	10313202201111301031212312100121021210231311112 01222112132222101132233123203320231023012301332
	Precoder	130120020010103100320112332222332201100210323 20 01111011033332232111210211303311231122330012 11
L1	PRBS	11011111010101000000100100110110011110001010101100001001001110111110011101000001110100110 1110 10011100110010101110001111111010111011011111110100010110111110100111101100101011001110010 0111
	Gray code	21222111000310213123033320031023220233002331323 31202033230222332321223303212210221311131203 12
	Precoder	23332322221002301122121131231120220300021230 21 32002212031111211201112130233322023010123312 33
L2	PRBS	1100101111100001111101110111011001100110011100011100011000011000011101110000011001100000011 10 0011011000011000101011000110010011101010100011001001000011100111101110101011001100100101010 1
	Gray code	20322002232323202020230230200200232300202000 23 02130130332013102333302031002312323332020311 11
	Precoder	22111311120330220022031122000222033000220000 21 02300122120012311212133123133011203033113010 10
L3	PRBS	0110111101000111101111101011001101111111000111101101011101111001000010110001011001010111110 00 1001011010111110010100101100010011111000010101101011001001111110001010110111010010001011111 00
	Gray code	13221012322332021223022133232220301130320332230 31133220331130312200332113102220111323310112 20
	Precoder	12023102111211332021333212033312232130221202 13 32303331210122102000302321002022323021231011 13

Slide 14

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underline first symbol to indicate precoder init per 94.2.2.6?

put arrows denoting order

note first and 2nd TFW

kclusted, 10/24/2012

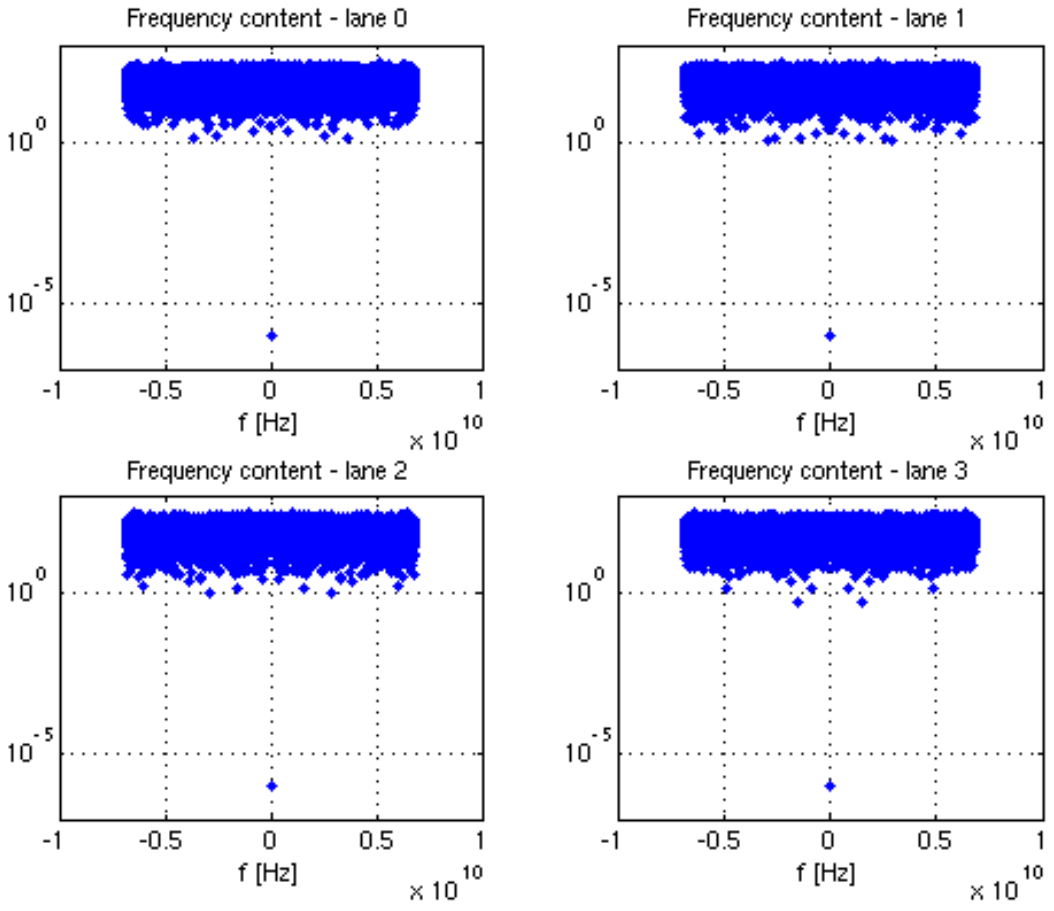
Training pattern features

- The resulting sequences are DC balanced, quasi-white and have low correlation between lanes
- Distribution of voltage levels is nearly uniform
- Distribution of transitions between level is nearly uniform

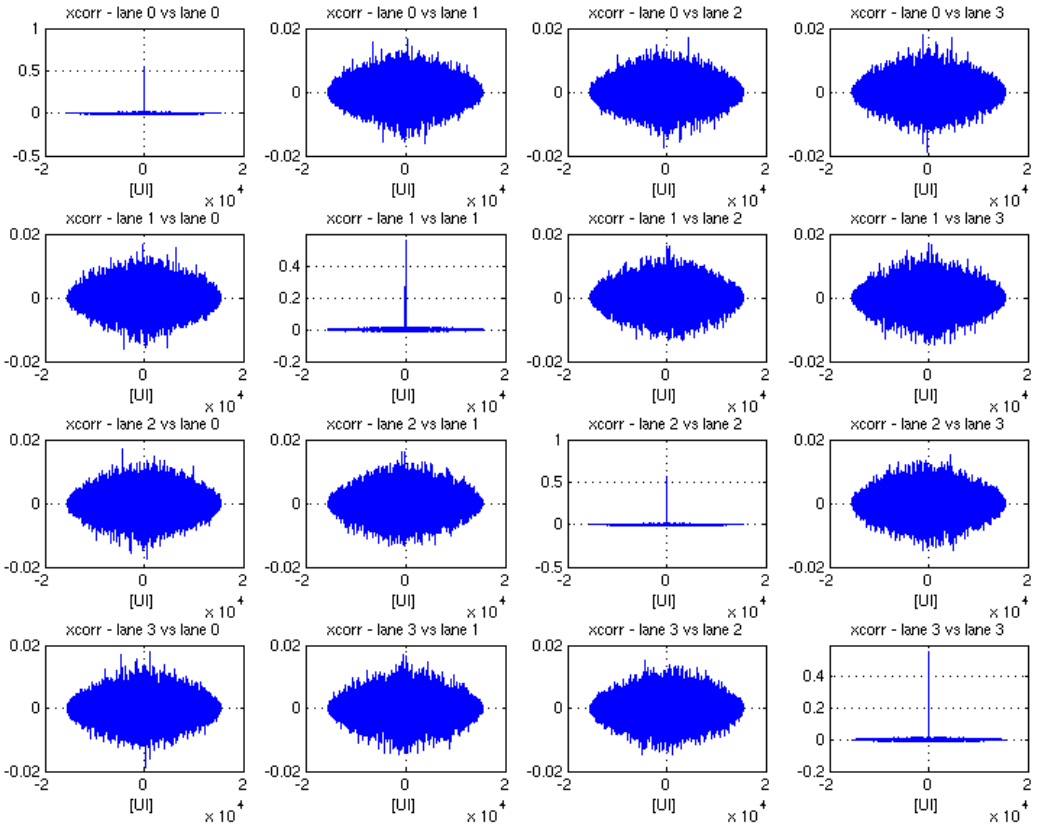
Discussion

BACKUP

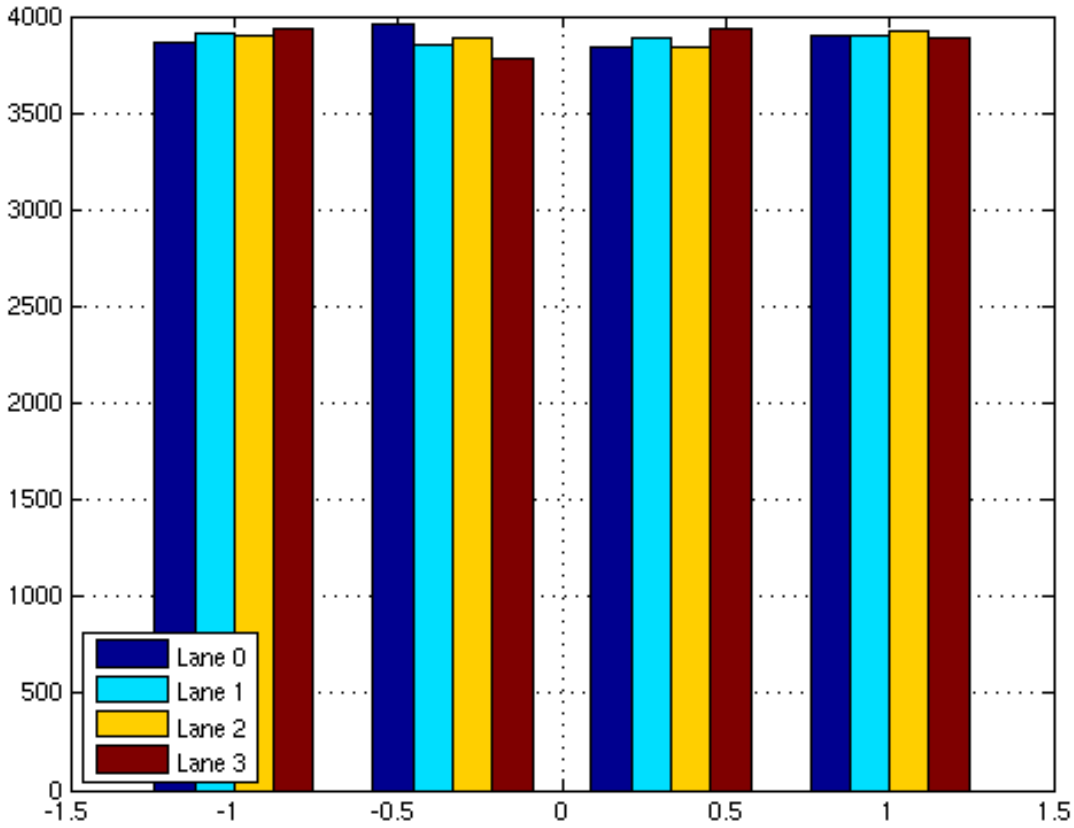
Patterns are quasi-white and DC balanced



Low correlation between lanes

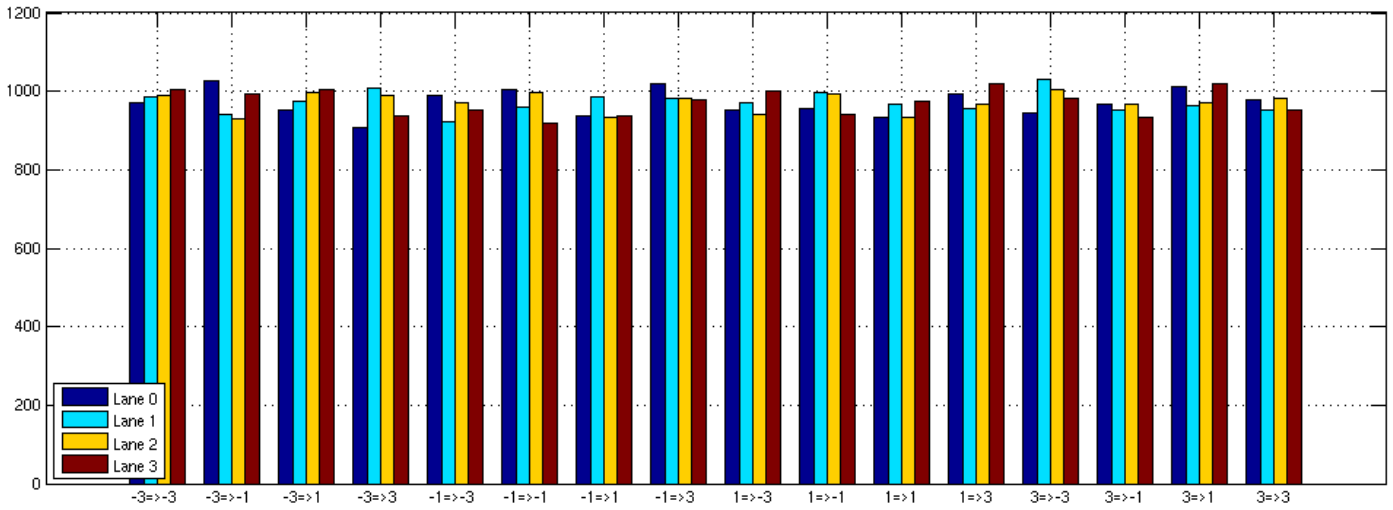


Level distribution



PRBS pattern portion only

Transition distribution



k27 of pattern only

kclusted, 10/22/2012