25Gb/s VSR LINK DATA
01/24/2011

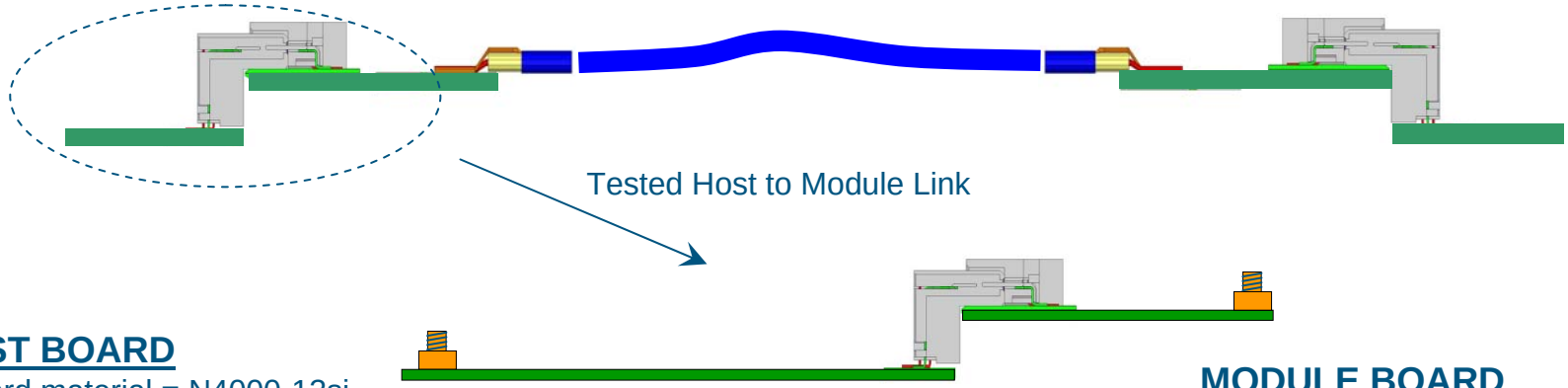
Reference document: shanbhag01_0111.pdf

presented at the IEEE 802.3 Interim Meeting, fort Lauderdale, Florida

Tyco Electronics

PASSIVE COPPER CABLE ASSEMBLY

Tested Link Description



HOST BOARD
- Board material = N4000-13si
- Trace length = **4" and 7"**
- Trace geometry = stripline
- Trace width = 5 mils
- Differential trace spacing = 6 mils
- PCB thickness = 0.093"
- 2 signal layers
- 6 ground planes
- Layer connection = layer 2 (near top)
- Counterbored (4-8mil stub)

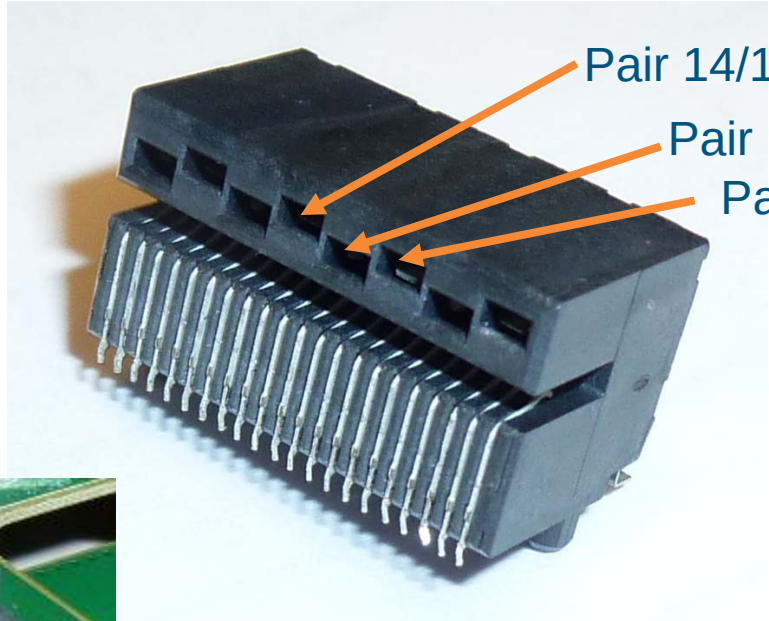
CONNECTOR
- QUADRA
- 2 piece connector design
- All 8 high speed pairs on top of the module board
- No vias required on module PCB
- Approximately the size of QSFP

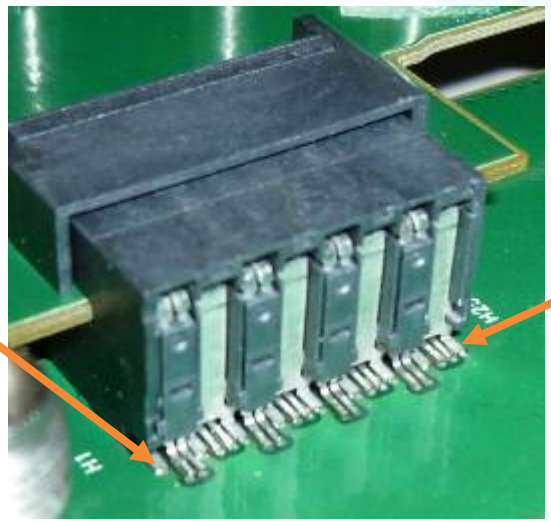
MODULE BOARD
- Board Material = N4000-13si
- Trace length = 1.25"
- Trace geometry = μStrip
- Trace width = 7 mils
- Differential trace spacing = 5 mils
- PCB thickness = 1 mm

- Data is in .s4p format for through and corresponding near and far end aggressors
  - Pair 8-9 is the victim.
  - Pair 11-12 is adjacent aggressor
  - Pair 14-15 is aggressor two aways in upper row
- Data includes SMA test points.

CONNECTOR TEST SET-UP

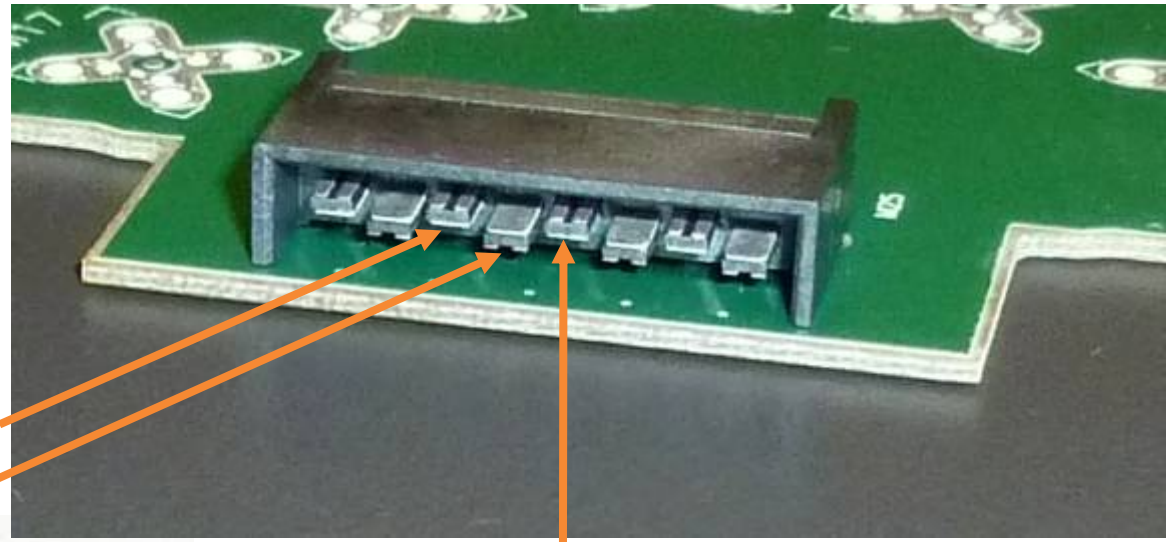
Quadra Receptacle





CONNECTOR TEST SET-UP

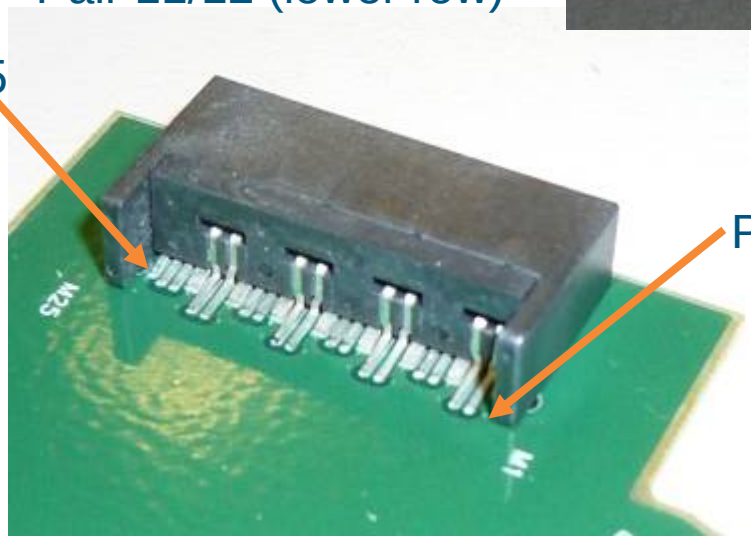
Quadra Plug



Pair 8/9 (upper row)

Pair 11/12 (lower row)

Pair 14/15 (upper row)



Pin 25

Pin 1

ICN LIMIT VALUES

ICN Limit Values used in presentation "shanbhag_01_0111" on 01/12/2011 at the IEEE802.3 meeting in Fort Lauderdale, Florida are below,

$\sigma_x <= \sigma_{x,max}$ = 10, for 3 <= IL <= 5.3

= 12.4 - 0.45*IL, for 5.3 < IL <= 25.5