100Gb/s MEASURED BACKPLANE CHANNELS

100Gb/s Ethernet Electrical Backplane and Twinaxial Copper Cable Assemblies Study Group

March 2011 IEEE 802 LMSC Plenary Session

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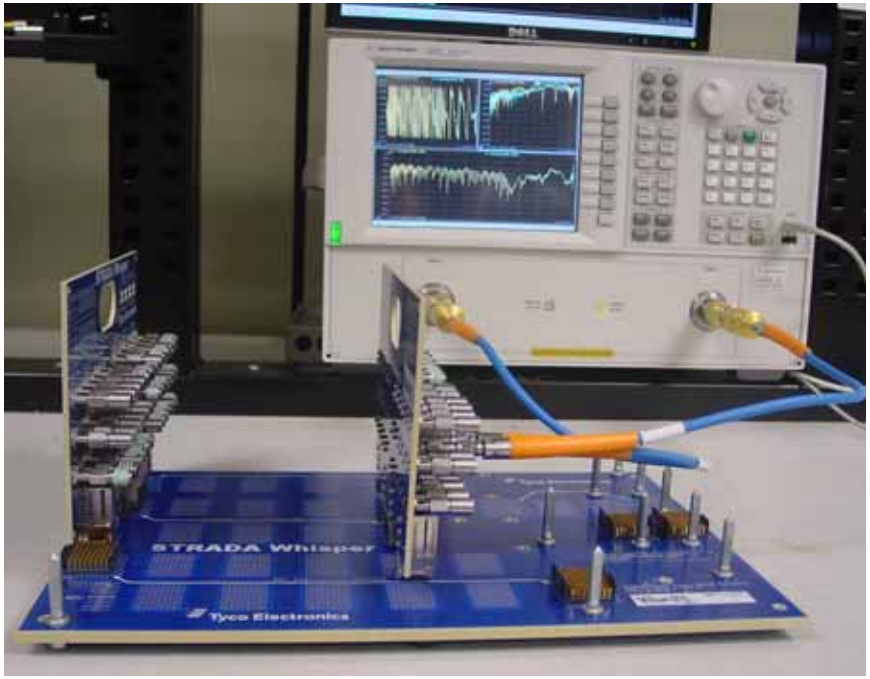
STRADA WHISPER BACKPLANE CHANNEL

27” Link Test Set-up



H17-H18	G11-G12
G17-G18	G14-G15
F17-F18	F14-F15

- All data is measured and include test points
- Measurements are pair G14-G15 centric .s4p files
- Near End and Far End measurements for 5 aggressors

DAUGHTER CARD

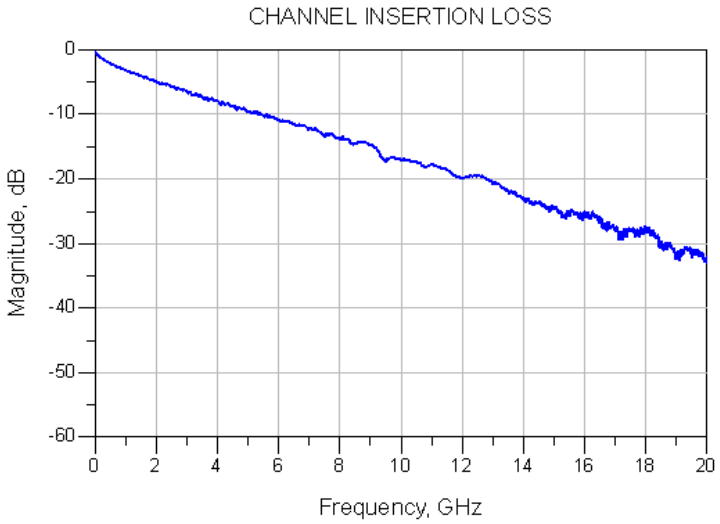
- Board Material = Megtron6 VLP
- Trace length = 5”
- Trace geometry = Stripline
- Trace width = 6 mils
- Differential trace spacing = 9 mils
- PCB thickness = 110mils, 14 layers
- Counterbored vias, 1 – 6mil stub
- Test Points = 2.4mm (included in data)

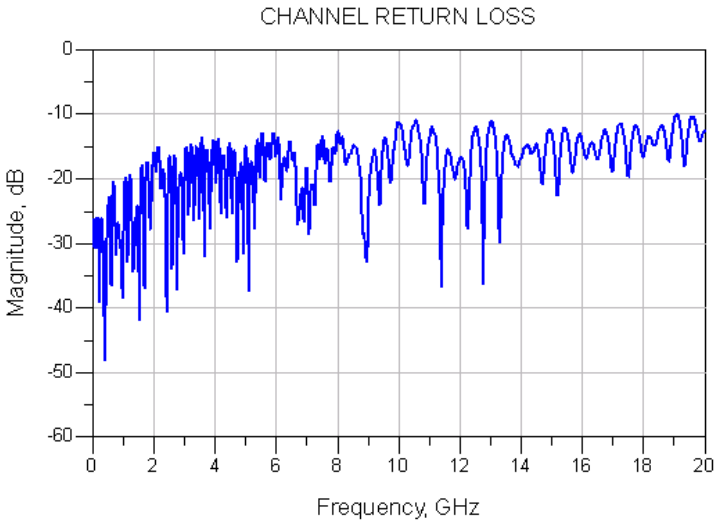
BACKPLANE

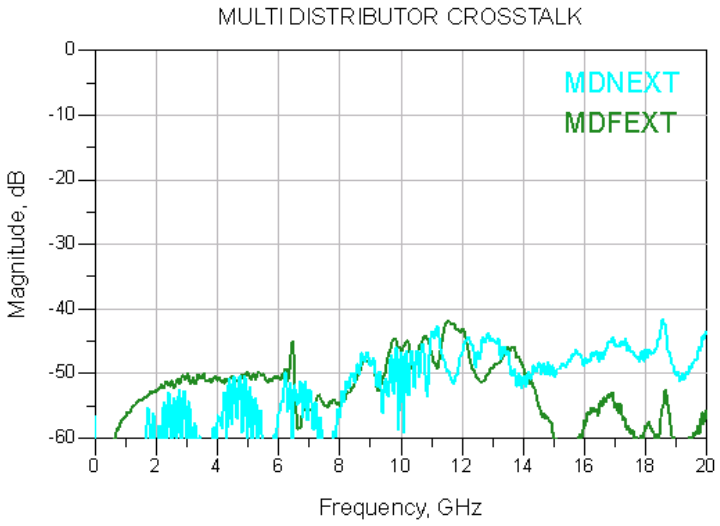
- Board Material = Megtron6 HVLP
- Trace length = 17”
- Trace geometry = Stripline
- Trace width = 8 mils
- Differential trace spacing = 13 mils
- PCB thickness = 200 mils, 20 layers
- Counterbored vias, 1 – 6mil stub

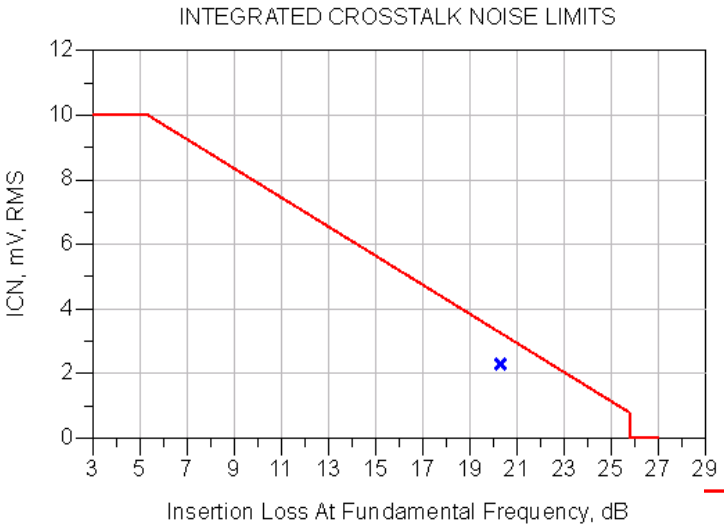
STRADA WHISPER BACKPLANE CHANNEL

27” Link Measured Data

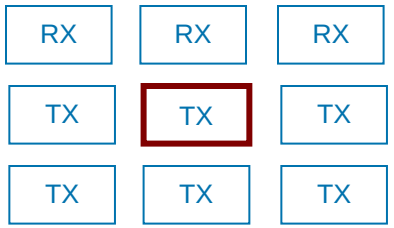








Aggressors for 2nd adjacent column obtained using symmetry



- Data Rate [fb] = 25.8 Gbps
- Rise Time [Tnt,Tft] = 8ps [20-80%]
- Fmax=25.8GHz
- Df = 0.01GHz

$s_x <= s_{x,max} = 10$, for $3 <= IL <= 5.3$

$= 12.4 - 0.45*IL$, for $5.3 < IL <= 25.5$

Where IL is Insertion Loss in dB at half baud rate