Feasibility of 100 Gb/s operation on installed backplane channels

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May 2011

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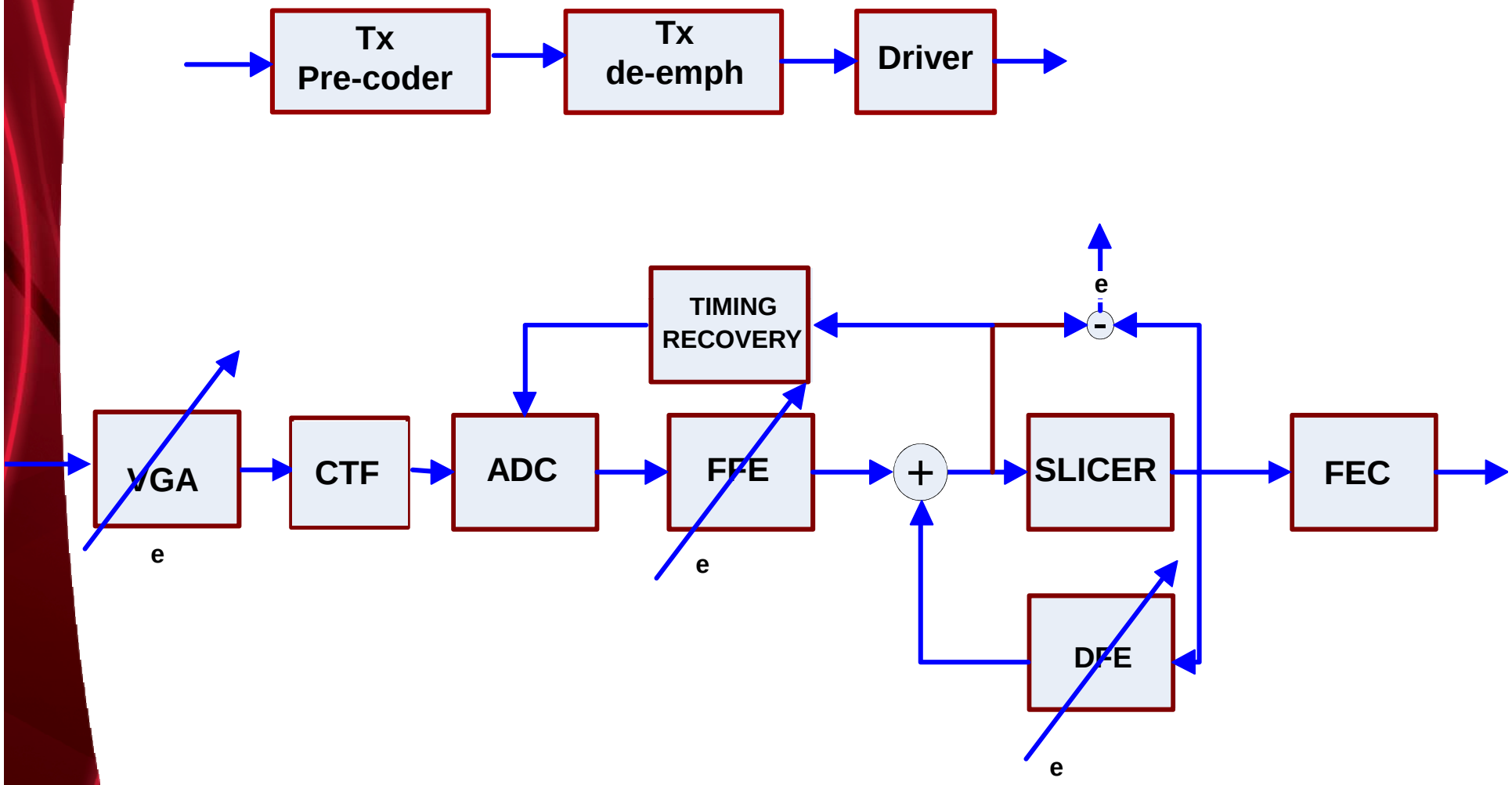
Outline

- **Identify a line code/modulation technique that can**
  - Operate on a broad range of material types
  - Permit a broad range of receiver architectures
  - Allow trading material cost against receiver complexity
- **An analog/digital ADC based receiver architecture is feasible for supporting 100 Gbps operation on the installed base of backplane channels**
- **A primarily analog receiver architecture is feasible for channels built using advanced materials**

100GBASE-KR4 Digital Transceiver Block Diagram



Transmitter Feasibility

- Transmitters have been built with 10 taps of de-emphasis for NRZ designs at 10 Gbps[1]
- Literature reports of an 5 tap de-emphasis PAM4 transmitter at 20 Gbps[2]
- High precision DAC's have been fabricated around rates of 24 Gbps (12 Gsamples/sec)[3,4]
- PAM4 transmitter with 3 tap de-emphasis should be feasible in current technology at a reasonable power
- PAM4 transmitter is assumed for the remainder of this presentation

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[1] D.Crivelli et. al., "Architecture and Experimental Evaluation of a 10Gb/s MLSD based Transceiver for Optical Multimode applications", *Proceedings of ICC*, May 2008

[2] Z.Gao et. al., "A 10 Gb/s Wire-line Transceiver with Half Rate Period Calibration CDR", *Proceedings of IEEE ISCAS*, May 2009

[3] A.Amirkhany et. al., "A 24 Gb/s Software Programmable Analog Multi-Tone Transmitter", *IEEE Journal of solid state circuits*, April 2008

[4] Greshishchev, Y.M. et. al., "A 56GS/S 6b DAC in 65nm CMOS with 256×6b memory", *Proceedings of the IEEE ISSCC*, April 2011

100GBASE-KR4 Rx Architecture

- Receiver assumes using a mixed-signal (AFE+DSP) data path at 25.78 Gbps
- Equalization is performed using a FFE/DFE architecture
- Transmit de-emphasis allows better performance while simplifying receiver complexity
- Assume a 5 dB coding gain FEC to allow for sufficient implementation penalty in the design
- We will first discuss the feasibility of a ADC-based digital architecture and follow it up with an analog architecture

Simulation Setup

- **Study focused on the same installed base of 10GBASE-KR/40GBASE-KR4 compliant channels that we presented in January[5]**

- **MATLAB simulations**
  - Pulse Response “Frequency-domain” Analysis with MMSE optimization

- **Simulation Parameters**
  - Tx Launch = 1Vppd
  - $T_{rise/fall}$ = 20ps
  - Tx RJ = 10mUI rms
  - Rx RJ = 10mUI rms
  - AWGN PSD = -147.3 dBm/Hz double-sided
  - Each crosstalk aggressor added individually (not power summed)
  - Package Model: s-parameters from current 10GBASE-KR production package
  - SNR Target = 24.0 dB (corresponds to BER = 10^{-12})

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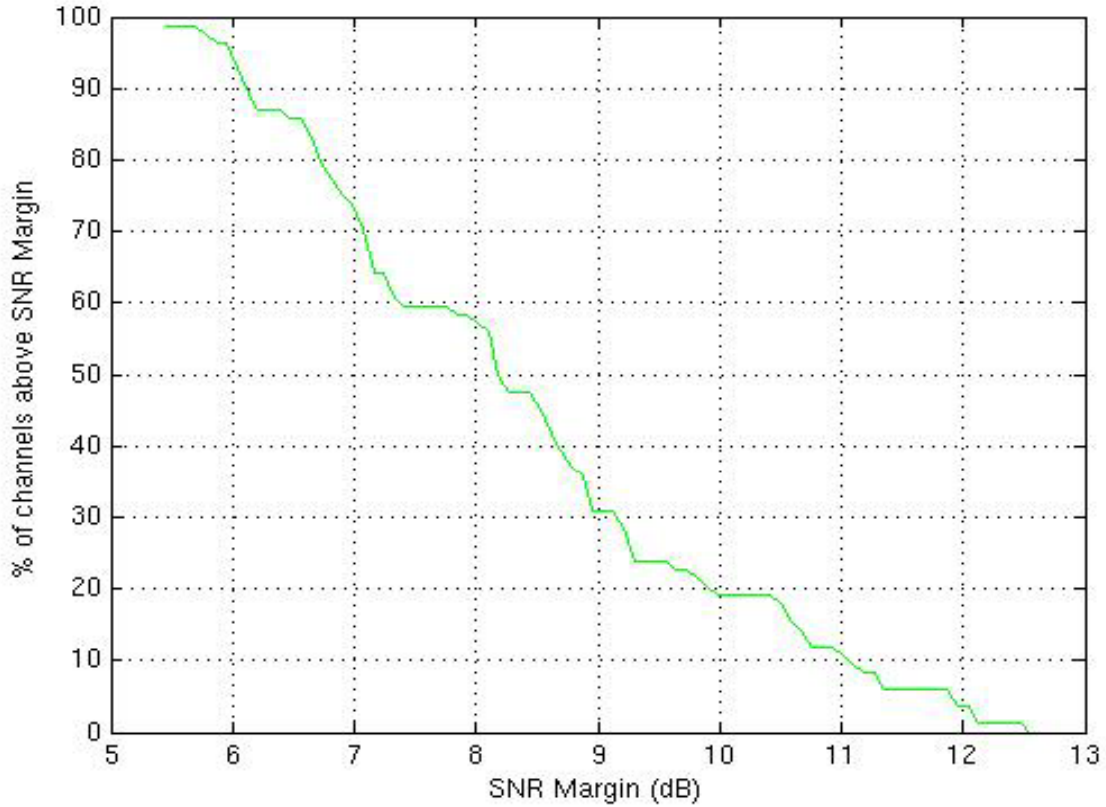
[5] H.Frazier and V.Parthasarathy , Study of 100 Gb/s on 40GBASE-KR4 Channels, IEEE, Ft. Lauderdale, FL, Jan 2011

Digital Receiver performance over KR-compliant installed base



- 3 tap TX de-emphasis, 32 tap FFE, 2 tap DFE, Continuous time filter (CTF), 6 ENOB ADC and FEC with 5dB coding gain
- Full coverage on the installed base feasible

ADC Feasibility

- A 6 bit low power ADC at 10 Gbps KR line rate in 65 nm has been demonstrated in literature[6]
- For coherent receivers in optical communications, a 8 bit ADC at 56 Gbps has been demonstrated showing that high ENOB, high speed ADC's are feasible[7]
- POWER : 260 mW (extrapolation from reference 7)
- NOTE: Technology changes from 65 nm to 28 nm allow 50% increases in speed to further scale power
- Should be sufficient in accommodating the 25% increase in ADC speed from 10 Gbps KR to 25 Gbps PAM4 line rates

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[6] J.Cao et. al., A 500 mW ADC-Based CMOS AFE With Digital Calibration for 10 Gb/s Serial Links Over KR-Backplane and Multimode Fiber", *IEEE Journal on Solid State Circuits*, June 2010

[7] http://www.fujitsu.com/downloads/MICRO/fme/dataconverters/OFC-2010-56Gss-ADC-Enabling-100GbE.pdf

Equalizer (FFE) Feasibility

- Synthesized a parallelized 32 tap FFE with 40nm std cell TSMC library (effective bit-rate is around 26 Gbps)
- Develops on a Fast FFE implementation[8]
- Production part type synthesis with 20% timing margin to worst PVT corner (to estimate feasibility, area and power)
- Straightforward Fast FFE implementation, further optimizations possible in tap widths and adders for smaller area, power and latency
- POWER (Synopsys DC estimated pre-layout, static + dynamic): around twice that of a 10 tap KR FFE implementation at 10.5 Gbps

[8] Richard Blahut, “Fast Algorithms for Digital Signal Processing”, Addison-Wesley, 1985

Equalizer (DFE) Feasibility

- Synthesized a 2 tap look-ahead[9] PAM4 DFE with 40nm std cell library (effective bit-rate is around 26 Gbps)
- Production part type synthesis with 20% timing margin to worst PVT corner (to estimate feasibility, area and power)
- Straightforward implementation used, further optimizations possible in look-ahead structure for lower area/power/latency
- POWER (Synopsys DC estimated pre-layout, static + dynamic) : similar to a 4 tap NRZ DFE at KR rates of 10.5 Gbps

[9] Keshab K. Parhi, "Design of Multigigabit Multiplexer-Loop-Based Decision Feedback Equalizers", *IEEE Transactions On Very Large Scale Integration (VLSI) systems*, Vol. 13, No.4, April 2005

FEC Feasibility

- Block codes which provide 5 dB coding gain are readily available and have been presented at IEEE [10, 11]
- G.975 RS(255,239) already implements a FEC with 6dB gain at ~10.5 Gbps line rates
- Synthesized the RS(255,239) FEC at an effective bit rate of 25.78 Gbps with 40nm standard cells
- POWER (Synopsys DC estimated pre-layout, static + dynamic) : around 1.25 times that of a KR Fire code operating over 5 virtual lanes (25.78 Gbps)

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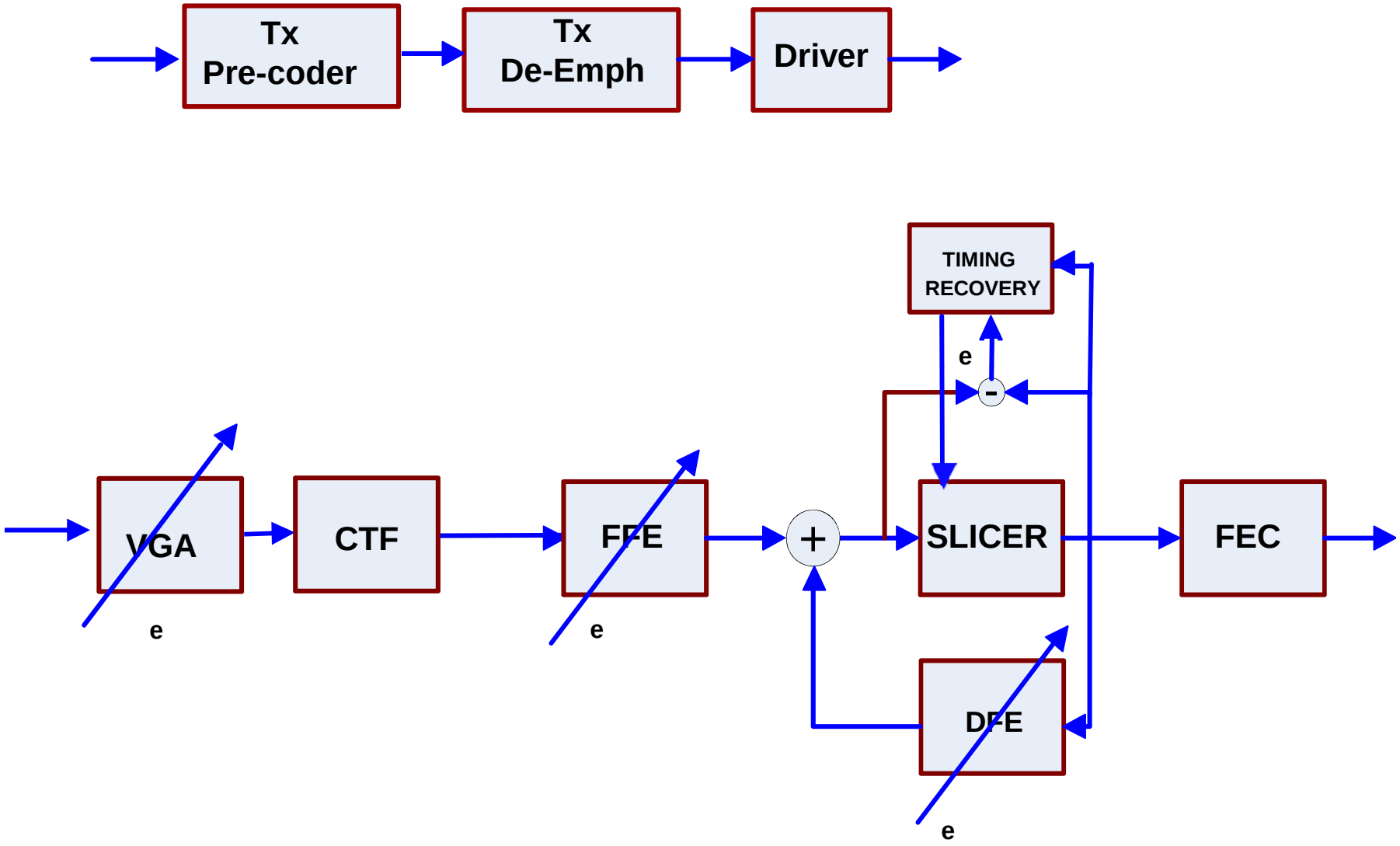
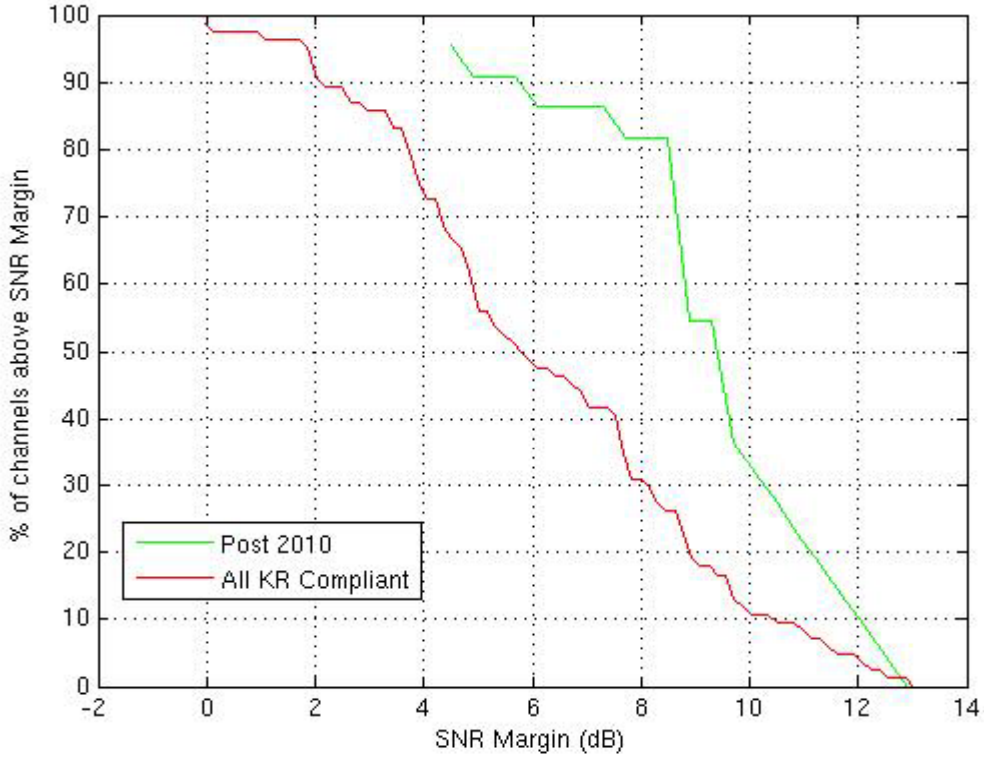
[10] S. Bhoja and M. Gustlin, http://www.ieee802.org/3/100GCU/public/mar11/gustlin_02a_0311.pdf, IEEE March 2011

[11] Z.Wang and C.J.Chen, " Feasibility of 100G-KR FEC", IEEE May 2011

100GBASE-KR4 Analog Transceiver Block Diagram



Analog Receiver performance over KR-compliant installed base



- 3 tap TX de-emphasis, 5 tap FFE, 5 tap DFE, FEC with 5dB coding gain
- Coverage improves over all KR compliant backplanes with a sliding tap DFE design (refer to backup slide)
- Post 2010 channels show adequate margin

Analog Architecture Feasibility

- **Analog FFE/DFE architectures have been demonstrated for 10GBASE-LRM channels[12]**
- **Analog DFE architectures have been presented in ISSCC for ~25Gbps backplane channels[13]**
- **A PAM4 DFE at first order will have around twice the complexity but at half the speed**

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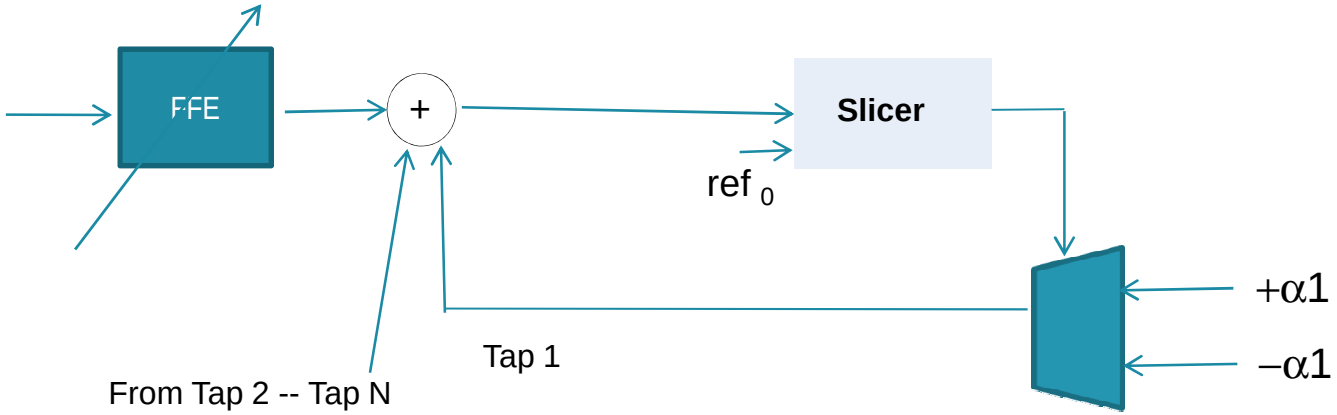
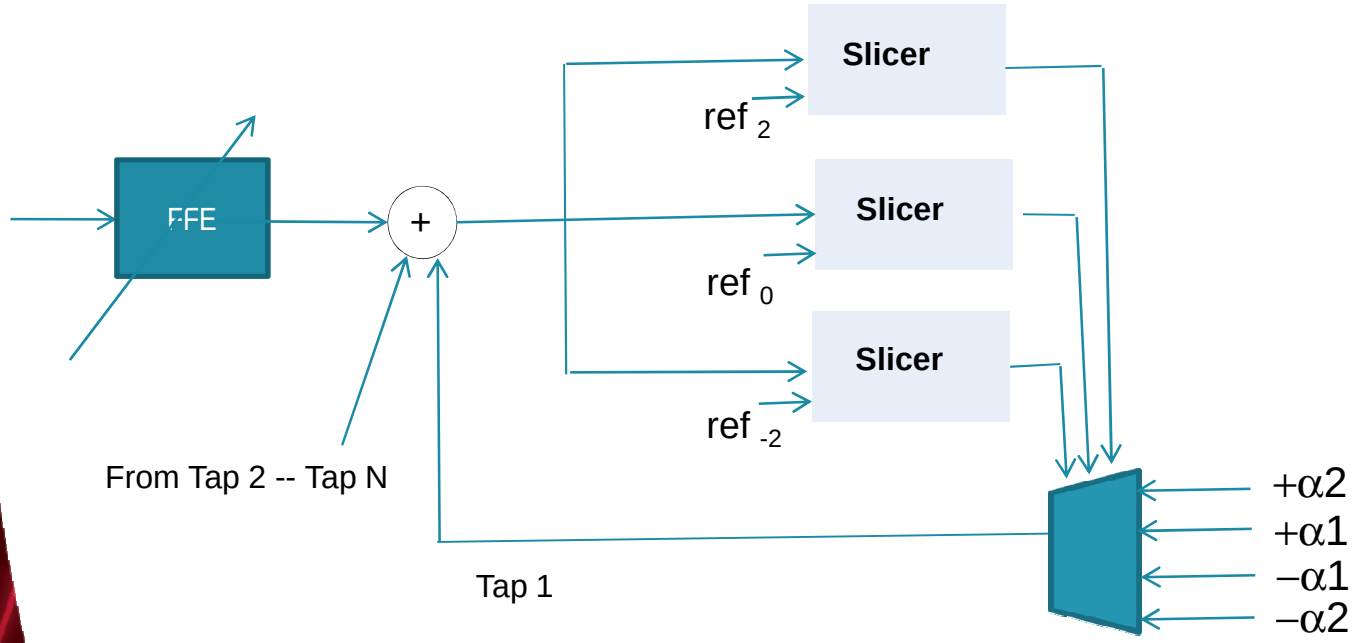
[12] S. Pavan, ``Continuous-Time Integrated FIR Filters at Microwave Frequencies", *IEEE Transactions on Circuits and Systems-II, Analog and Digital Signal Processing*, January 2004

[13] S.Quan et. al., A 1.0625-to-14.025Gb/s multimedia transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40nm CMOS, *Proceedings of IEEE ISSCC*, Feb. 2011

Conceptual Block Diagram of an Analog DFE



NRZ DFE



PAM4 DFE

Analog DFE Complexity Estimate

N tap DFE	12.5 Gbps NRZ	12.5 Gbaud PAM4 (25 Gbps)	25 Gbps NRZ
Slicer	N	3N	N
Adder	N	N	N
Mux (current sum)	N 2:1	N 4:1	N2:1
Clock	12.5 GHz	12.5 GHz	25 GHz
Complexity	1x	~2x	~2x

- **Complexity increase from 12.5 Gbps NRZ DFE → 12.5 Gbaud PAM4 (25 Gbps) DFE slightly over 2x**
- **Complexity increase from 12.5 Gbps NRZ DFE → 25 Gbps NRZ DFE slightly over 2x**
- **Complexity of a N tap 12.5 Gbps NRZ DFE → 25 Gbps PAM4 DFE roughly about the same[14]**

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[14] NOTE: Equalizing a channel signaling at F symbols per second typically requires half as many equalizer taps as signaling at 2F symbols per second

Conclusions

- **We have demonstrated that it is technically feasible to**
  - operate on a broad range of material types,
  - permit a broad range of receiver architectures, and
  - allow trading material cost against receiver complexity

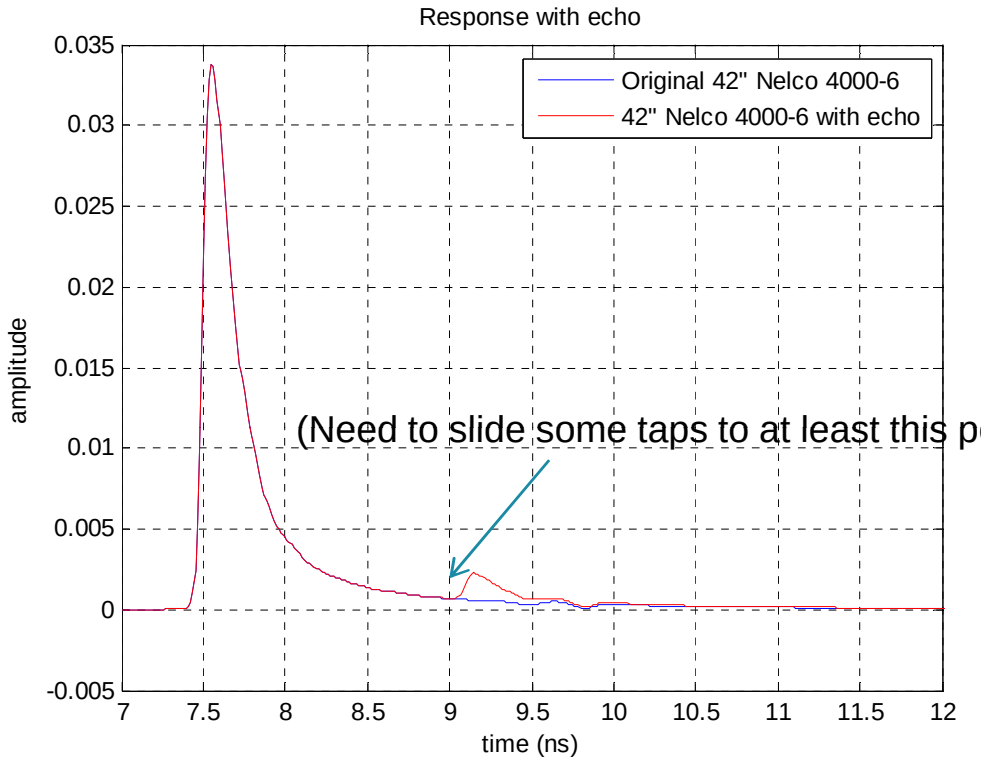
  by using PAM4 as the line code/modulation technique

- **We have examined the performance of both analog and digital PAM4 receiver architectures across an extensive database of backplane channel characteristics**

- **All of the major blocks required for an implementation are technically and economically feasible using current technology**

Backup

Sliding taps to improve performance: Example



(Need to slide some taps to at least this point to cancel echo)

- **Echo in the impulse response can be cancelled by having a larger number of FFE taps**
- **Sliding some of the DFE taps by a sufficient number of bauds can also help cancel reflections and improve SNR (in this case by about 4 dB)**