



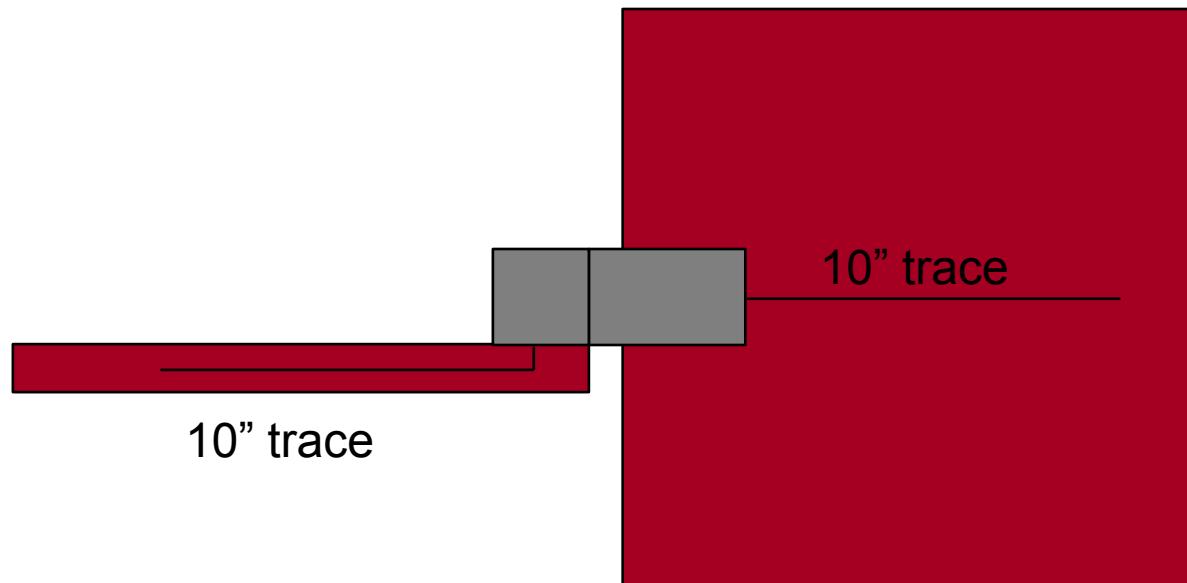
112G Channel Analysis

ExaMAX⁺ Direct-Mate Orthogonal Channel

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Purpose

- To provide channels to be used for 112G analysis.
- Channel consists of 20" of trace and one orthogonal connector, with footprints.

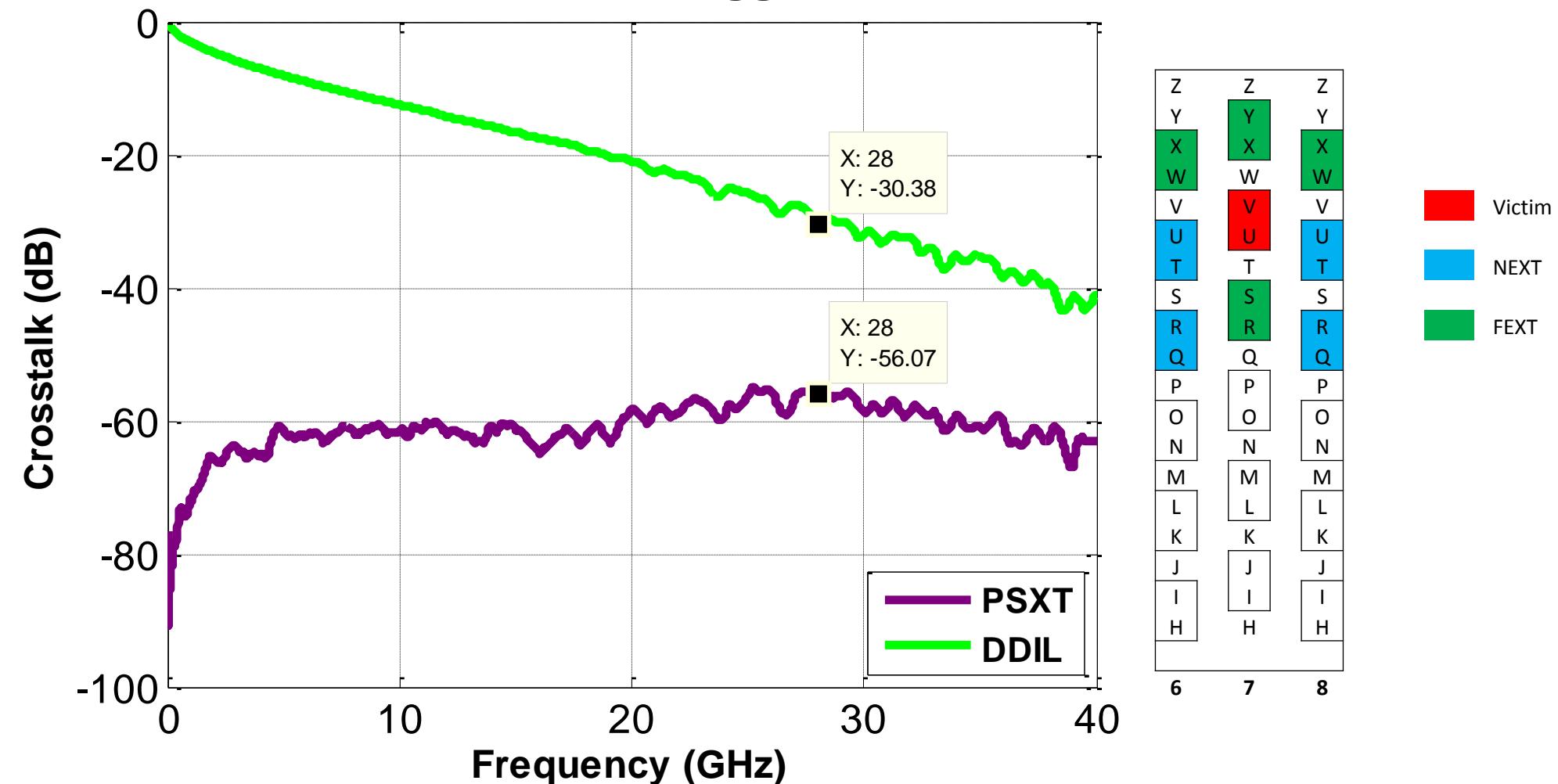


Details

- A connector was measured on test boards and then de-embedded to be used in this link.
- A 10" simulated trace was concatenated to each side of the de-embedded connector & footprints for a total channel length of 20".
- Board material is Doosan DS7409DV (N-Glass) HVLP
 - $D_k = 3.25$ & $D_{k\prime} = 0.0015$
 - Board thickness = 77 mils
 - Trace width \ spacing = 9.6 \ 6.5 mils
 - This is the material used in the test boards as well as the simulated traces.
- Touchstone files go from 10 MHz to 40 GHz in 10 MHz steps

Insertion Loss and PSXT

ExaMAX+ Orthogonal Link - PSXT
Pair UV7 - Mixed Aggressors



IEEE P802.3cd COM and ERL

ExaMAX+ Orthogonal Link Config. 1		
	Case 1	Case 2
UV7	8.61	8.26

```
PASS... ERL11 = 26.994 dB; ERL22 = 26.232 dB;
```

```
ans =  
  
    Z11: 0  
    Z22: 0  
    ERL11: 26.9938  
    ERL22: 26.2316  
    ERL: 26.9938  
code_revision: '2.26'  
config_file: 'D:\Users\AZambell\Desktop\Work_Folder\IEEE_and_OIF\config_com_ieee8023_93a=50GBASE-KR_cdD3p1.xls'  
    Z_t: 50  
file_names: '"KR_50G_PAM4 --Thru_Ortho_C1_Pr_14_to_Pr_5"'
```

IEEE P802.3cd COM Spreadsheet

Table 93A-1 parameters

Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.8e-4 1.8e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.25:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(1)	[-0.25:0.05:0]		[min:step:max]
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	10.625	GHz	
f_p1	10.625	GHz	
f_p2	53.125	GHz	
A_v	0.415	V	tdr selected
A_fe	0.415	V	tdr selected
A_ne	0.604	V	tdr selected
L	4		
M	32		
N_b	12	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	1.64E-08	V^2/GHz	
SNR_TX	32.5	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control

DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
Display frequency domain	1	logical
CSV_REPORT	1	logical
RESULT_DIR	IEEE_802p3cd_D2p0_BP_{date}\	
SAVE FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	IEEE_802p3cd_D2p0_BP	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_RX_TERM	0	logical
T_r	1.20E-02	ns
FORCE_TR	1	logical
Non standard control options		
INC_PACKAGE	1	logical
IDEAL_RX_TERM	0	logical
INCLUDE_CTLE	1	logical
INCLUDE_TX_RX_FILTER	1	logical
COM_CONTRIBUTION	0	logical
New 'cd exploratory		
TDR	1	logical
WC_PORTZ	1	logical

Table 93A-3 parameters

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[95 95]	Ohm

Table 92-12 parameters

Parameter	Setting	Units
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_z_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

IEEE P802.3cd ERL Spreadsheet

Table 93A-1 parameters

Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.8e-4 1.8e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.25:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(1)	[-0.25:0.05:0]		[min:step:max]
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	10.625	GHz	
f_p1	10.625	GHz	
f_p2	53.125	GHz	
A_v	0.415	V	tdr selected
A_fe	0.415	V	tdr selected
A_ne	0.604	V	tdr selected
L	4		
M	32		
N_b	12	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	1.64E-08	V^2/GHz	
SNR_TX	32.5	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
Display frequency domain	1	logical
CSV_REPORT	1	logical
RESULT_DIR	ults\KRorCA_50G_PAM4_{date}\	
SAVE FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KRorCA_50G_PAM4	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	0.012	ns
FORCE_TR	1	logical

Non standard control options		
COM_CONTRIBUTION	0	logical
TDR	1	logical
ERL	1	logical
Z_t	50	ohms
ERL_ONLY	1	logical
TR_TDR	0.0189	ns
TDR_duration	10	
TDR_f_BT_3db	19.921875	GHz
TDR_Butterworth	1	logical
beta_x	10700000000	
rho_x	0.44	
fixture delay time	0.00E+00	
Grr_limit	0	
ERL_FOM	0	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.73e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	95	Ohm (tdr sel)

Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_Z_c	6.191E-03	ns/mm
z_bp (TX)	110	Ohm
z_bp (NEXT)	151	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

set to zero for no fixture. For a CR cable this is determined outside of this program

Update

- Re-ran ERL using version 2.26.