Synthesized CR End to End Models for Objective Work

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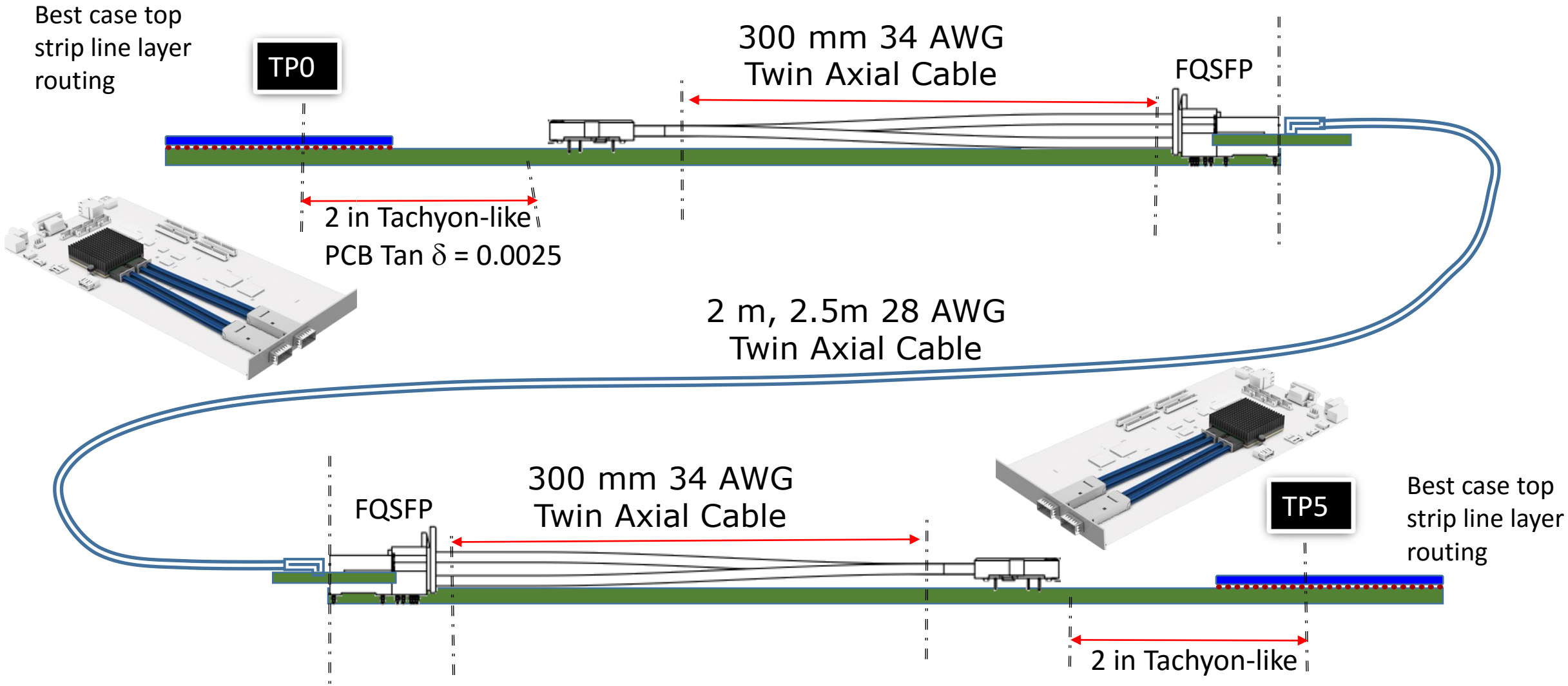
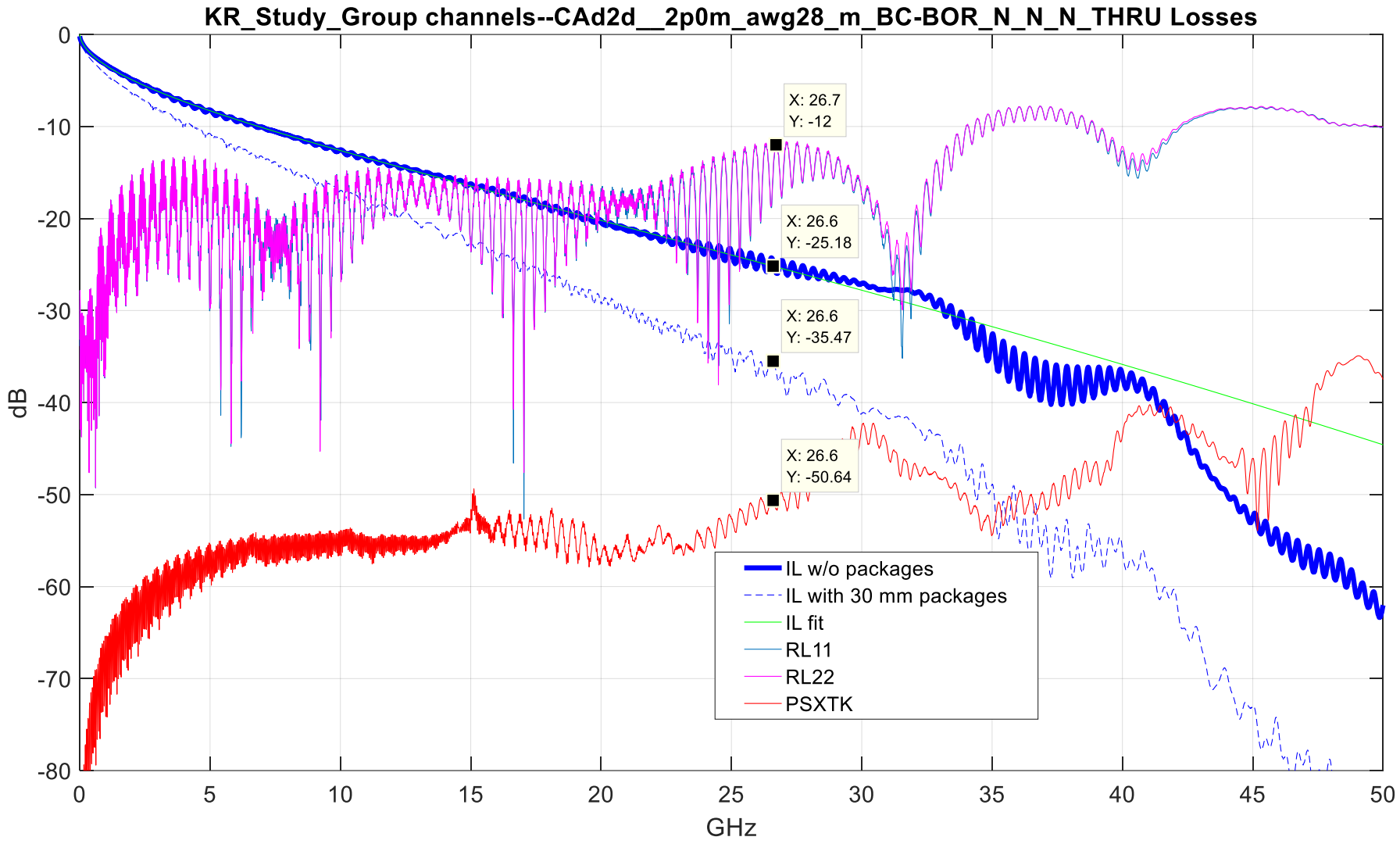
Channel description

- Synthesize complete best case channel for 100G CR cabling
- Use this to determine a loss limit for the 100Gel CR objective
  - Real cable reaches could be determined from this limit
- For this experiment flyover cabling is assumed on the line cards and a model of 2.0 m and 2.5 m of 28 AWG cable at 25 degrees C was used.
  - 3 FEXT, 4 NEXT, 1 THRU
- All models used were derived from modeling simulations tuned from measurements.
- It's likely manufacturing constrains for channels will not be this good
- For this experiment, BGA routing break outs are mostly electrically invisible
  - This will be called a BC BOR (best case break out region)
  - Practical channels will likely be worse
- All routing in the models have a differential impedance of 100 ohms
- It is likely routing closer to 90 ohms will perform better.

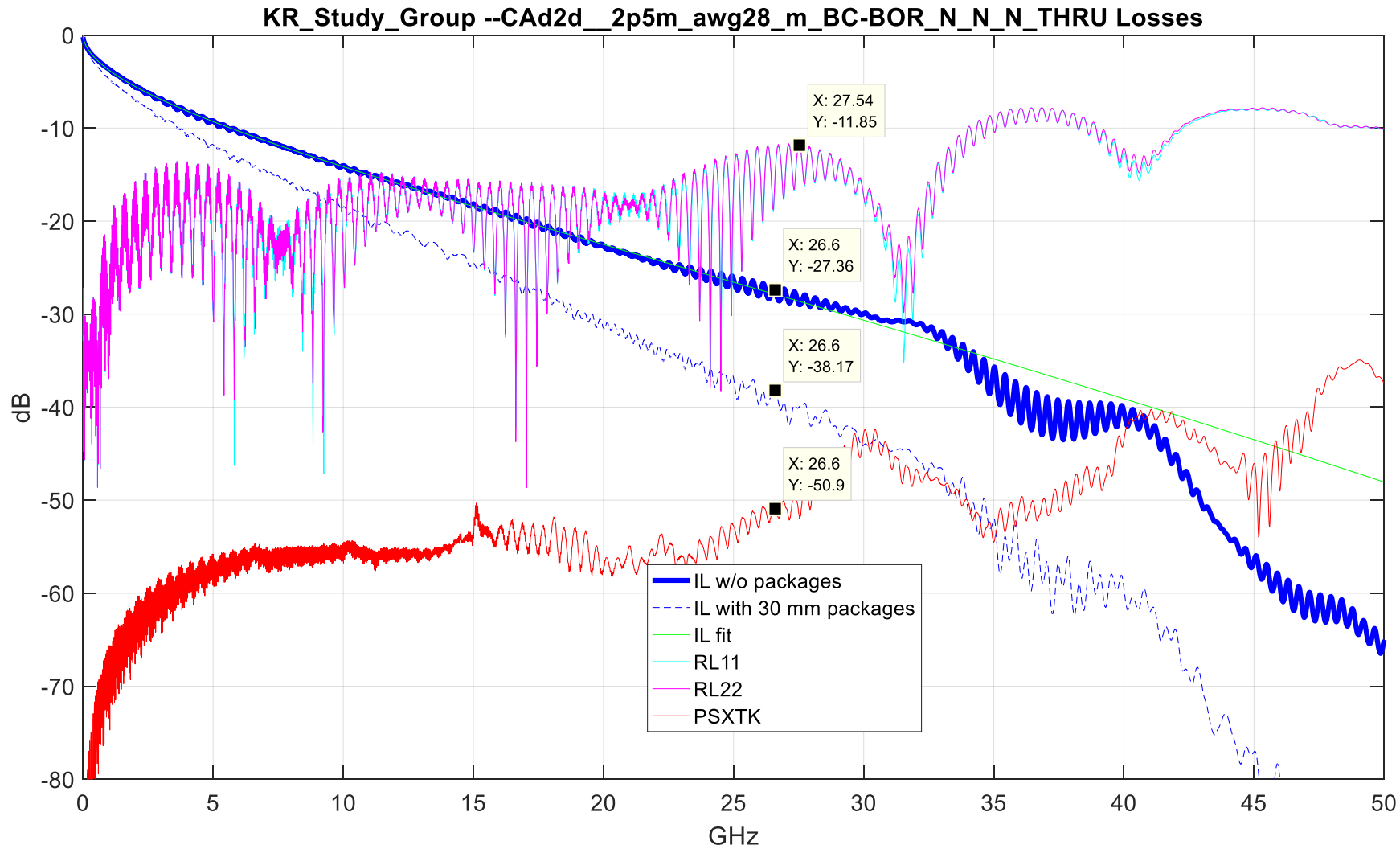
System Topology Overview: CR



2.0 dB Cable Loss and Crosstalk Plots



2.5 dB Cable Loss and Crosstalk Plots



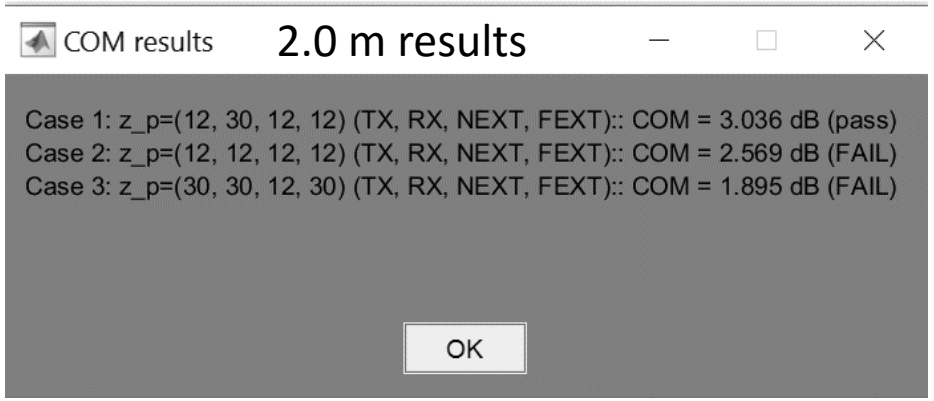
COM Configuration Sheet Experiment

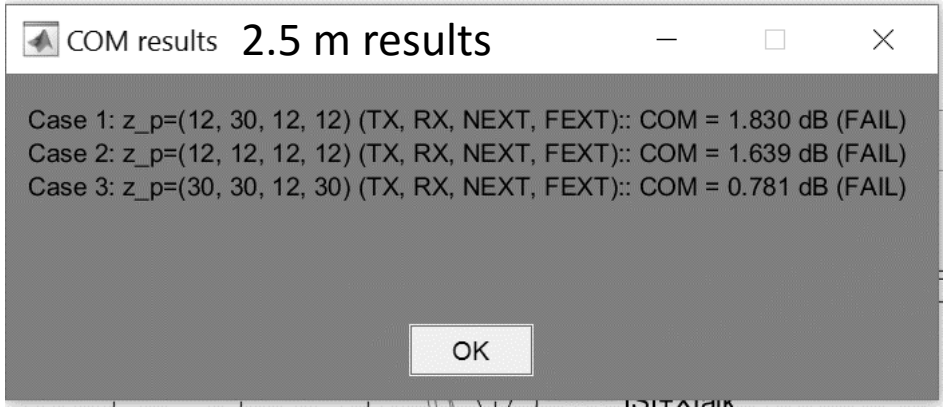
Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2 3]		[test cases to run]
z_p (TX)	[12 12 30]	mm	[test cases]
z_p (NEXT)	[12 12 12]	mm	[test cases]
z_p (FEXT)	[12 12 30]	mm	[test cases]
z_p (RX)	[30 12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.25:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.15]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
A_v	0.45	V	tdr selected
A_fe	0.45	V	tdr selected
A_ne	0.63	V	tdr selected
L	4		
M	32		
N_b	38	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	1.64E-08	V^2/GHz	
SNR_TX	35	dB	tdr selected
R_LM	0.96		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

I/O control			
DIAGNOSTICS	1	logical	
DISPLAY_WINDOW	1	logical	
Display frequency domain	1	logical	
CSV_REPORT	1	logical	
RESULT_DIR	.\results\100G_Study_Group_{date}\		
SAVE_FIGURES	0	logical	
Port Order	[1 3 2 4]		
RUNTAG	KR_Study_Group		
Receiver testing			
RX_CALIBRATION	0	logical	
Sigma BBN step	5.00E-03	V	
IDEAL_TX_TERM	0	logical	
T_r	7.00E-03	ns	
FORCE_TR	1	logical	

Non standard control options			
COM_CONTRIBUTION	0	logical	
TDR	0	logical	

g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	1.328125	GHz	





Summary

- 2 m and longer cables may require a very strong signaling architecture
- 2 m cables may be possible but will likely require heavy lifting for the chips and interconnect.
- Potential Working Group Activities
  - Determine how much relief could be gained with larger gage cable
    - Perhaps only 10% reach improvement.
  - Determine how much relief could be gained with 90 ohm target impedance
- 2.0 m cable objectives will likely require substantial work in the task force
- Will there be enough margin left for interoperable assemblies?