Initial Backplane Models for IEEE 802.3 100 Gb/s per Lane Electrical Study Group

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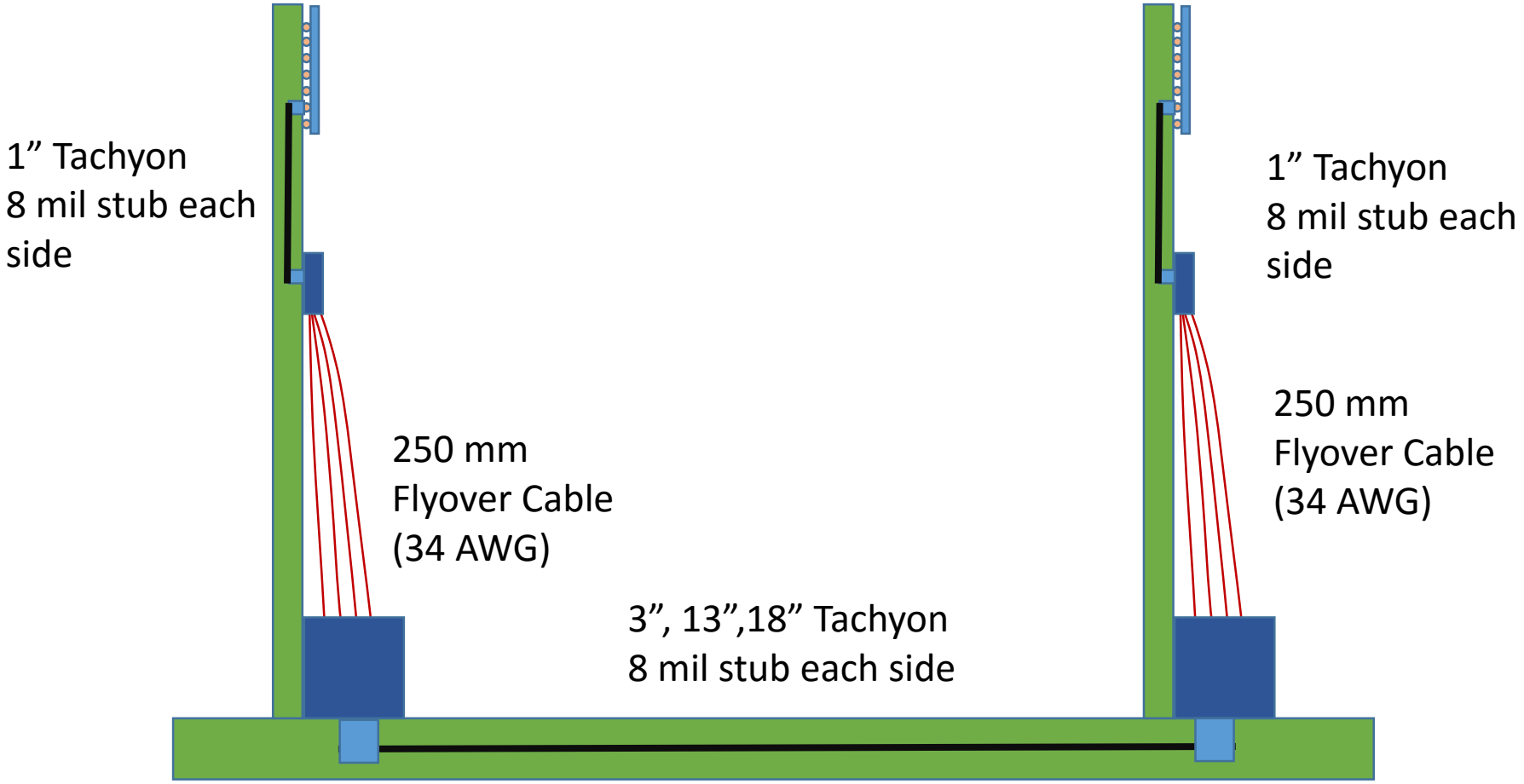
Summary

- 3 models of best case backplane
  - Short and longer trace on a low loss backplane (D_f=0.0025)
  - Line cards have flyover cables from the board backplane connector to the a connector on the board
- This are best case models
  - All traces and cables are a nominal 100 ohm Impedance
  - BGA and connector breakout routing is best case top layer and back drilled
- Manufactured channels will not be this good
  - Manufacturing and design variations
  - These channel are just to put “foot on the ground” for Study group assessment
- Pin assignment not tuned for NEXT reduction

Three Flyover Tachyon Backplane Channels

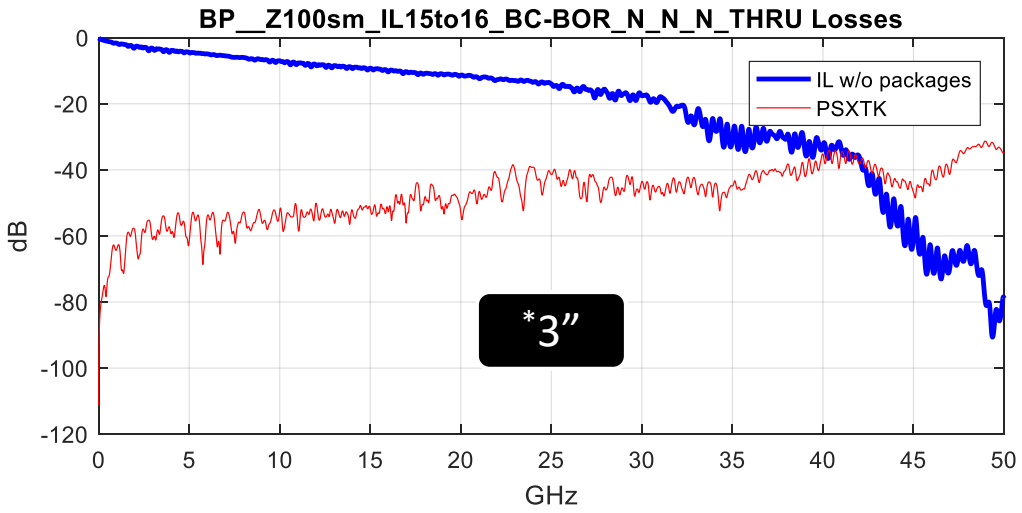


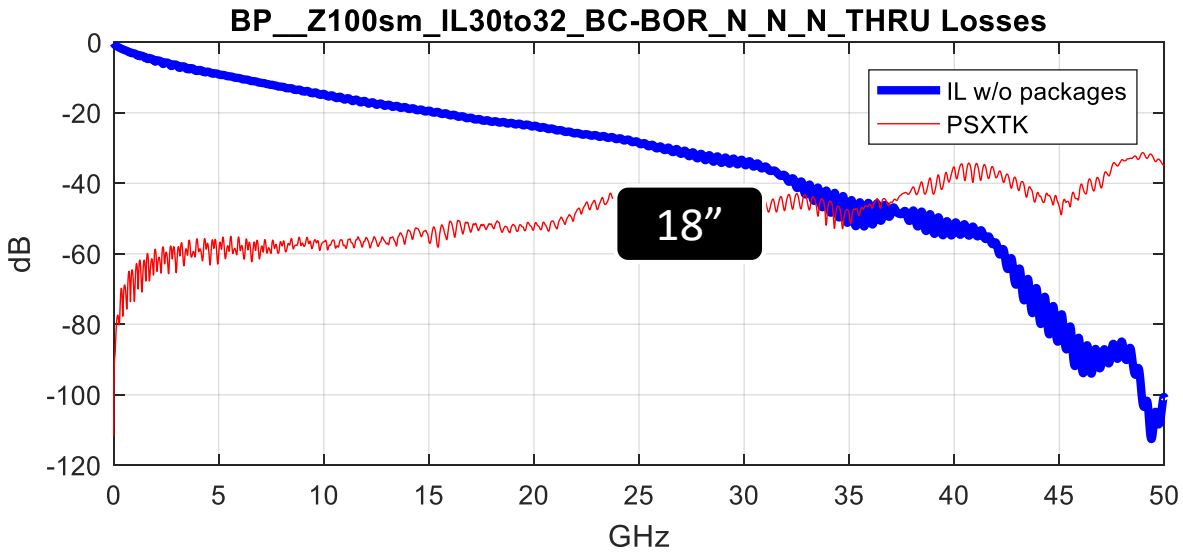
Some data on the three channels

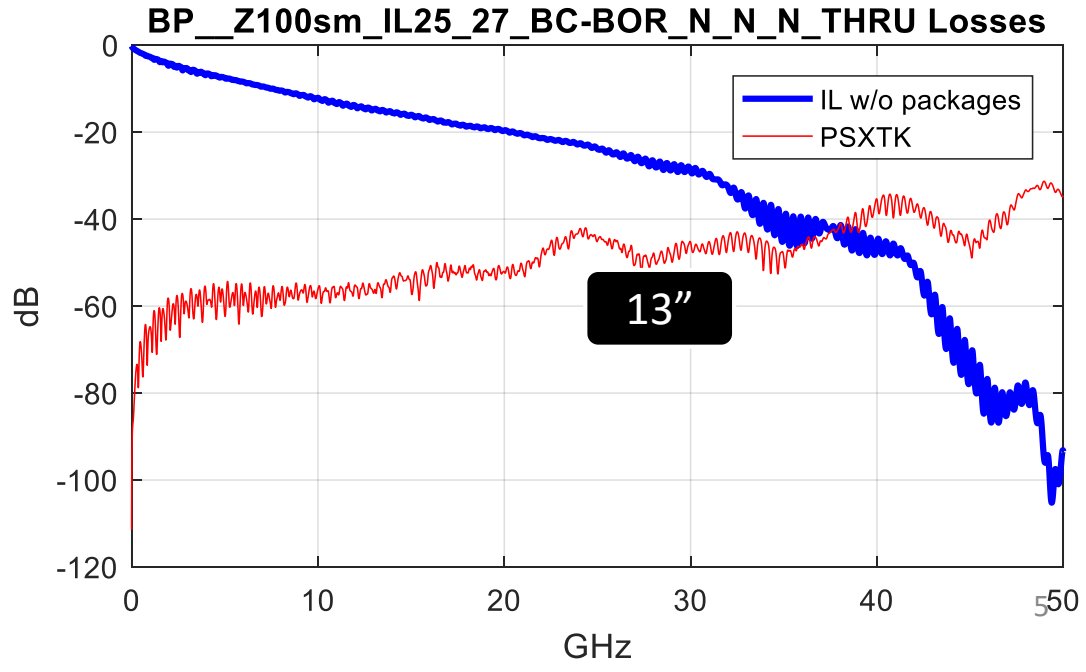
name	ASIC Break Out	Line card 1 Z0	backplane Z0	backplane routing length	Line card 1 Z0	Aprox. IL @ 26 GHz	Aprox. IL @ 28 GHz
BP__Z100sm_IL15to16_BC-BOR_N_N_N	best case top layers	100 ohms	100 ohms	3"	100 ohms	15 dB	16 dB
BP__Z100sm_IL25to26_BC-BOR_N_N_N	best case top layers	100 ohms	100 ohms	13"	100 ohms	25 dB	26 dB
BP__Z100sm_IL30to32_BC-BOR_N_N_N	best case top layers	100 ohms	100 ohms	18"	100 ohms	30 dB	32 dB

Worse case lower layer ASIC break outs can increase insertion loss up to 5 dB and add more ISI.

Thru Response and Power Sum Crosstalk

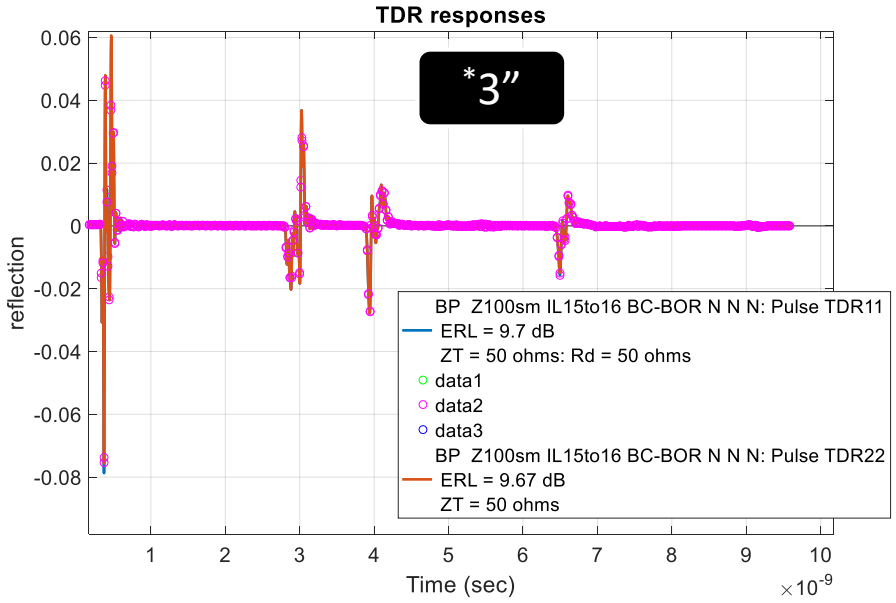




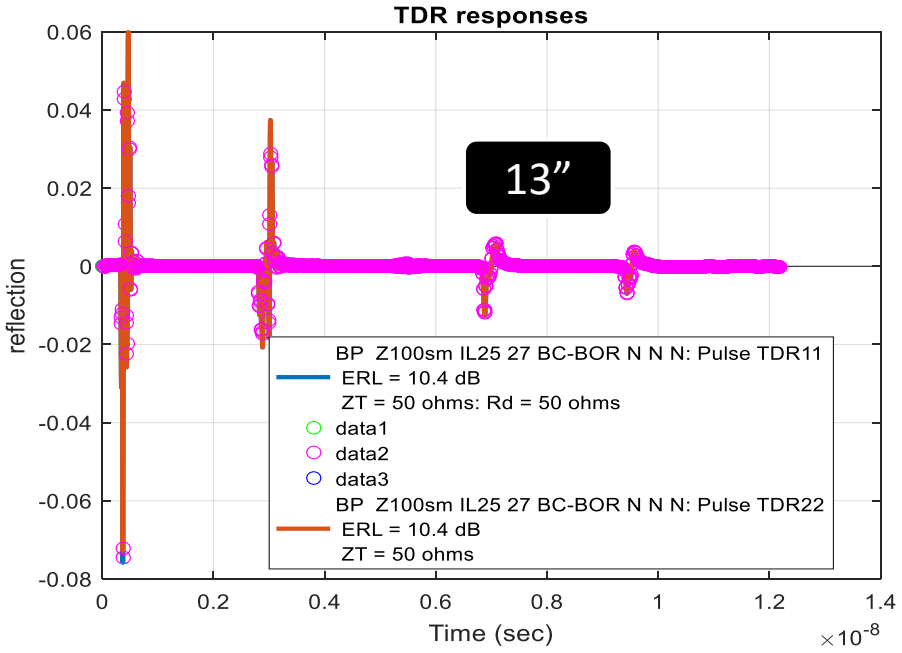


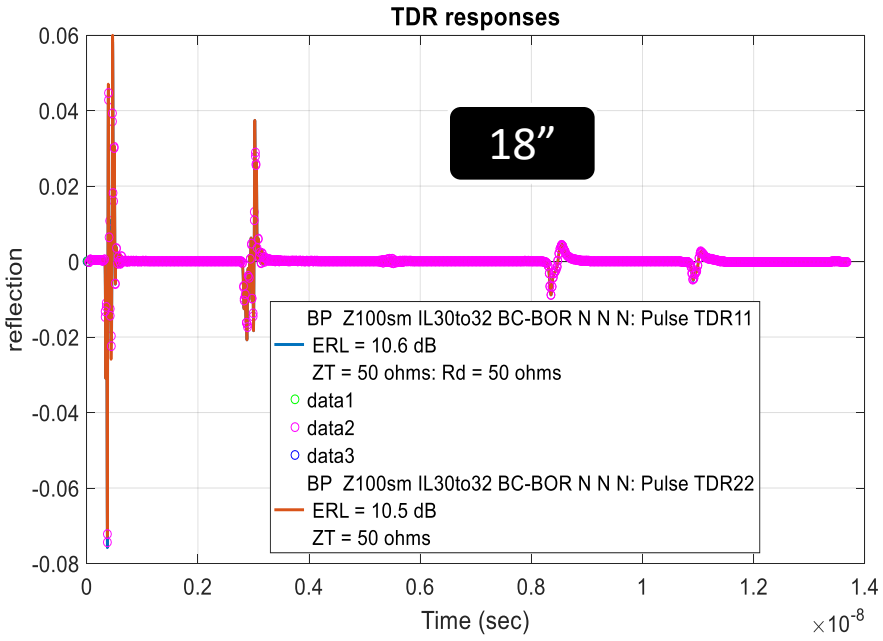
* Routed length on backplane

ERL (Effective Return Loss), 14 DFE taps with Fb = 28 GHz, T_r=10ps

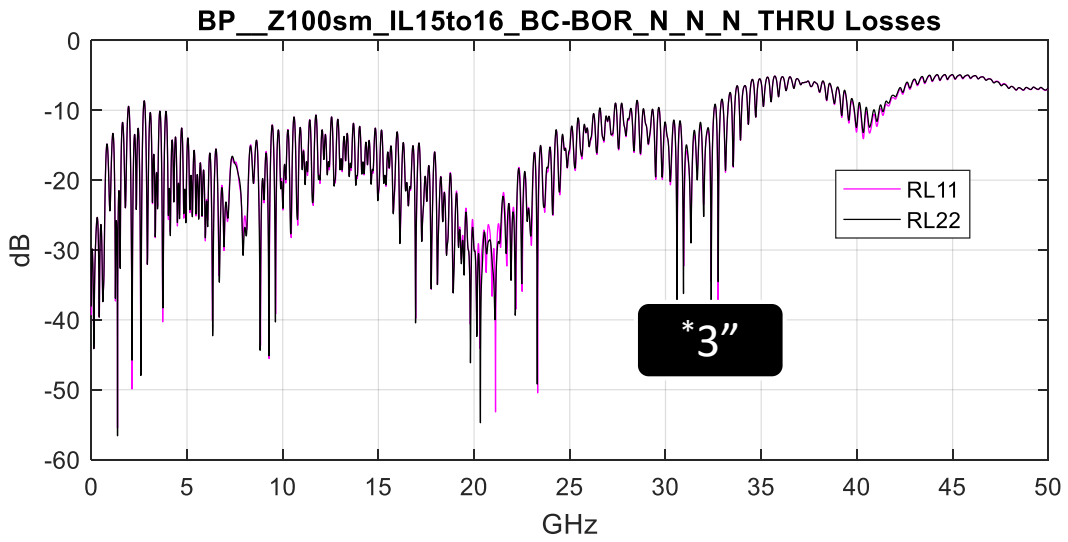


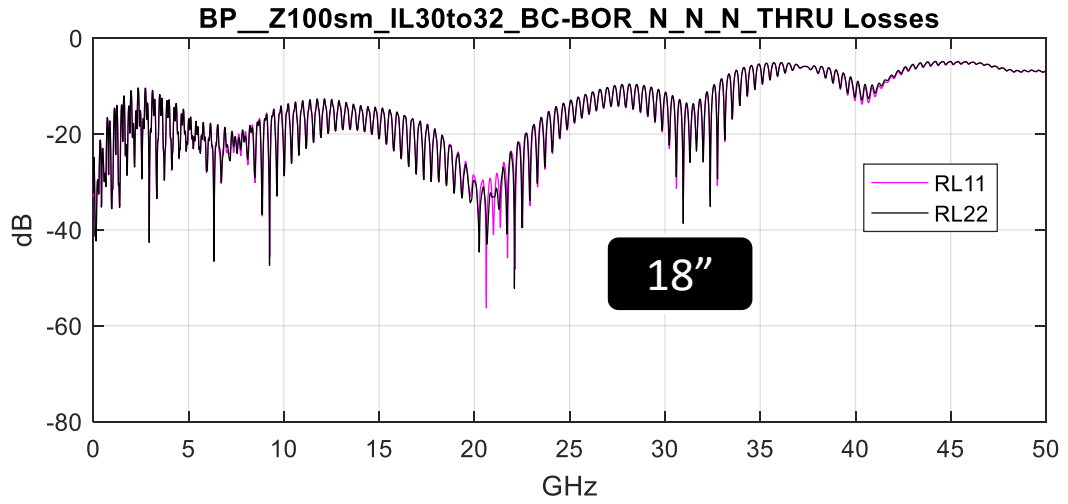
* Routed length on backplane

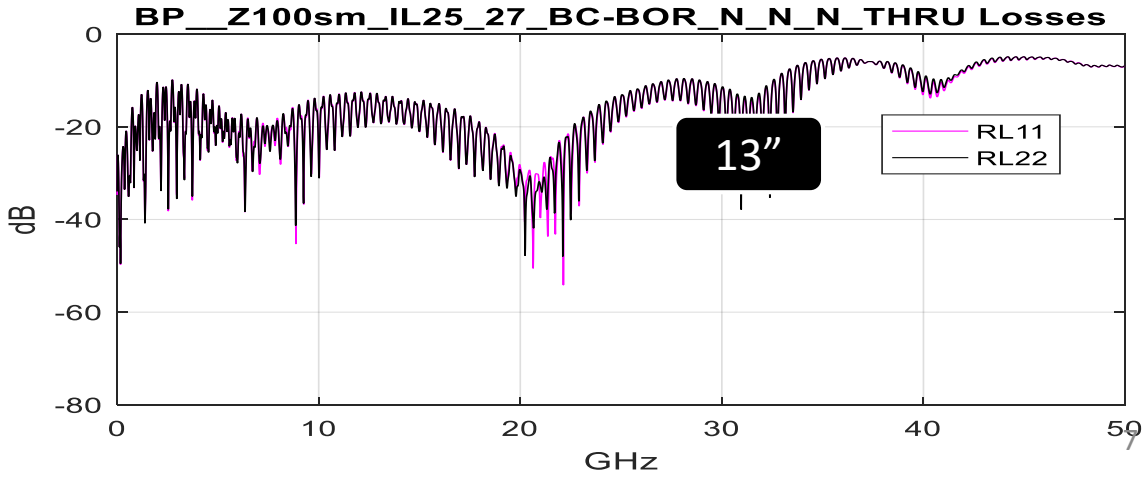




Return Loss







* Routed length on backplane

Files Sets

mellitz_100GEL_adhoc_02_010318.zip	mellitz_100GEL_adhoc_03_010318.zip	mellitz_100GEL_adhoc_04_010318.zip
BP__Z100sm_IL15to16_BC-BOR_N_N_N_THRU.s4p	BP__Z100sm_IL25to26_BC-BOR_N_N_N_THRU.s4p	BP__Z100sm_IL30to32_BC-BOR_N_N_N_THRU.s4p
BP__Z100sm_IL15to16_BC-BOR_N_N_N_NEXT_1.s4p	BP__Z100sm_IL25to26_BC-BOR_N_N_N_NEXT_1.s4p	BP__Z100sm_IL30to32_BC-BOR_N_N_N_NEXT_1.s4p
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