# Objectives for Next Generation 100GbE Optical Interfaces

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# Introduction

One of the key outputs of the *Next Generation 100GbE Optical Interfaces* Study Group is the set of objectives.

This contribution discusses what the possible objectives might be in order to understand what questions need to be answered by the Study Group before a suitable set of objectives can be agreed.

Note – * in the top right corner of the slide indicates slide has changed from previous version of this presentation

# Adopted objectives

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The following objectives have been adopted by the Study Group:

- Support full-duplex operation only
- Preserve the IEEE 802.3 / Ethernet frame format utilizing the IEEE 802.3 MAC
- Preserve minimum and maximum FrameSize of current IEEE 802.3 standard
- Support a BER better than or equal to $10^{-12}$ at the MAC/PLS service interface
- Provide appropriate support for OTN
- Define re-timed 4-lane 100G PMA to PMA electrical interfaces for chip to chip and chip to module applications

# 100G over Multimode fibre

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One of the expected elements of this project is a new 4-lane multimode PMD.

The corresponding objective could be:

- Define a 4-lane 100 Gb/s PHY for operation over OMX MMF with lengths up to at least Y m

Questions that need to be answered by the study group:

- Technical and economic feasibility of transmitters and receivers – confirm that this 4-lane interface is lower cost than 100GBASE-SR10 with reverse gearbox
- Can this interface be realized un-retimed, half re-timed, or is full re-timing needed for realistic host board trace length / material?
- Does the inclusion of EDC and/or FEC improve the broad market potential?
- Is it acceptable to rely on OM4 to meet the reach objective? So should the objective be for OM3 or OM4 or just MMF?
- Given answers to the above, what should the value of OMX and Y be?

# 100G over Single-mode fibre

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There is a strong desire to improve the size, power and cost of a 100G single mode interface. Some improvement in these metrics (at least for the module) can be realised by defining a 4-lane electrical interface (see slide 3).

Some options for an improved SM module may not be capable of supporting the 100GBASE-LR4 spec. In that case a possible objective could be:

- Define a 100 Gb/s PHY for operation over at least C km of SMF

Questions that need to be answered by the study group:

- Technical and economic feasibility of transmitters and receivers – what makes this interface significantly cheaper than 100GBASE-LR4 with no gearbox in the module?
- Can this interface be realized un-retimed, half re-timed, or is full re-timing needed for realistic host board trace length / material?
- What is the market need for reaches capable of being met by the identified technology?
- Given answers to the above, **should there be a 100G SM objective?** If so, what is the value of C?

Thanks!