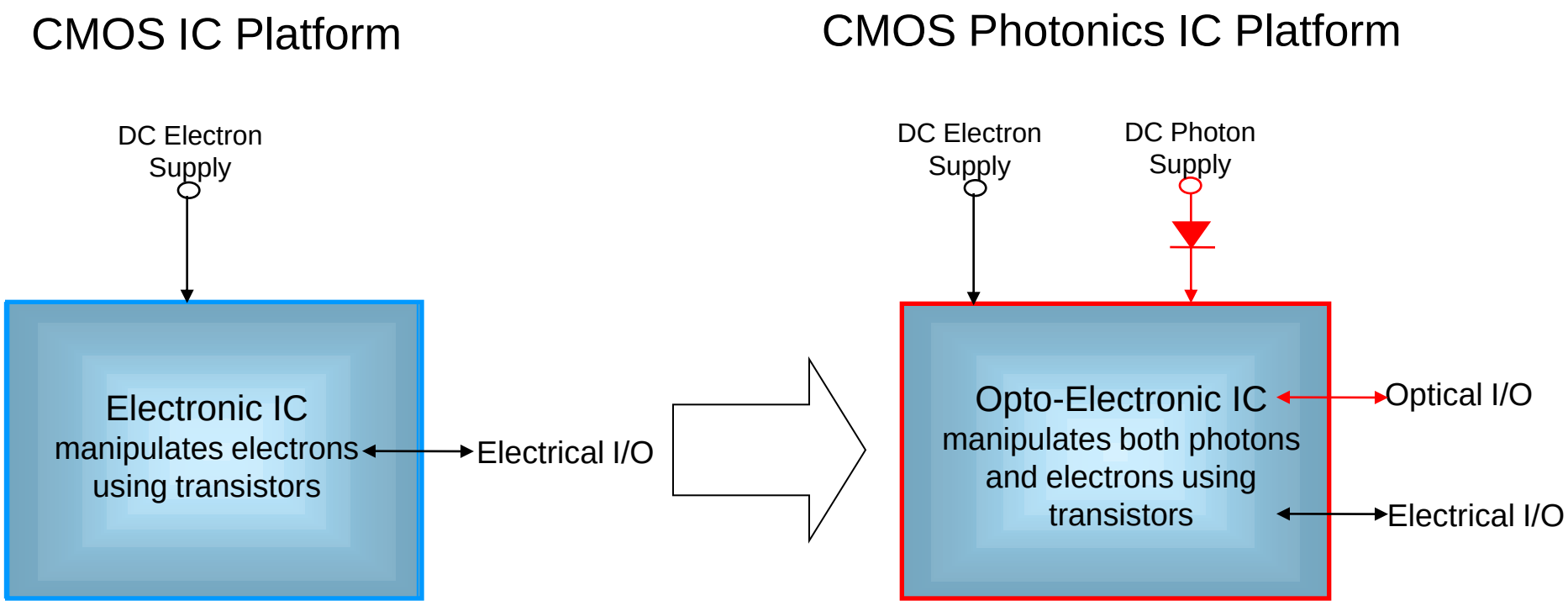
CMOS Photonics 101

Contributors:
Tom Palkert (Luxtera)
Dave Piede (Lightwire)

What is CMOS Photonics?



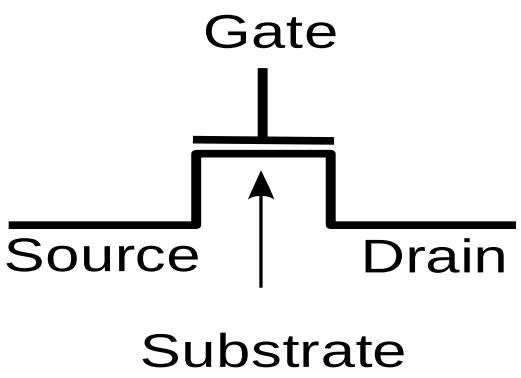
CMOS Photonics IC Platform leverages existing multi-billion dollars of investment, Infra-structure and discipline of the CMOS IC industry to manipulate both Electrons & Photons to achieve desired Opto-Electronics functions using External DC Sources

LUXTERA

LIGHTWIRE

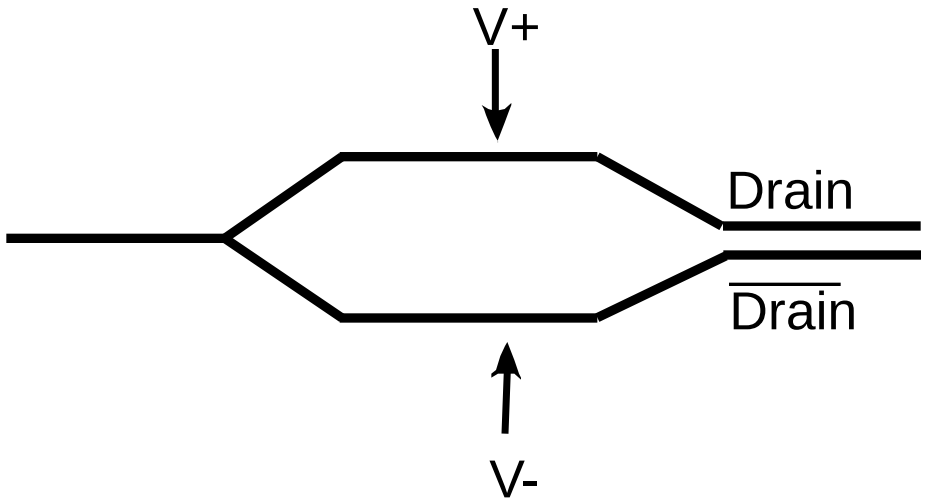
Fundamental Technology

MOS Transistor



By controlling the voltages on terminals, MOS Transistor controls the flow of electrons from source to drain. Today, 100s of millions can be placed on a single electronics chip.

CMOS Photonics Modulator



By controlling the voltages of the two arms of the modulator, one controls the flow of photons from source to drain with one major difference – Photons cannot be stopped and hence the unwanted will go to Drain. A large numbers of these can be integrated on a single chip.

Just like the transistor is the basic building block for all ICs, Broadband Modulator is the basic building block for all high speed optical interconnects

LUXTERA

LIGHTWIRE

Optical Components and Libraries in CMOS

Silicon waveguides:

- SOI and etched trenches for respectively vertical and horiz ement
- Small mode size - > small bending radii -> compact photoni
- Demonstrated losses < 0.1 dB/cm

Library of passive waveguide structures

- Termination
- Splitters
- Directional couplers

Library of fiber-to-the-chip couplers

- Single and polarization splitting grating couplers
- Low loss-coupling waveguide to single mode fiber
- Enable wafer scale optical testability

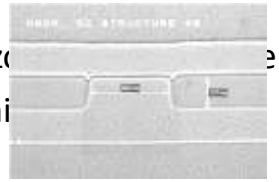
Library of waveguide photo-detectors

- Selective epitaxy of germanium on silicon
- Enable low cost, high-sensitivity integrated receivers

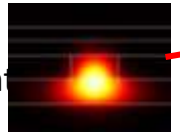
Library of phase modulators

- Building block for intensity modulators (MZI, ring,…)
- Very high modulation bandwidth: ~ 160 GHz

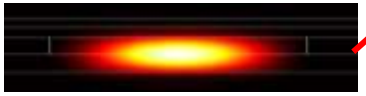
Cross-section single mode waveguide

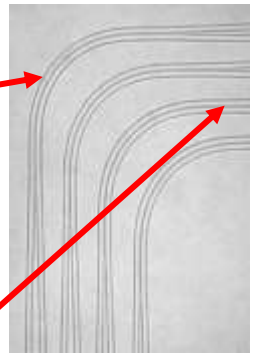


Single Mode

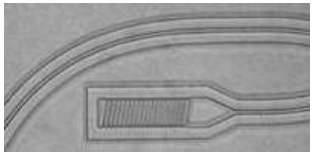


Multi Mode

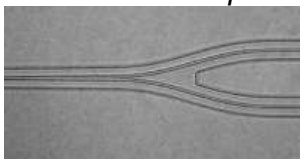




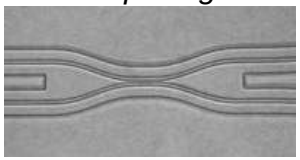
Waveguide Termination



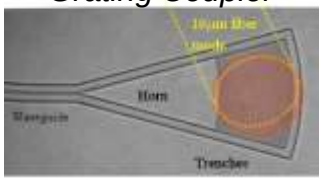
Y-junction Low loss 50% splitter



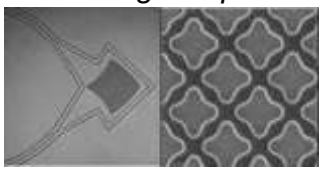
Directional Coupler: tunable splitting ratio



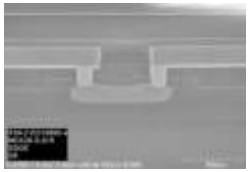
Single Polarization Grating Coupler



Polarization Splitting Grating Coupler



Germanium Detector

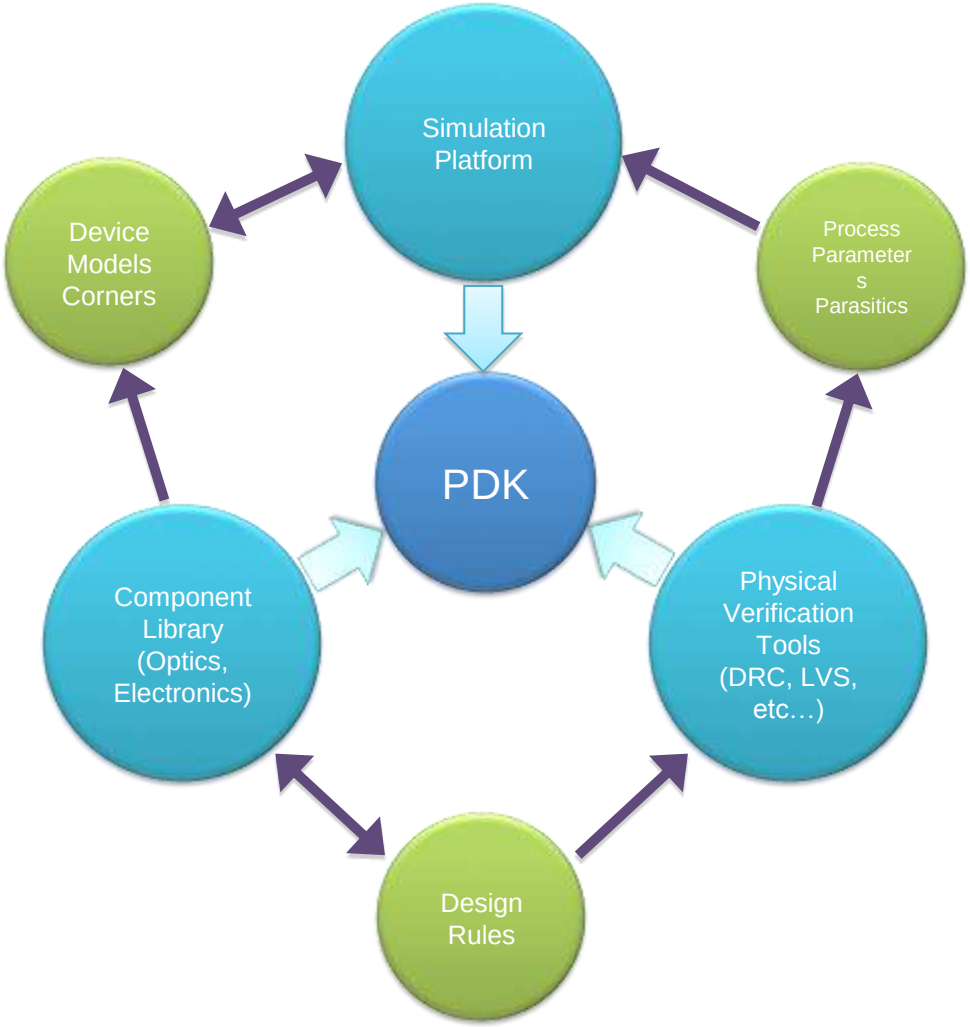


Integrated Receiver

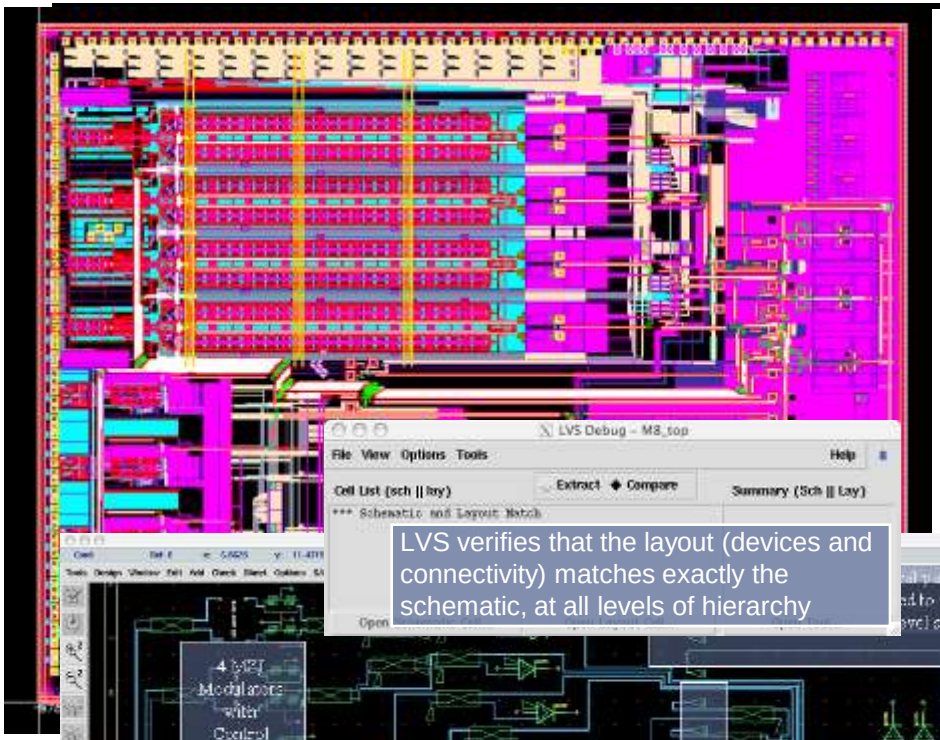
Design Tools: Process Design Kit (PDK)

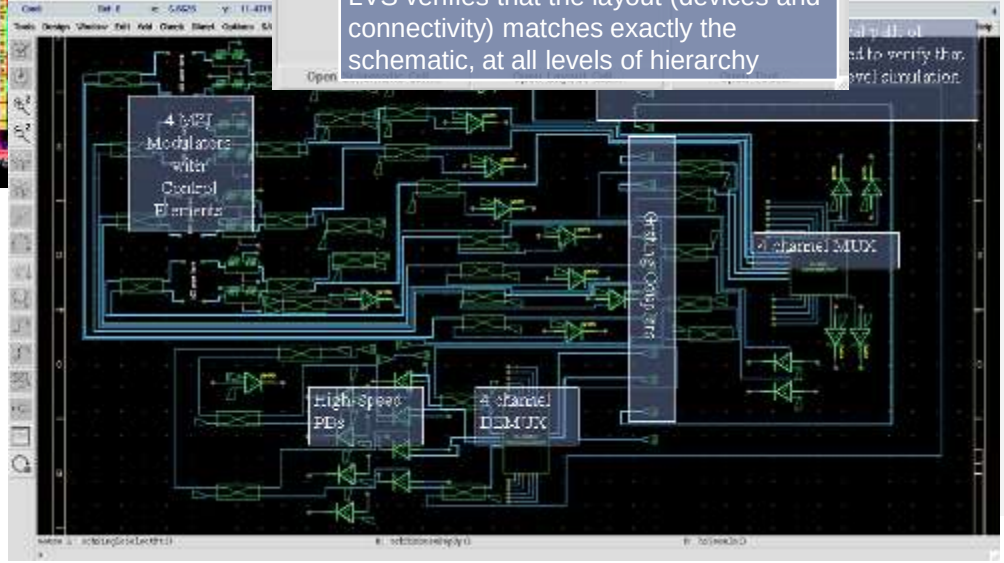
ENABLE ELECTRONICS TYPE OF DESIGN PROCESSES FOR OPTICS

- Basic set of optical design rules
  - Process checks
  - Device checks
  - Interaction of optics and electronics
  - Run separately from electrical DRC
- LVS
  - Additional optical LVS for optical connectivity
  - Additional OE LVS for devices connecting to electrical circuits
- Simulation
  - OE simulation of complete subsystems
  - Using electrical models to represent subset of optical devices

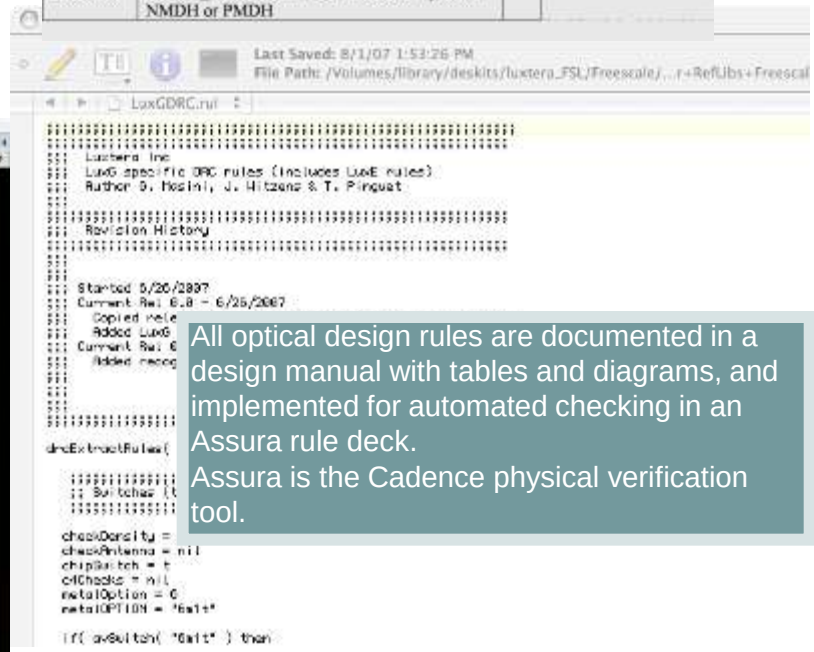


Photonic/Electronic LVS, DRC and Simulation



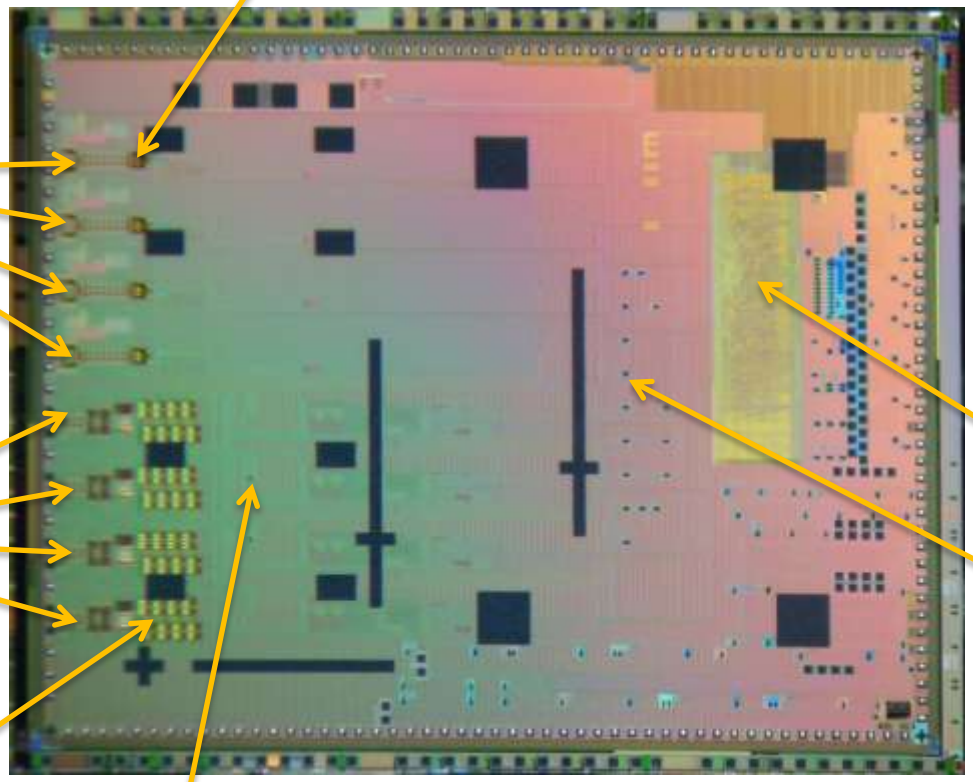


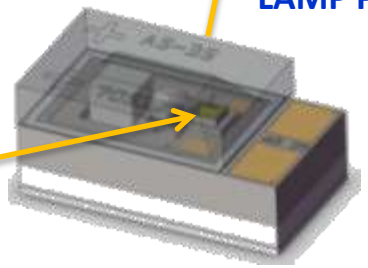
Rule	Description		Design (µm)	Scaled (µm)
LUX0000	OTRENCH width	≥		
LUX0001	OTRENCH area (um^2)	≥		
LUX0001b	OTRENCH enclosed area (um^2)	≥		
LUX0002	OTRENCH space to OTRENCH	≥		
LUX0003	OTRENCH must always be enclosed by dfOPTICAL			
LUX0004	Transistor implants must not overlap OTRENCH			
LUX0005a	dfOPTICAL enclosure of OTRENCH	≥		
LUX0005b	dfOPTICAL enclosure of OTRENCH	≤		
LUX0005c	OTRENCH space to OTRENCH within dfOPTICAL	≤		
LUX0006	NPLUSBlk spacing to contact_OTRENCH/NMDH	≥		
LUX0007a	NPLUSBlk enclosure of waveguide_OTRENCH	≥		
LUX0007b	PWELLBlk enclosure of OTRENCH	≥		
LUX0007c	HALOBLK enclosure of OTRENCH	≥		
LUX0008	Contact_OTRENCH must be enclosed by either NMDH or PMDH			



All optical design rules are documented in a design manual with tables and diagrams, and implemented for automated checking in an Assura rule deck.
Assura is the Cadence physical verification tool.

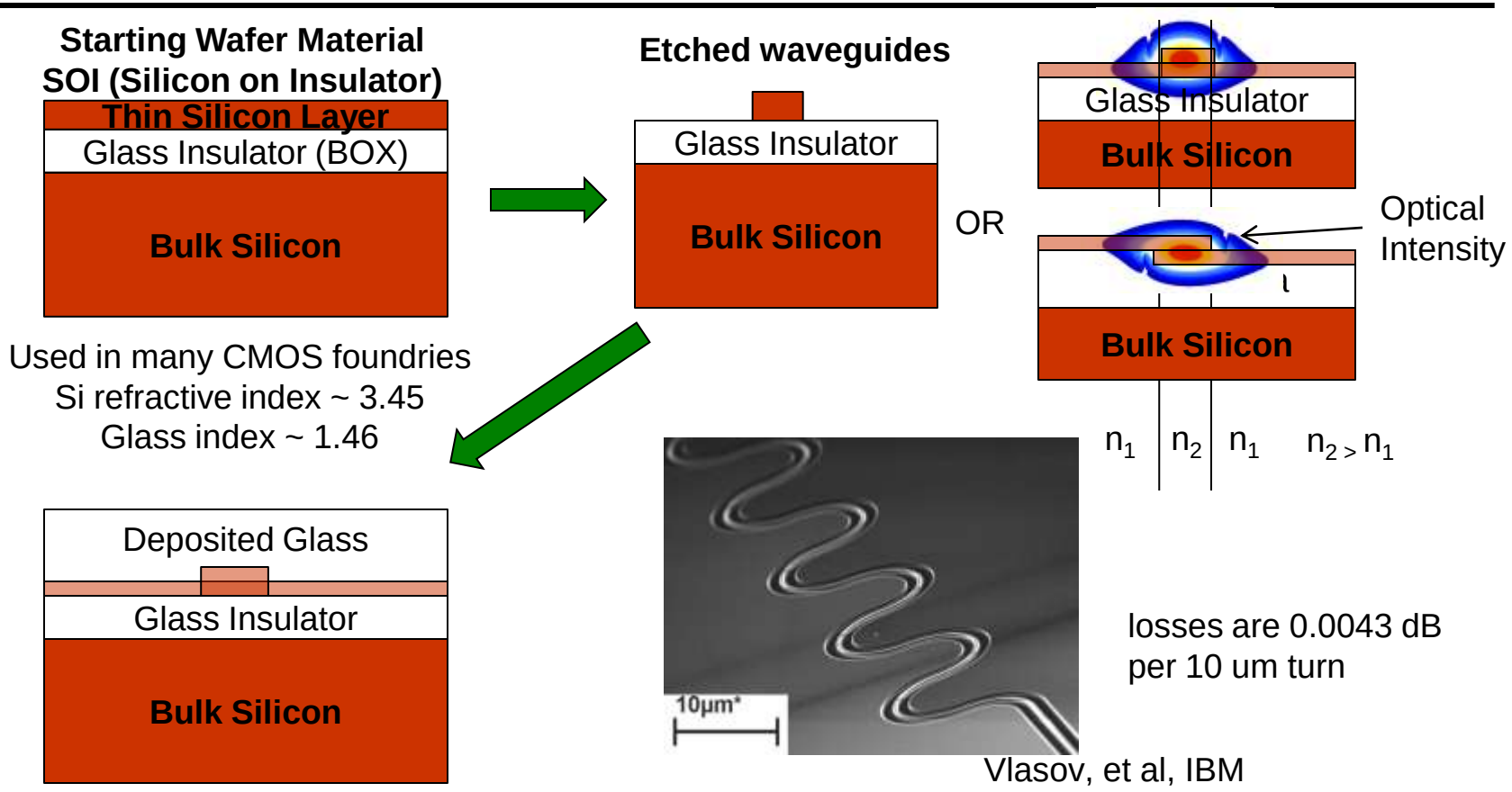
Single Chip 4x28Gbps Optical Transceiver





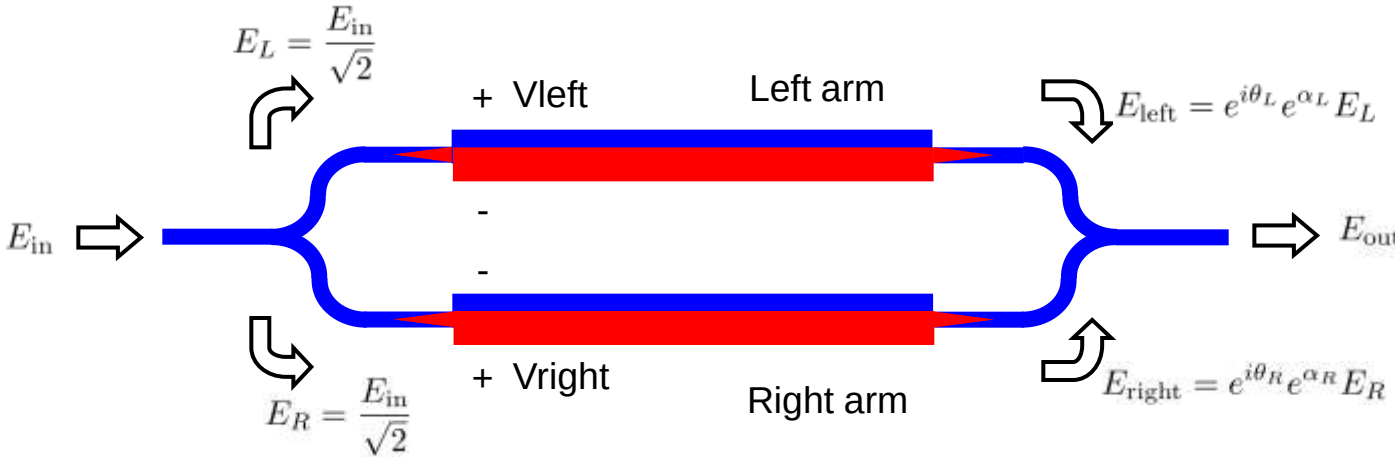
- Die size (5 mm x 6 mm)
- Die size is driven by laser and fiber attachment
- White space available for additional logic

Waveguides & Refractive Index in CMOS

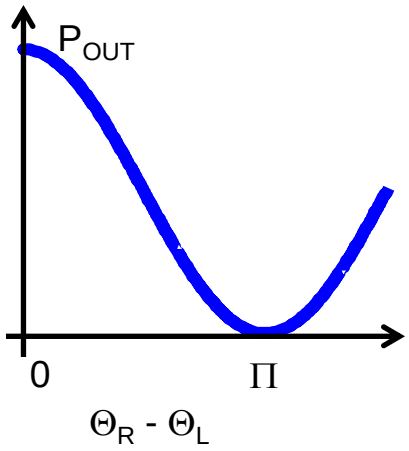


- Optically smooth surfaces are now possible in mature CMOS processes
- CMOS photonics uses standard CMOS equipment and processes
- Silicon is transparent at $\lambda > 1.1$ um
- High index contrast waveguide enables micron size devices

Mach Zehnder Interferometer (MZI) Modulator overview



$$P_{out} = |E_{out}|^2 = |E_{in}|^2 \frac{[1 + \cos(\theta_R - \theta_L)]}{2}$$



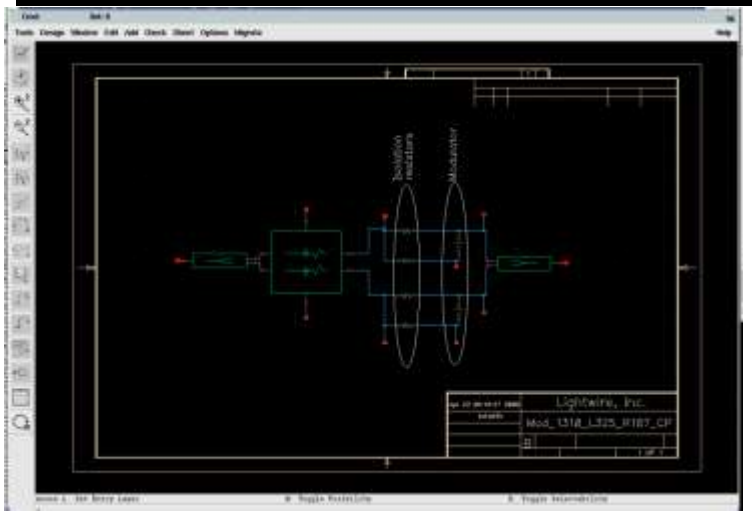
- When $\Theta_R - \Theta_L = 0$ Optical '1'
- When $\Theta_R - \Theta_L = \Pi$ Optical '0'
- Applying a + / - voltage on Vright decreases / increases Θ_R respectively.
- Applying a + / - voltage on Vleft decreases / increases Θ_L respectively.
- For silicon modulators, the applied + / - voltage injects / removes electrons and holes in the optical path which changes the optical index => Free Carrier Plasma Dispersion Effect

MZI deployed in optical systems for over 20 years

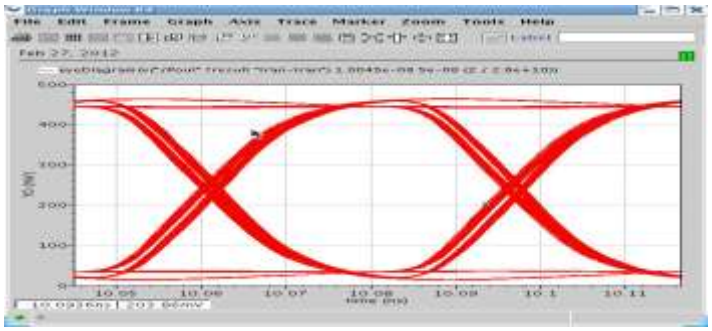
LUXTERA

LIGHTWIRE

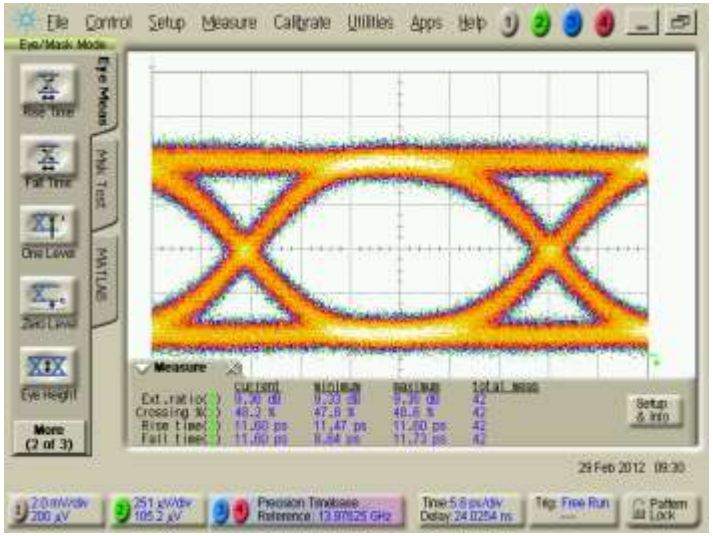
Tx Optical Eyes at 28Gbps – Simulation and Measurement:



Cadence MZI Simulation Model



Simulation

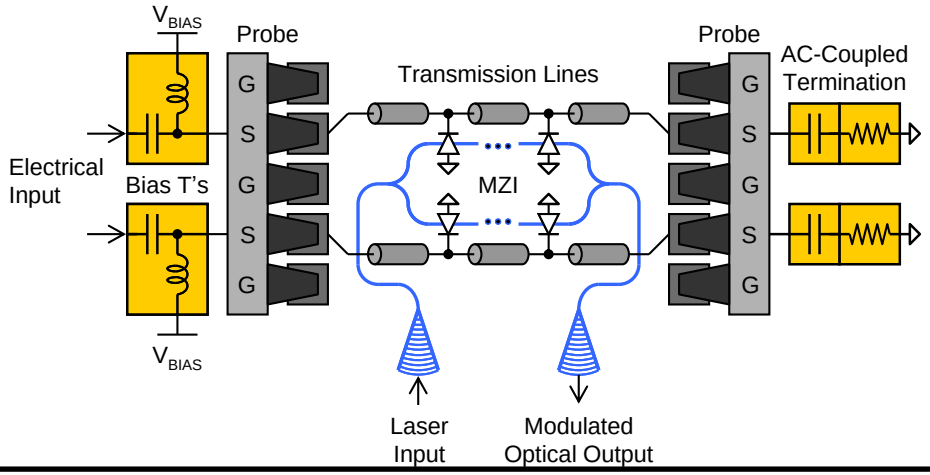


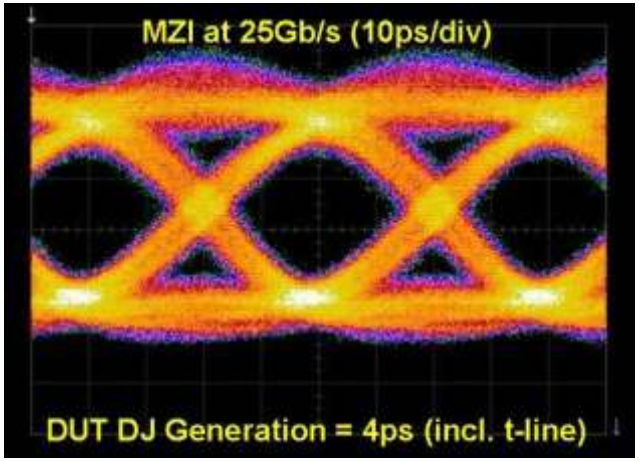
- 28G optical eye
- PRBS-31
- ER = 9.3 dB
- Trise/Tfall ~ 12ps (20%-80%)

Excellent correlation between simulation and measurement

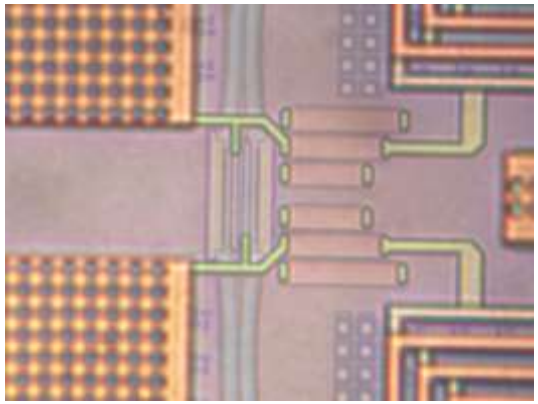
Demonstrated 25G Performance

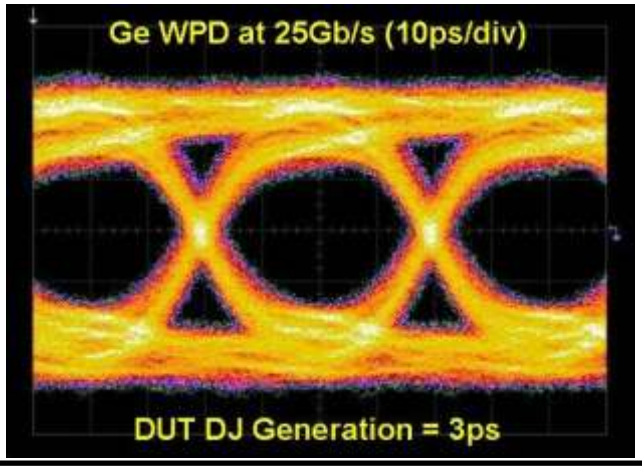
25G Modulator Demonstrated in Silicon





25G Photodetector Demonstrated in Silicon

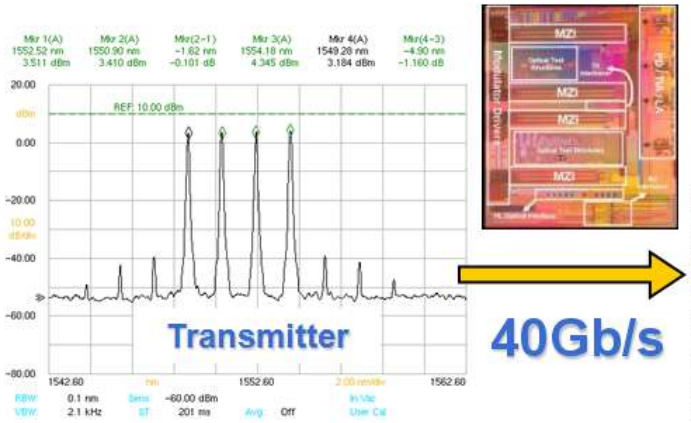




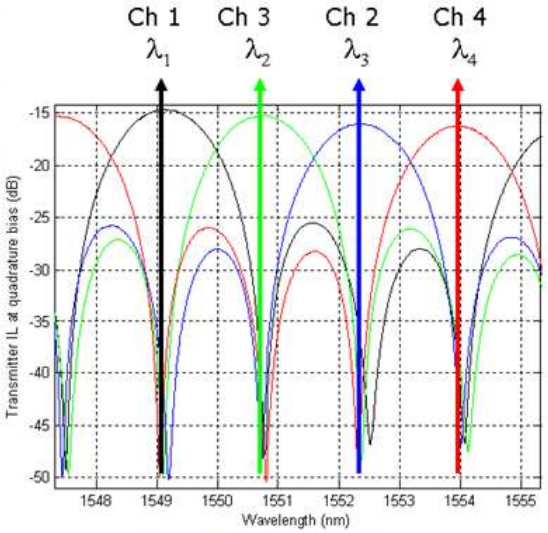
Technology Roadmap - Fiber Capacity

CMOS Photonics enables several ways to increase channel capacity beyond raw data rate:

- Wavelength diversity (WDM): Enabled by on-chip MUX/DEMUX.
- Multi-level signaling (i.e. PAM-4): Simplified by external laser modulation

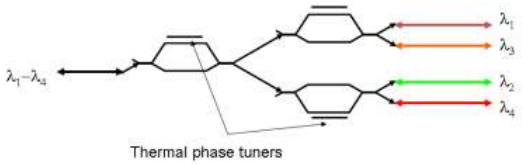


40Gb/s



Receiver Interleaver

- Channel spacing = 1.6 nm = 200 GHz
- Typical optical insertion loss < 2.5 dB
- Thermal phase tuners are used to shift the spectral response providing:
  - Temperature compensation
  - Process compensation
  - Agile wavelength plan



CMOS Photonics Integration - Advantages

- Low power
  - 780mw for 4x10G QSFP today (20mW/Gbit)
- Enables high density solutions
  - CMOS Photonics Physical Density > 130 Gbps/mm^2
  - CMOS Photonics I/O Density > 400 Tbps/mm^2
  - Show CFP going to SFP

CMOS Photonics
Summary of Capabilities

- Performance
  - Reliable (1M ports shipped to date)
  - Extremely small devices due to high contrast index waveguides
  - Multitude of optical building blocks – modulators, detectors, muxes, switches, etc
  - High Speed Modulation at extremely low power
  - CW laser source => low cost
- CMOS Compatibility
  - CMOS fabrication process => low cost
  - CMOS IC Simulation tools
  - CMOS IC layout tools
  - Monolithic integration of multiple opto-electronic building blocks in simulation tools => Large scale integration

CMOS Photonics enables a new class of low power, low cost, high density solutions

LUXTERA

LIGHTWIRE