PAM8 Gearbox issues

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Supporters

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Recap of szczepanek_01_0112

- Estimate for PAM-8/16 CDR power
  - Receiver CDR chip power is estimated based on CMOS process at TT, 85C, 1V supply condition.
  - Receiver CDR includes one PAM-8/16 input lane and four NRZ output lanes.
  - No FEC functions are included in the power estimates.

100 Gbps RX CDR Power Estimates					
Input Signaling	Input Data Rate (GSymbols/s)	Input Bits/Symbol	Number of RX Lanes	Number of TX Lanes @28G	Total Power (Normalized to NRZ power)
NRZ	25	1	4	4	100%
PAM-8	34	3	1	4	~80%
PAM-16	25	4	1	4	~85%

- Linear receivers at 32 GBaud/s for coherent QPSK systems are commercially shipping today
- Power consumption for PAM-N CDRs appear to be in line with NRZ CDRs
- Overall, feasibility for linear TIAs and PAM-N CDRs appears promising, and merits further investigation

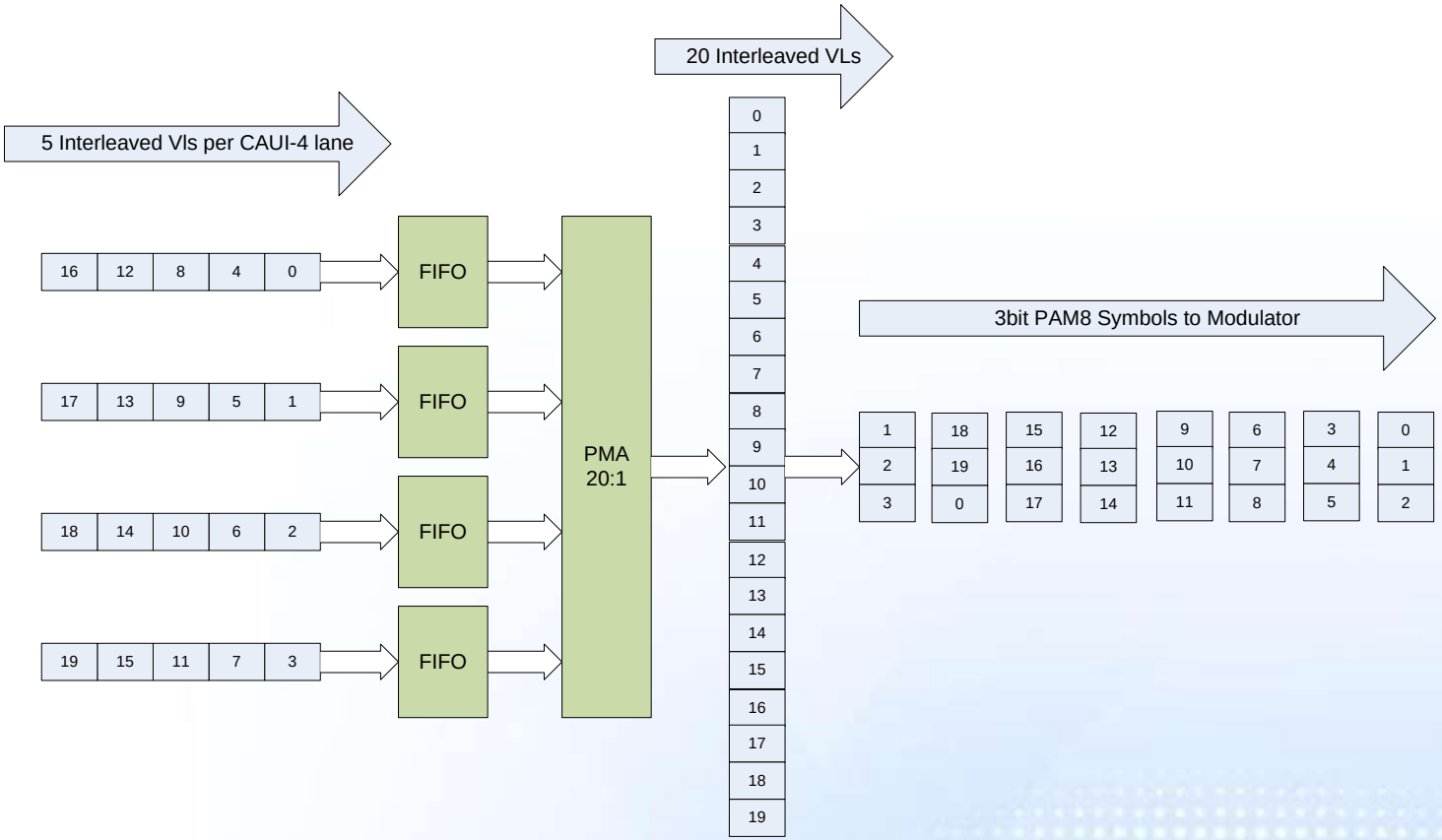
Overview

- At the January Interim meeting a couple of issues were raised about the gearbox function for the PAM8 :
  - How does 4:3 gearbox meet PMA/VL rules ?
  - Implementation complexity of 4:3 gearbox vs 4:4 retimers
- This presentation addresses these two issues for PAM8
  - The same principles are also true for PAM16

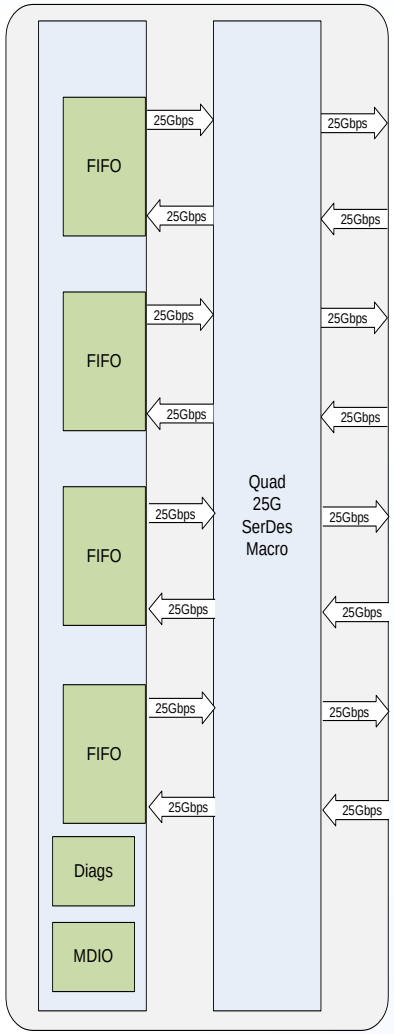
PAM8 4:3 gearbox function

- The PAM8 4:3 gearbox function is NOT a 4:3 PMA
  - PAM8 does not send 3 asynchronous bit streams, it sends a single 100Gbps bit stream using 8 levels.
- The PAM8 gearbox is a 20:1 PMA
  - The PMA follows the Clause 83 PMA rules to bit interleave the 20 VLs provided by the CAUI-4 interface
  - This serial bit stream is then sent as 3-bit PAM8 symbols to the Laser modulator

VL distribution and the 4:3 Gearbox

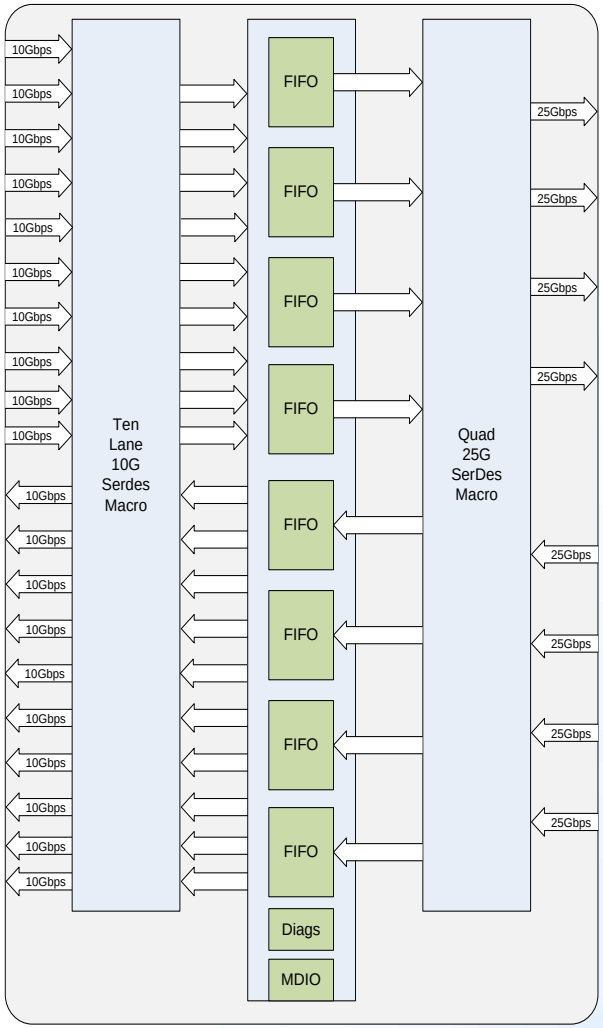


Implementation complexity of CMOS VSR re-timer



- CMOS retimers, can be based on a 28G Serdes macro + synthesized (skew) FIFOs
  - Power is dominated by Serdes macro, not FIFO function
  - Non-Serdes power is <5% of device power for Inphi retimer

Implementation complexity of CMOS VSR gearbox



- A CMOS 10:4 gearbox is also based on Serdes macros + synthesized (skew) FIFOs & VL muxing
  - Power is still dominated by Serdes macro, not FIFO functions
  - Non-Serdes power is <6% of device power for Inphi gearbox
  - Only 1% more power than the FIFO in a CMOS re-timer

Implementation complexity of PAM8 gearbox

- The Power consumption of CMOS re-timers and Gearboxes for CEI-28G-VSR is dominated by the power of the Serdes Macros
  - The difference in power between these devices is determined by the different Serdes not the gearbox function.
- The 4:3 gearbox function needed by PAM8 is no more complex than the 10:4 gearbox function already used for VSR
- So I estimate this function to again be <6% of Serdes power for the PAM8 device
  - 1-2% difference in overall power versus a 4:4 re-timer

Implementation complexity of FEC

- Gustlin_01_0112 provides power/complexity estimates for the various FEC options being considered for backplane NRZ
  - 0% overhead codes providing ~4.8dB of coding gain consume ~100mW
  - 3% overhead codes providing ~6dB of coding gain consume ~180mW
- The code needed for PAM8 has not been decided yet, but this gives us a range of 100-200mW for FEC implementation
  - Current re-timers in CMOS/InP consume ~2W for a re-timer pair
  - So FEC adds 5-9% power vs a 4:4 gearbox without FEC

Conclusions

- 4:3 Gearboxing adds negligible (1%) power/complexity vs a 4:4 retimer
- Inphi's analysis shows PAM8 CDR has roughly equivalent power complexity as a 4:4 retimer
- FEC implementation adds 5-9% power/complexity vs a 4:4 retimer

- The 4:3 Gearbox and CDR function required for PAM8 will consume ~6-10% more power than the equivalent 4:4 re-timer
  - In current technology this is ~120-200mW