Considerations for WDM NRZ links : CMOS-Integrated Silicon Photonics case

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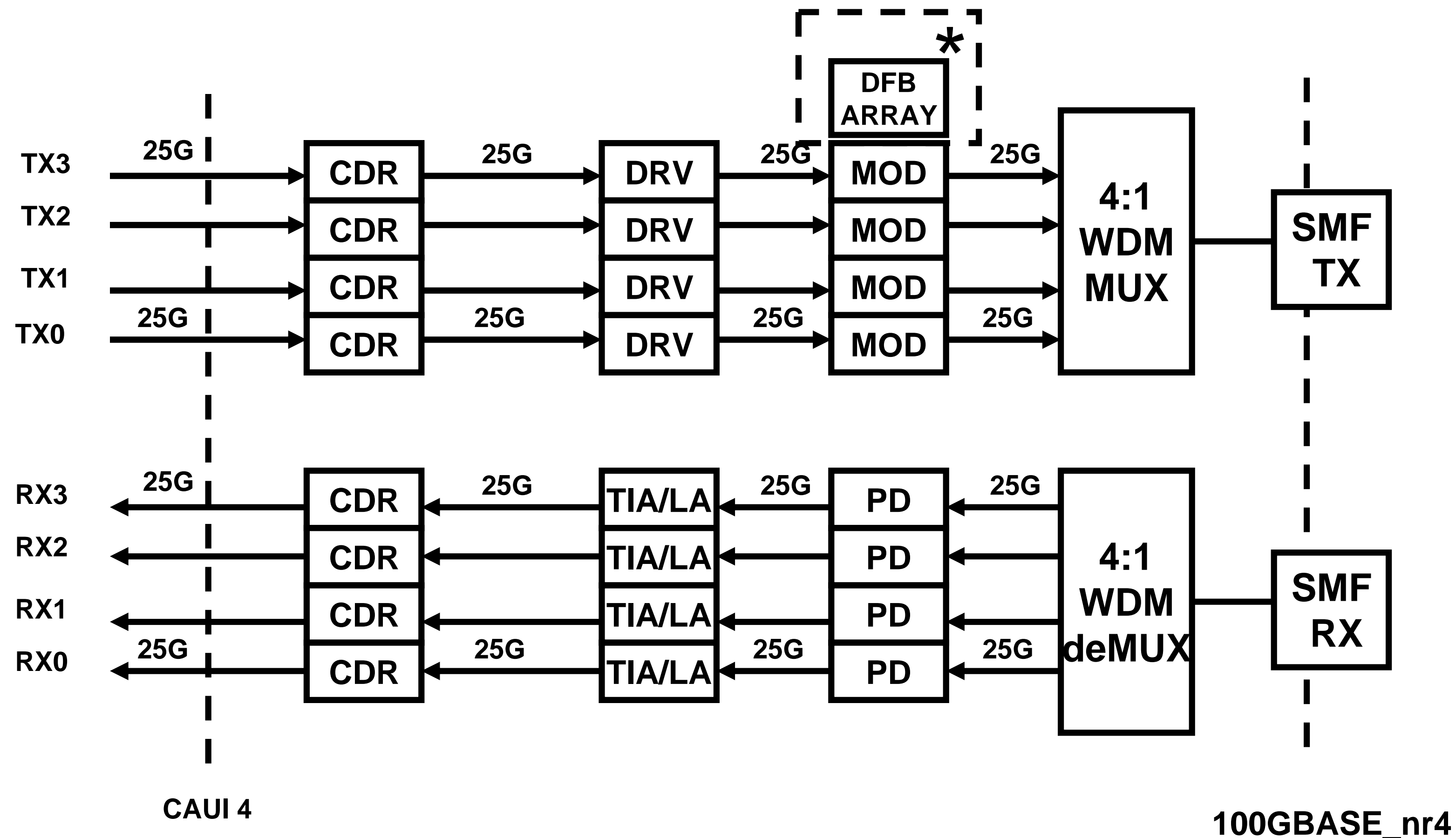
Introduction

- Step function cost reduction is needed
  nowell_01_1111_NG100GOPTX.pdf
- Cost of SM solution is mostly defined by module cost
  kipp_01_0112_NG100GOPTX.pdf
- PAM modulation is under consideration
  bhoja_01_0112_NG100GOPTX.pdf
  szczepanek_01_0112_NG100GOPTX.pdf
  - Laser is a largest part of module cost
  - PAM modulation is using a single laser
- CMOS-integrated WDM NRZ is considered here
  - LAN WDM, Uncooled, Retimed
  - Link budget 3-4dB
  - Link length 2km

Single-die WDM NRZ block diagram



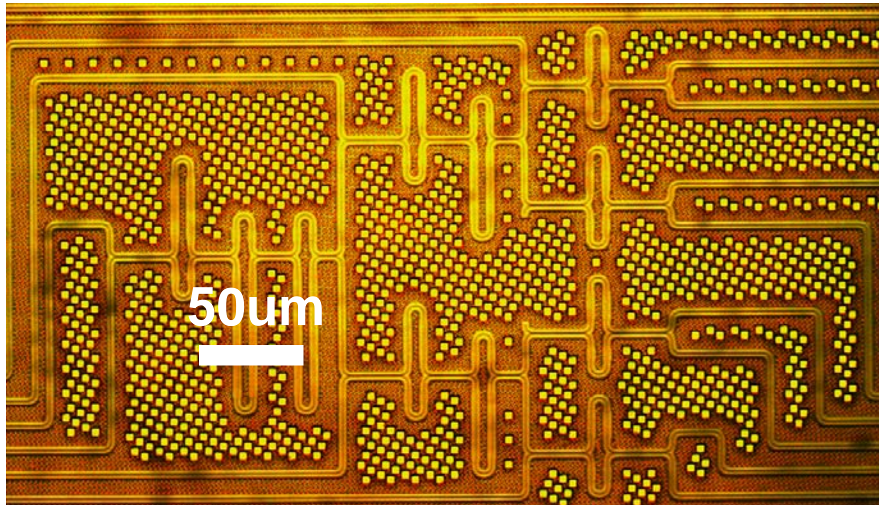
* DFB Array is a single die containing 4 DC DFB lasers

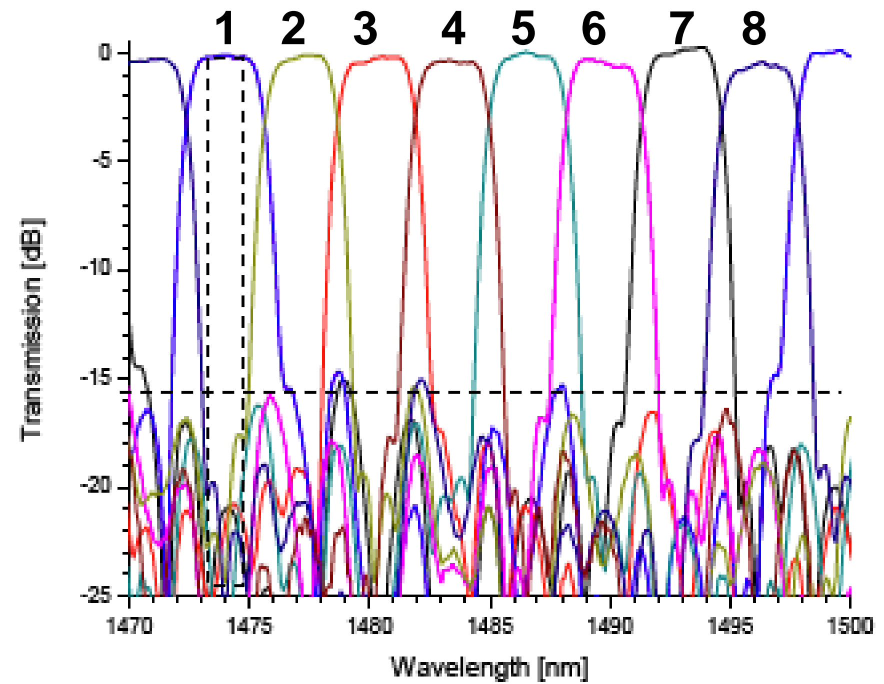
* Other implementations possible

Technical feasibility

- Example: 8 channel WDM at 1490nm

3-stage cascaded MZI lattice





▪No add-on charges: same mask and same processing as CMOS FETs
▪High yield and uniformity → passive filtering – no active tuning required

- 4 channel LAN WDM at 1310nm is an easier task

Scaling of CMOS-integrated Photonics

- Scaling of Photonics

  First technology node that can yield product-stable passive WDM is **the best**

  - 193nm lithography can control the LER (line edge roughness) variation within 9 nm (3σ)
  - Diffraction-limited scaled LAN WDM can be yielded by process control
  - No need to individually tune phase delays to compensate for fabrication-induced phase errors

  - Further scaling to advanced CMOS nodes would allow to control LER much better, however will nto decrease the size of the WDM

Scaling of CMOS-integrated Photonics

- Scaling of CMOS AMS circuits

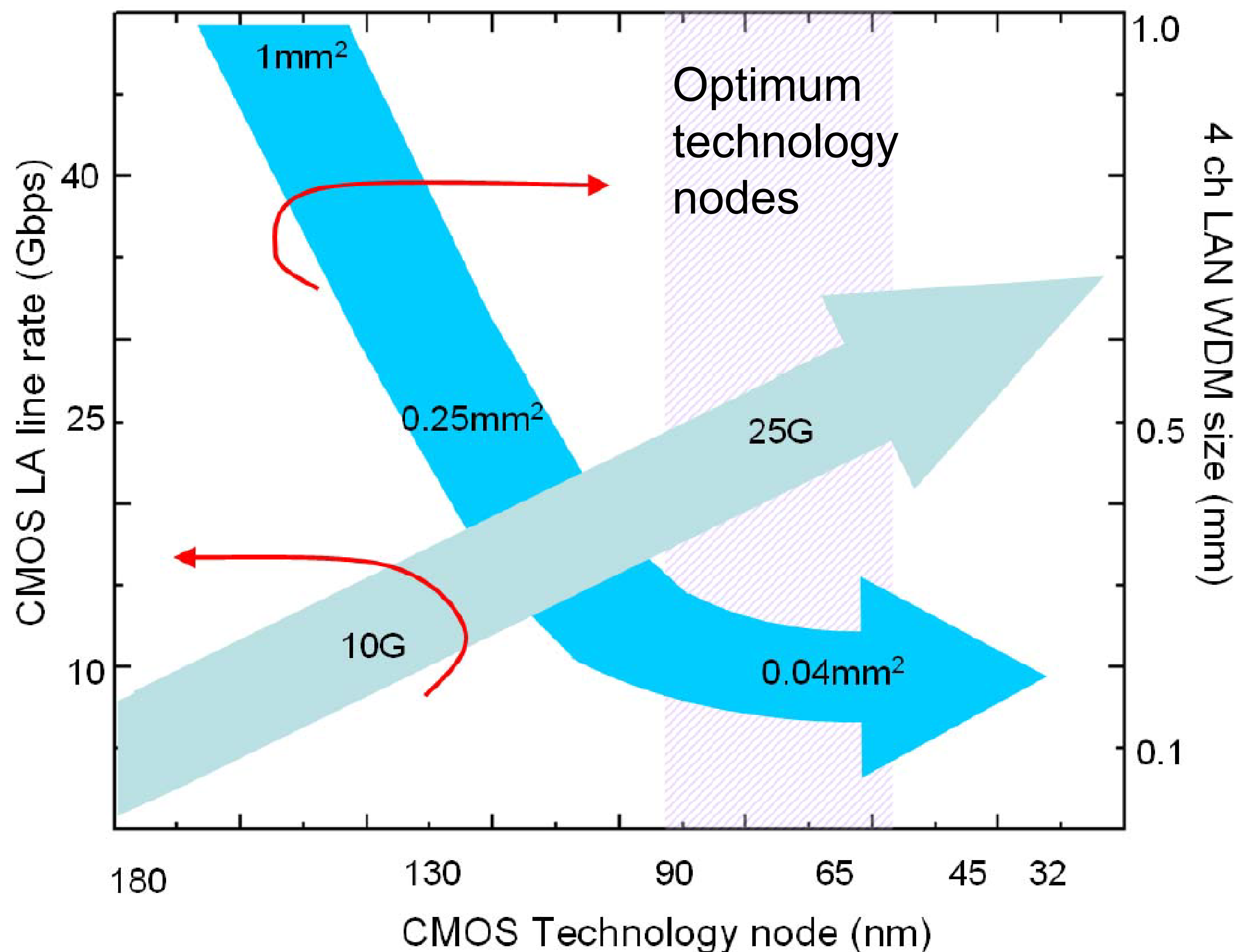
  First technology node that can yield product-stable 25/28Gbps AMS circuits including drivers, amps, CDR, etc. is **the best**

  – Advanced CMOS nodes will have higher bandwidth

  – However scaling of AMS circuits is not following the same trend as digital scaling: much less power and area savings

  – Significantly increased NRE, mask/step charges for advanced nodes

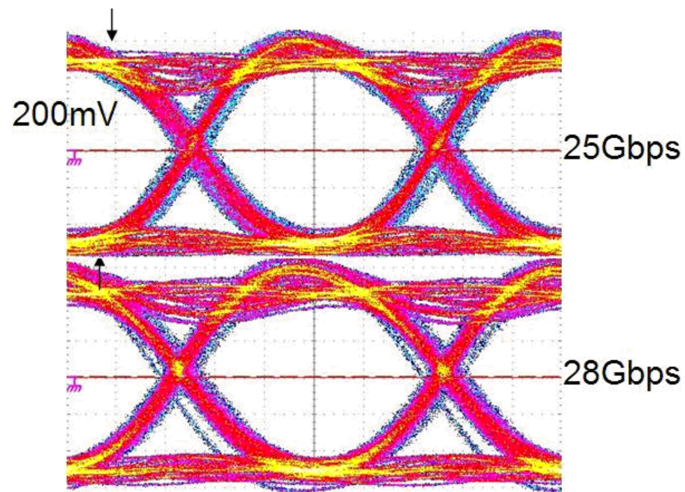
Choice of CMOS technology node



IEEE Comm. Mag. , February 2012, Y.Vlasov "Si nanophotonics for Computercom beyond 100G"

Feasibility demonstrations

- RX

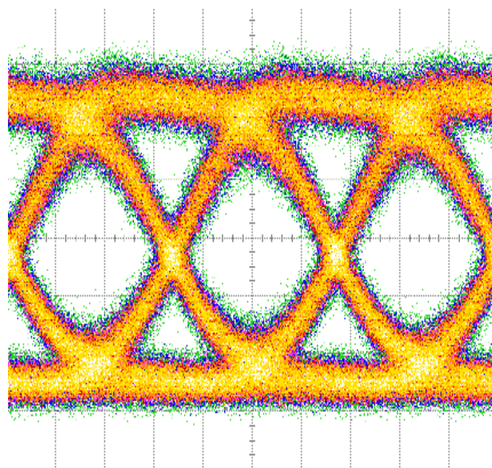


Measured 3.5pJ/bit @28Gbps

4ch@25Gbps = 350mW

Error-free (10^{-12} BER) up to 40Gbps

- TX



Ring modulator measured 100fJ/bit@25Gbps

Modulator driver measured 2pJ/bit@25Gbps

4ch@25Gbps = 200mW

Considerations for cost analysis

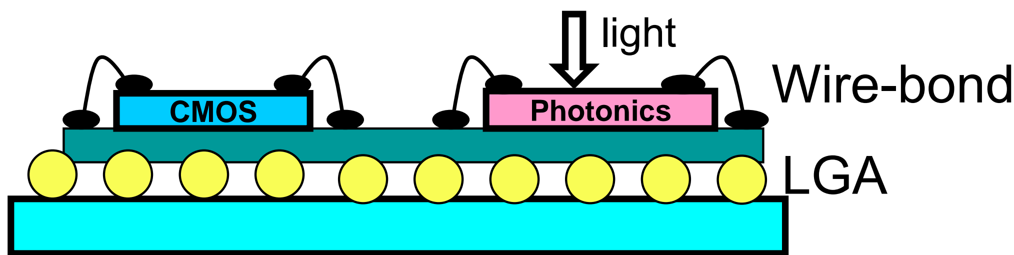
- Optical module cost analysis must include:
  - BOM (number / cost of components)
  - Assembly/packaging cost
  - Testing
- BOM for WDM CMOS transceiver
  - WDM CMOS Transceiver die * 1 (area 5x5mm^2)
  - InP laser array die 1 (area 1x0.5mm^2)
  - Fiber connector interface 1
  - Laminate 1

* Trivia: Integration of multiple optical and electrical components into a single CMOS die significantly decrease cost

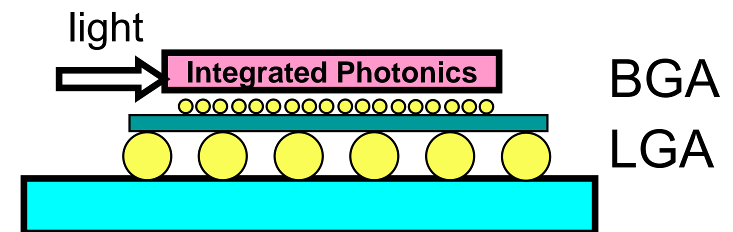
Packaging and Testing

- Implementation of WDM transceiver in CMOS allows to utilize **packaging** practices of microelectronics industry

Traditional optoelectronics approach



Traditional microelectronics approach



BOM ⇩
Packaging ⇧
Testing ⇧

BOM ⇩
Packaging ⇩
Testing ⇩

- Implementation of WDM transceiver in CMOS allows to utilize **testing** practices of microelectronics industry
  - Wafer-scale testing in the middle of CMOS line
  - Wafer-scale system test at the end of CMOS line
  - Module test after packaging of best-known die

Considerations on WDM uncooled operation

- LAN WDM with flat-top
  - Operation within 40°C pp

- DC DFB laser
  - Usual temperature constraints for 25Gbps DML DFB are not very relevant for DC DFB
  - Main concern for DC DFB:
    - Variation of slope efficiency
    - Variation of laser wavelength
  - Both can be addressed by on-chip track-and-lock control circuitry

- Case temperature control vs die temperature control

Summary

- WDM NRZ CMOS-integrated single-chip TRX solution is considered
- Presented considerations on cost reductions looks promising
- Rigorous RCA analysis is required
- Feasibility requires further investigation