10GBASE-T Tutorial Overview

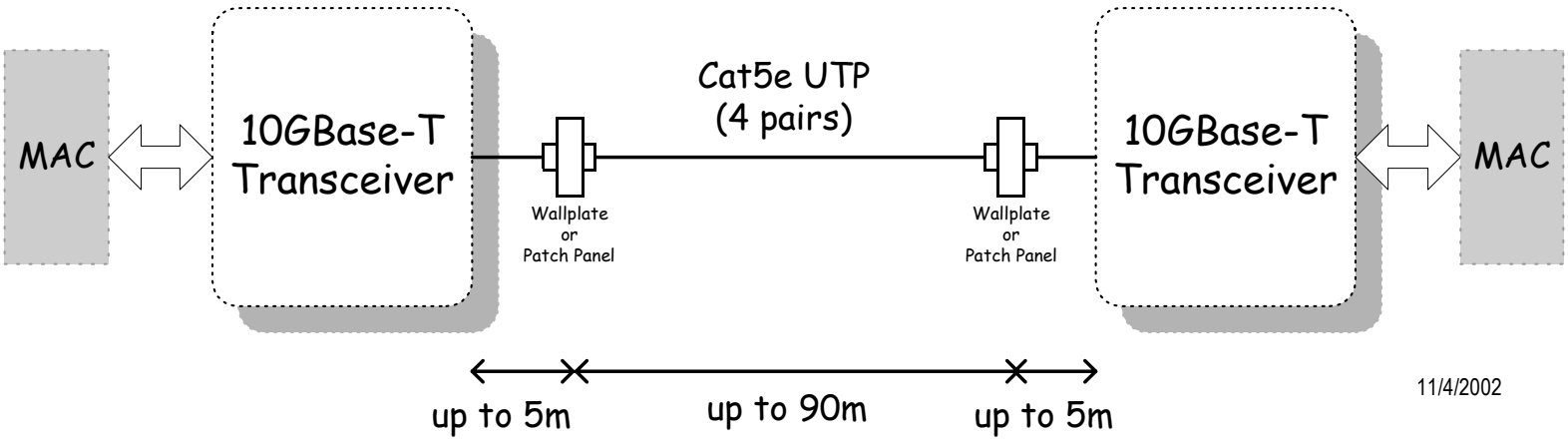
William Jones
Solarflare Communications

Introduction: Realizing 10GBASE-T

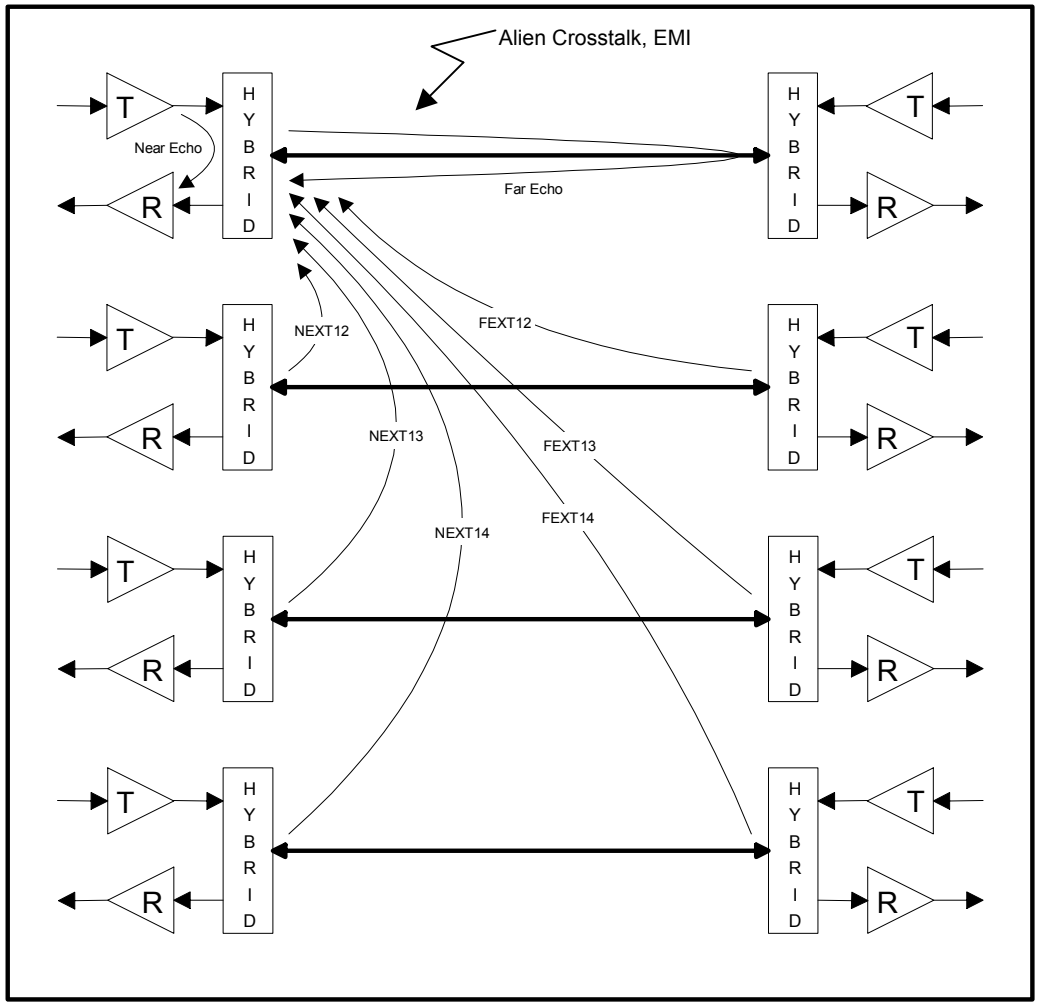
- Application Overview
- Cabling & Impairments
- Strawman System
- Implementation
- Performance Results
- Conclusion

Applications Overview

- 10-Gb/s Ethernet connections <= 100m
- Utilize installed base of structured Cat 5e UTP
- Upgrade from 1000BASE-T



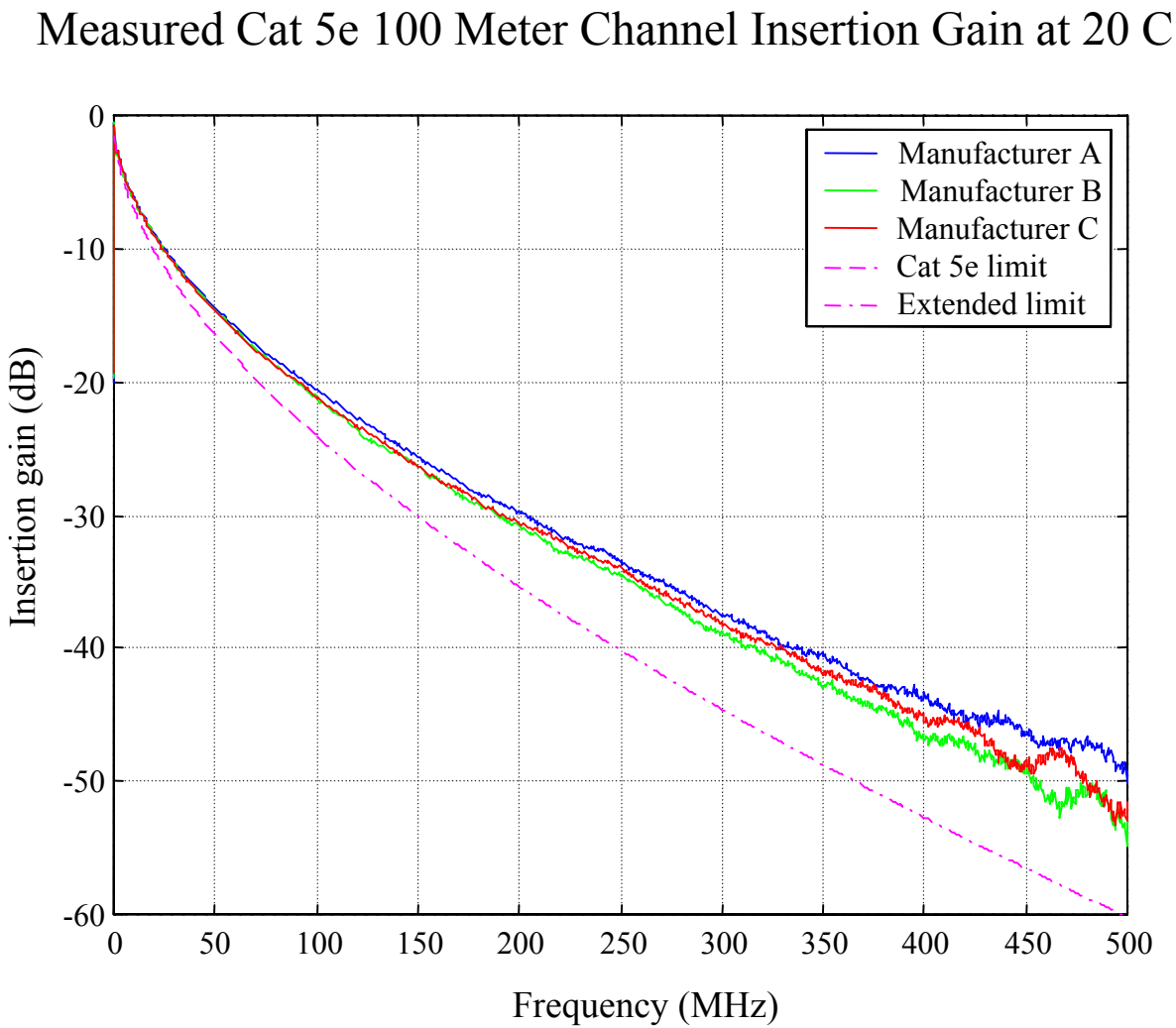
Channel Impairments



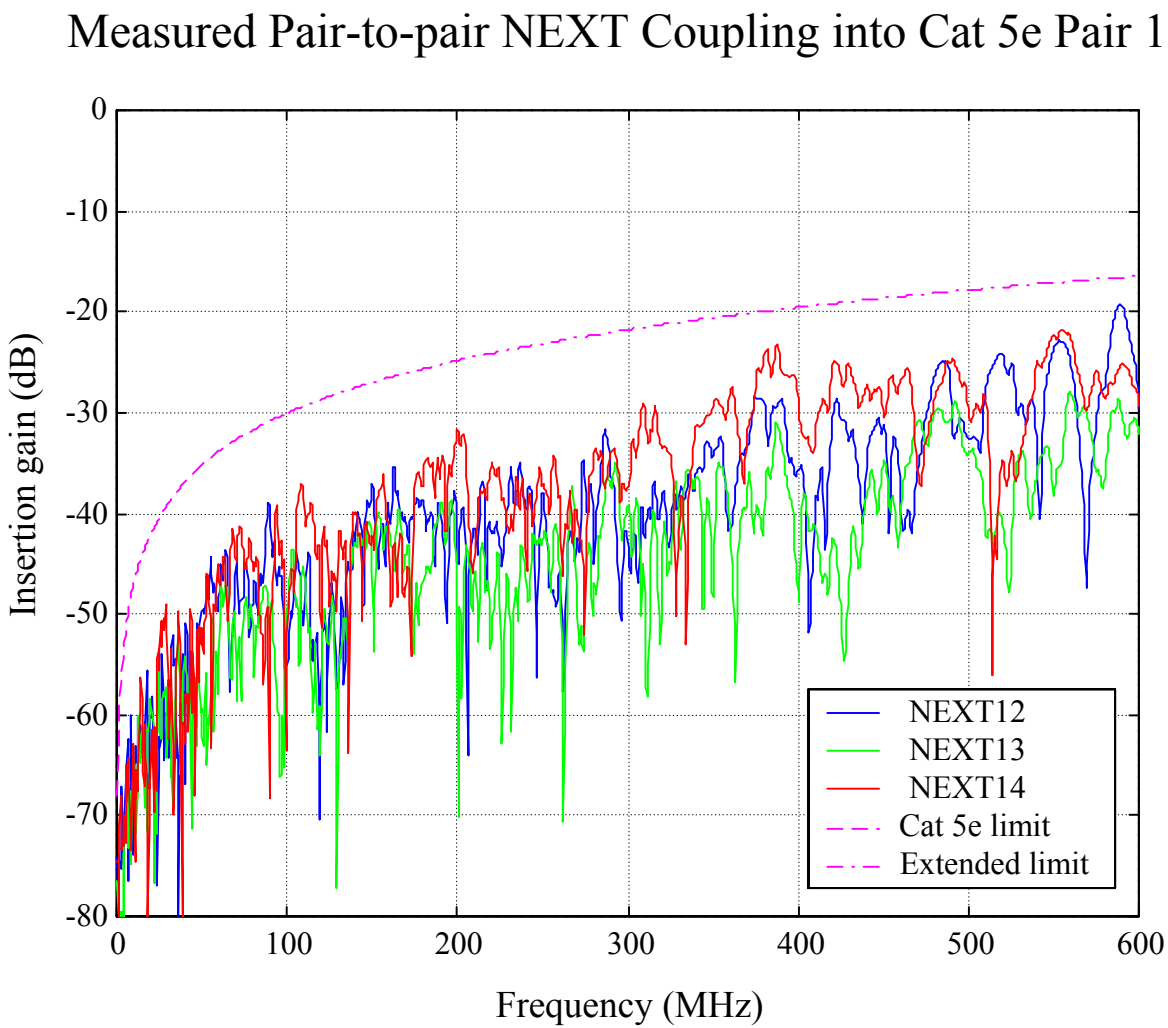
Characterization vs. Specification

- Cat 5/5e cable must be high quality with minor structural variations to meet TIA-568 requirements
- 100 MHz (or 250 MHz) "limit" imposed by TIA qualification requirements
  - not the physical limitations of the cable
- Cable properties stable beyond 500 MHz
  - depends mainly on transmission line geometry and construction materials
- Minor structural variations and connector discontinuities affect channel transmission, but not catastrophically

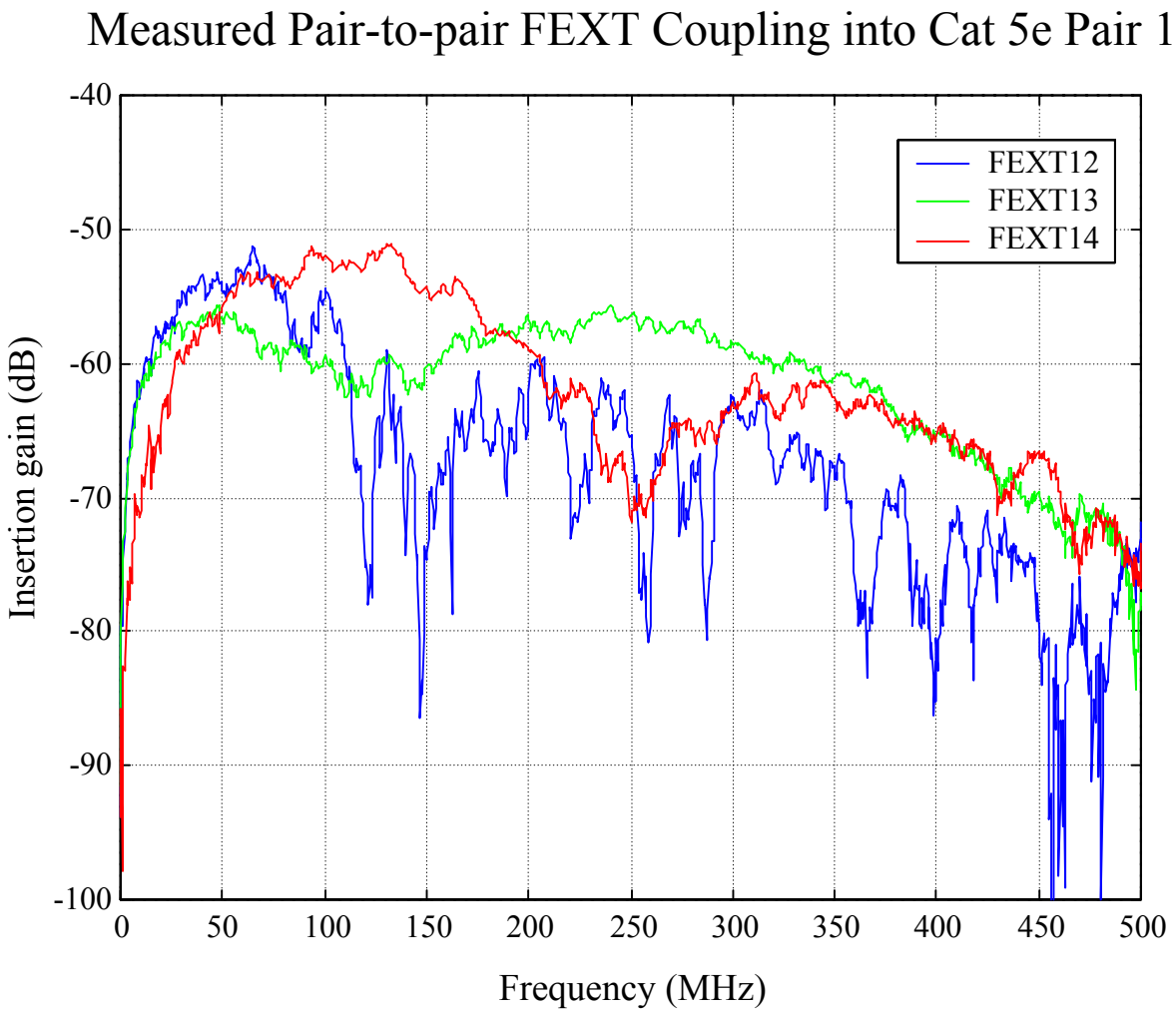
Cat 5e Channel: Insertion Loss



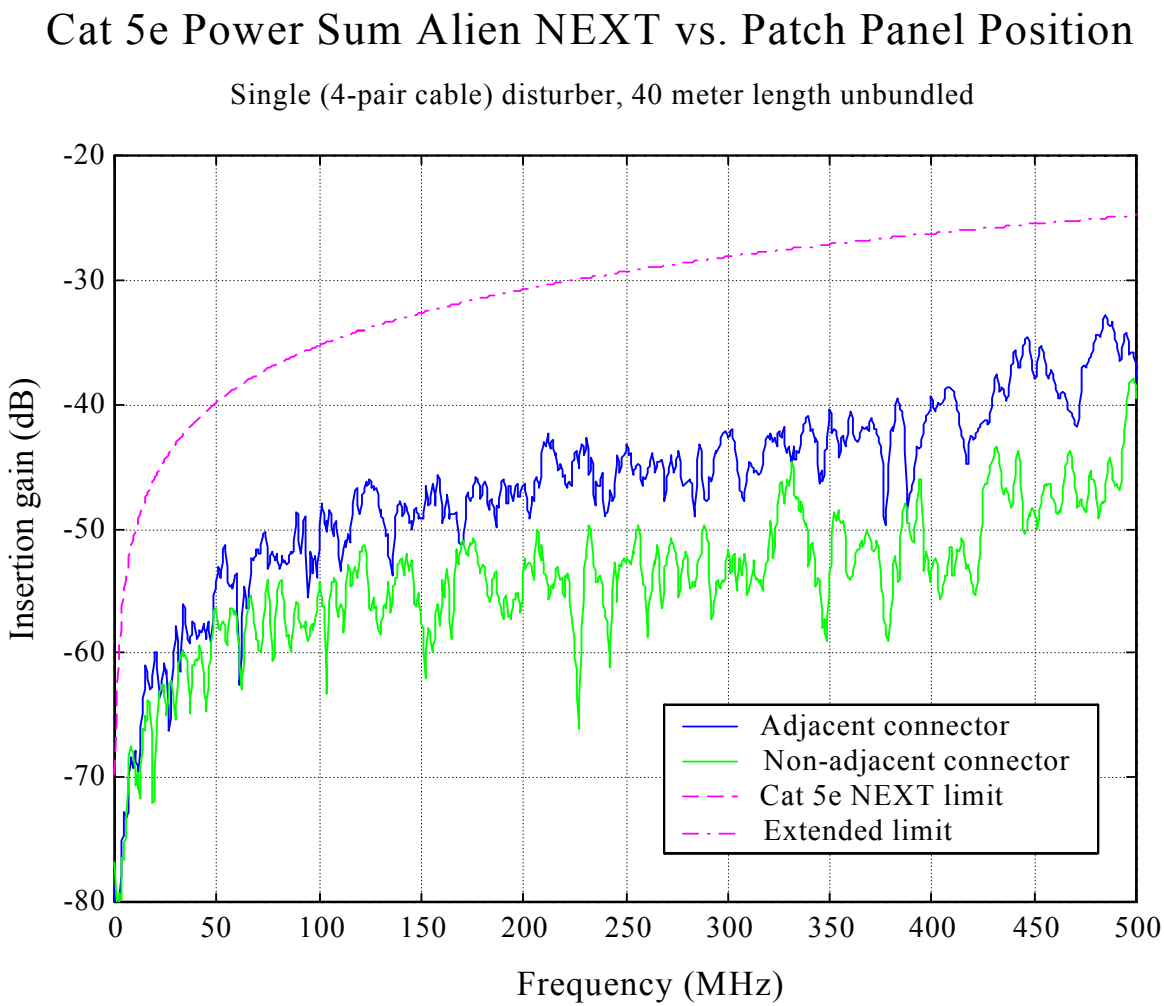
Cat 5e Channel: NEXT



Cat 5e Channel: FEXT

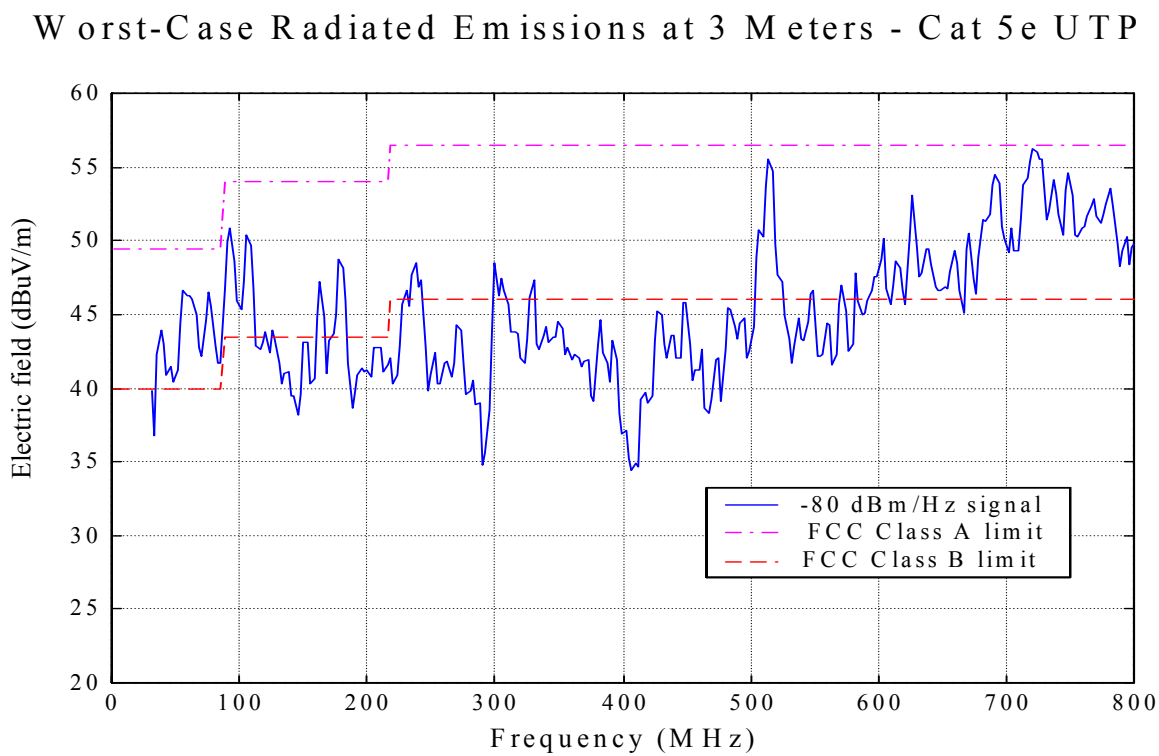


Alien NEXT


Cat 5e Power Sum Alien NEXT vs. Patch Panel Position
Single (4-pair cable) disturber, 40 meter length unbundled
Insertion gain (dB)
-20
-30
-40
-50
-60
-70
-80
0
50
100
150
200
250
300
350
400
450
500
Frequency (MHz)
Adjacent connector
Non-adjacent connector
Cat 5e NEXT limit
Extended limit

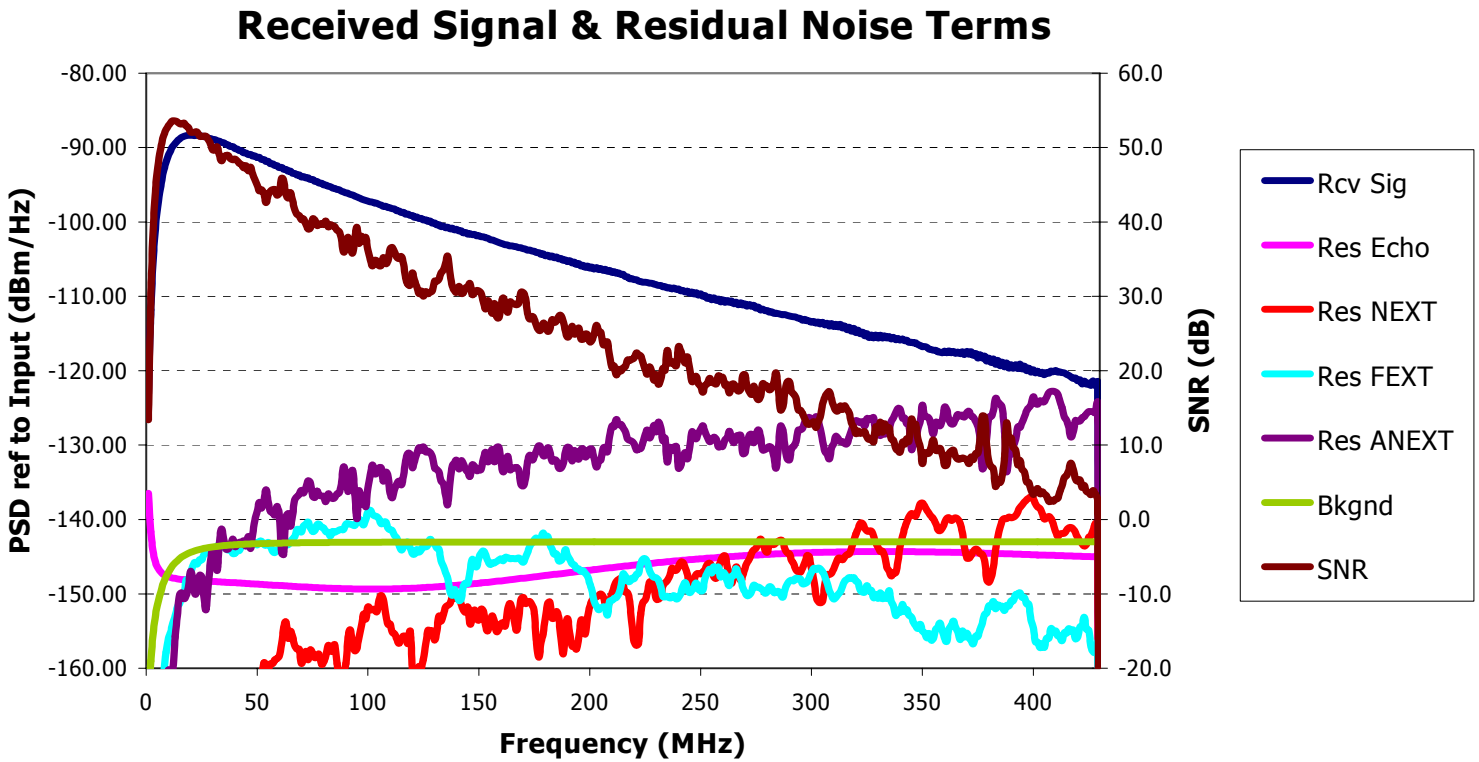
EMI - Emitted

- >100 MHz on Cat 5e can meet FCC Class A
  ~12 dBm launch power limitation
- < 500 MHz limits larger high frequency emissions



Baseline Requirements

- ~ 10 dBm Transmit power
- ~ 400 MHz Bandwidth
- ~ 40 dB Echo & NEXT Cancellation, ~ 20 dB FEXT Cancellation
- Alien NEXT suppression for crowded installations



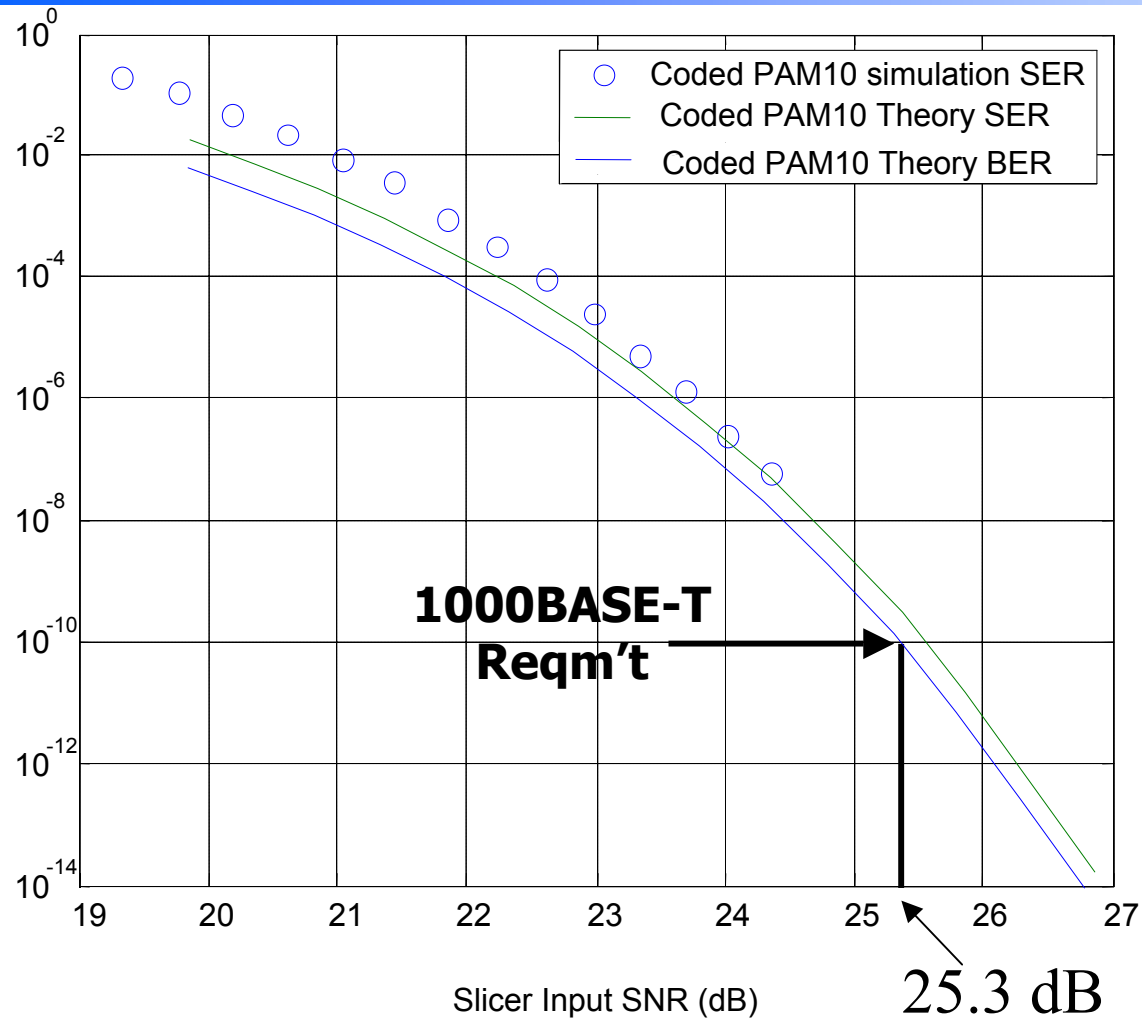
Strawman System: PAM-10 Coding

- Given the characteristics of the channel/disturbers, capacity is maximized with an analog bandwidth around 400MHz
- 10Gbps is achieved with a baud rate of 833MHz and 12 bits/baud or 3 bits/pair (4 pairs)
  - Minimum requirement of PAM8 for uncoded operation
- PAM9 may be sufficient for Ethernet control symbols
- PAM10 needed for both control and Trellis coding
- Extension of 1000BASE-T
  - 4D, 8-state Trellis code (one dimension per pair)
  - 6 dB coding gain relative to uncoded 10PAM

Comparison With 1000BASE-T

1000BASE-T	Straw Man 10GBASE-T
Multilevel coded PAM signaling (2-bits/symbol)	Multilevel coded PAM signaling (3-bits/symbol)
5-level with Trellis code across pairs	10-level with Trellis code across pairs
Full duplex echo-cancelled transmission	Full duplex echo-cancelled transmission
125 Mbaud, ~80 MHz used bandwidth	833 Mbaud, ~400 MHz used bandwidth
Moderate NEXT cancellation	High-Performance NEXT cancellation
No specified FEXT cancellation	High-Performance FEXT cancellation

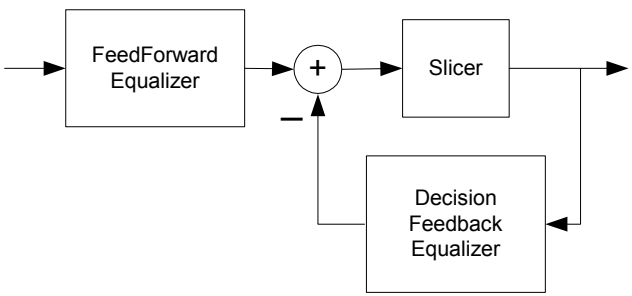
PCS SER & BER Straw Man Goal

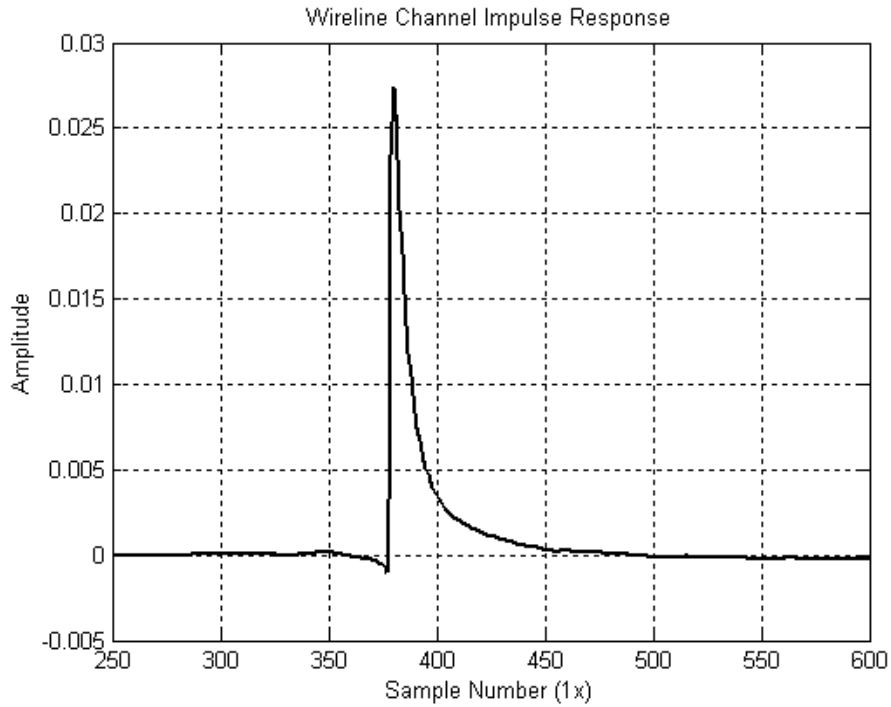


- For an aggregate slicer SNR of 25.3 dB with five dominating noise terms requires individually around 32 dB SNR

Implementation Requirement - ISI

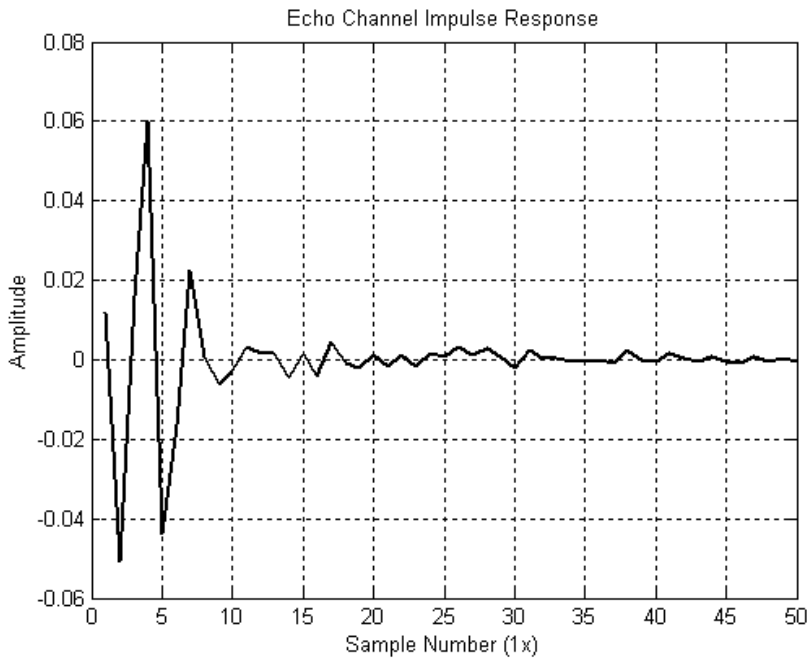
- Pre- & Post-Cursor Interference from limited Bandwidth
- Post-Cursor Dominates (>100 terms)
- Feedforward & Decision Feedback Equalization Solution





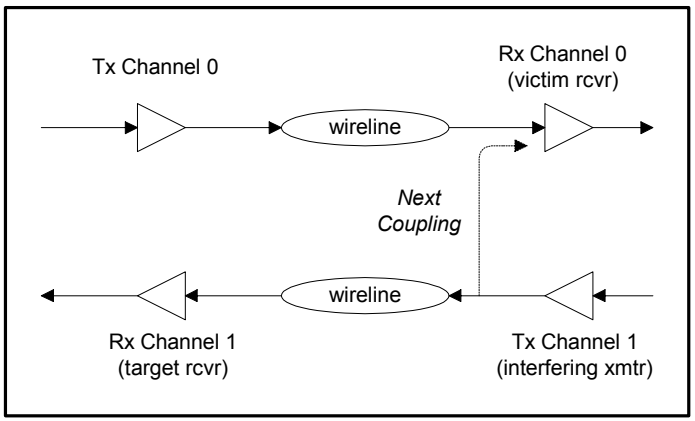
Implementation Requirement - Echo

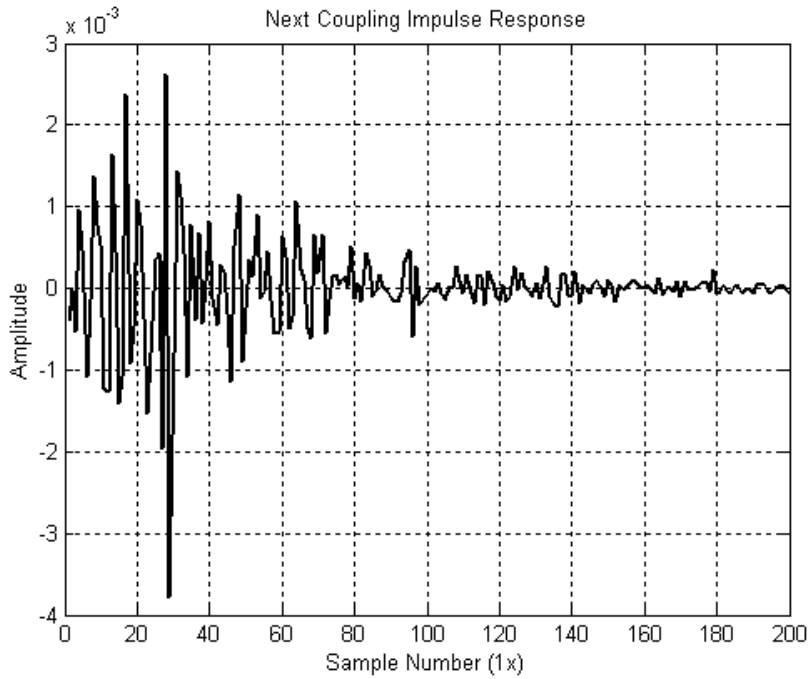
- Full duplex needed for limited BW
- Compromise hybrid for Tx/Rx isolation
- Impedance mismatches require residual echo cancellation
- > 40 dB rejection



Implementation Requirement - NEXT

- High-level interference from transmitters
- Very long response time
- > 40dB NEXT cancellation

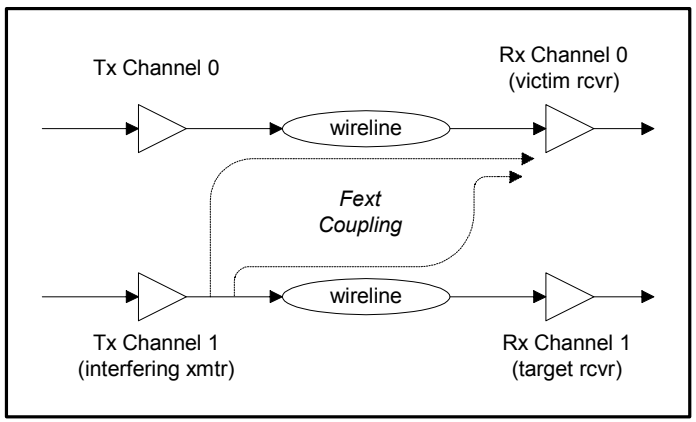


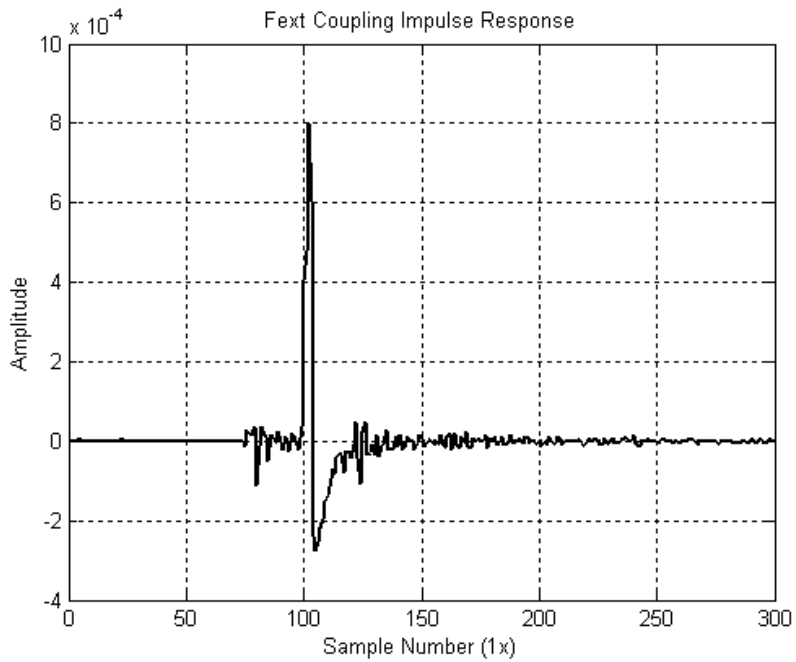


Implementation Requirement - FEXT

- Pre- and post-cursor elements of interference
- Based on an equal-level FEXT (ELFEXT) model
- Uncompensated in 1000BASE-T
- Must be cancelled in 10GBASE-T
- > 20 dB cancellation

$$H_{fext} = H_{elf} \cdot H_{chan}$$



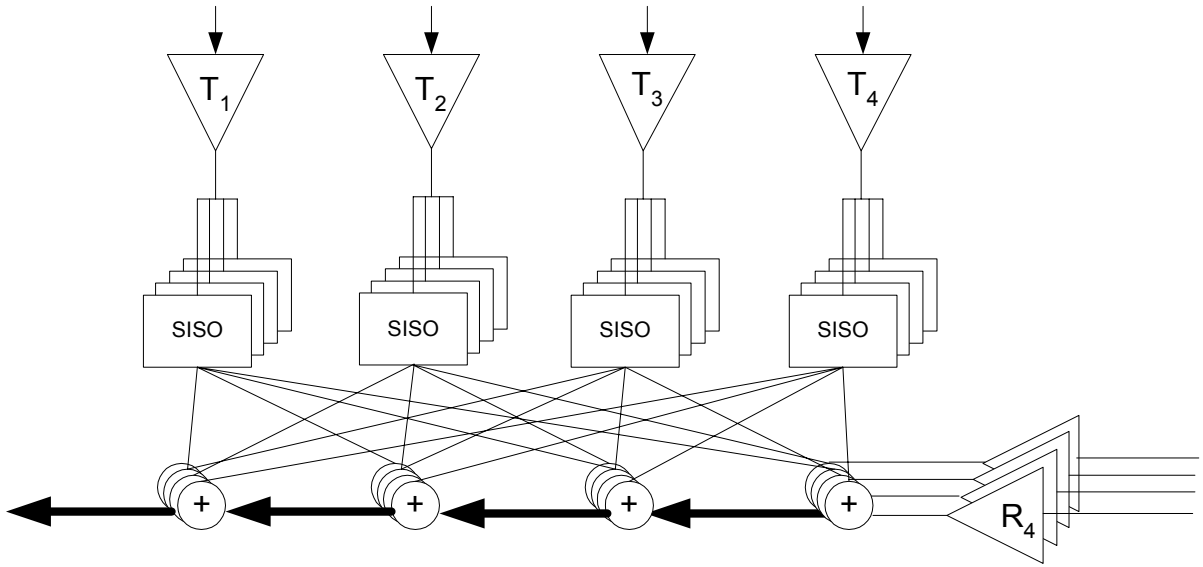


Challenging Implementation

- A new approach to problem solving needed to meet SNR requirement (> 25.3 dB)
- Efficient reuse of resources in MIMO modeling
- Utilization of parallel structures

Traditional Signal Processing

- Echo & NEXT cancellation

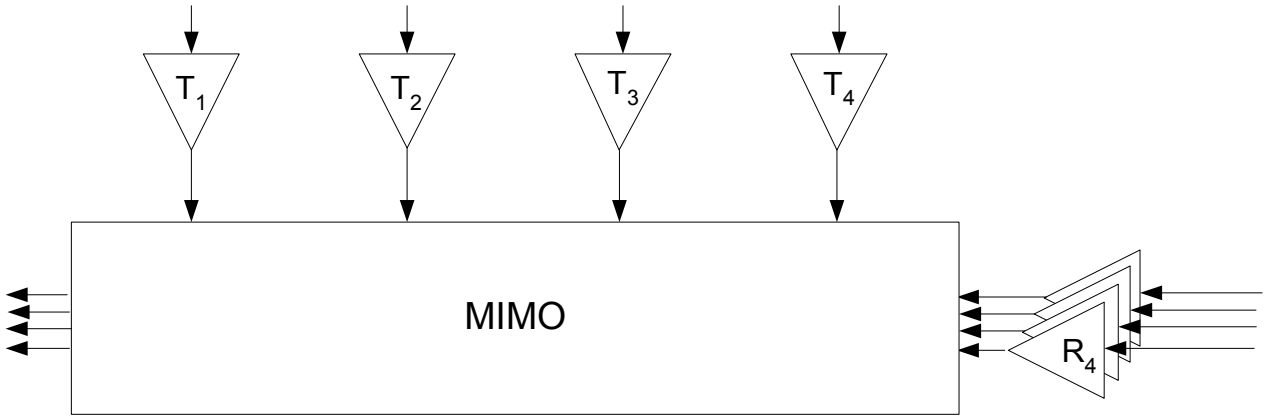


- 16 Single Input Single Output (SISO) processing elements (scalar filters)
- With canceller taps on the order of several hundred

  → 10 Tera Operations (TOps)!

Modern Signal Processing

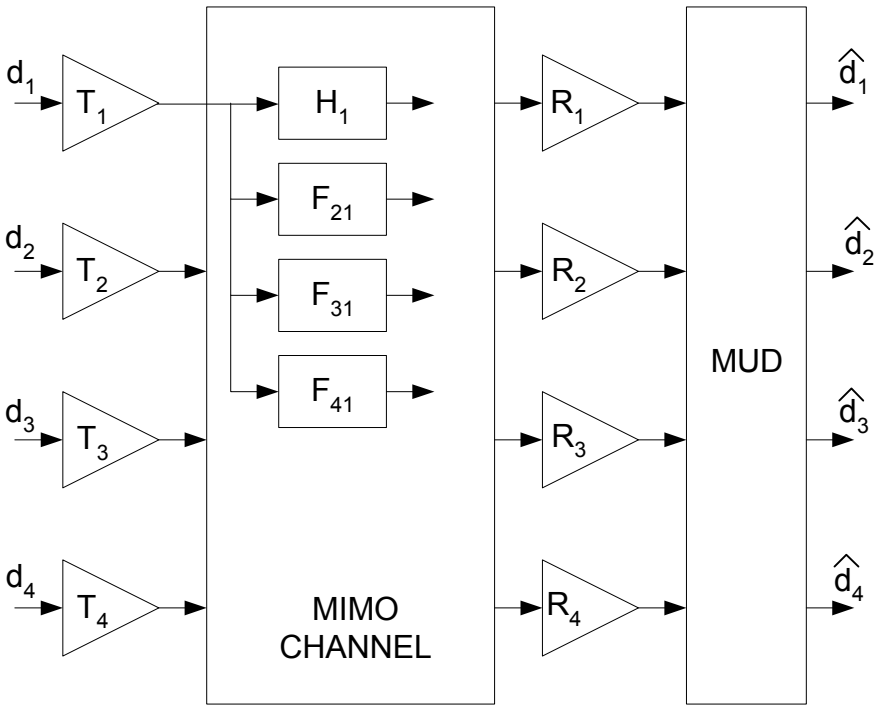
- Echo & NEXT Cancellation



- One Multiple Input Multiple Output (MIMO) processing element (matrix filter)
- Exploits correlation to reduce interference common to all received channels
- Enables massive reuse of computing resources

Modern Signal Processing

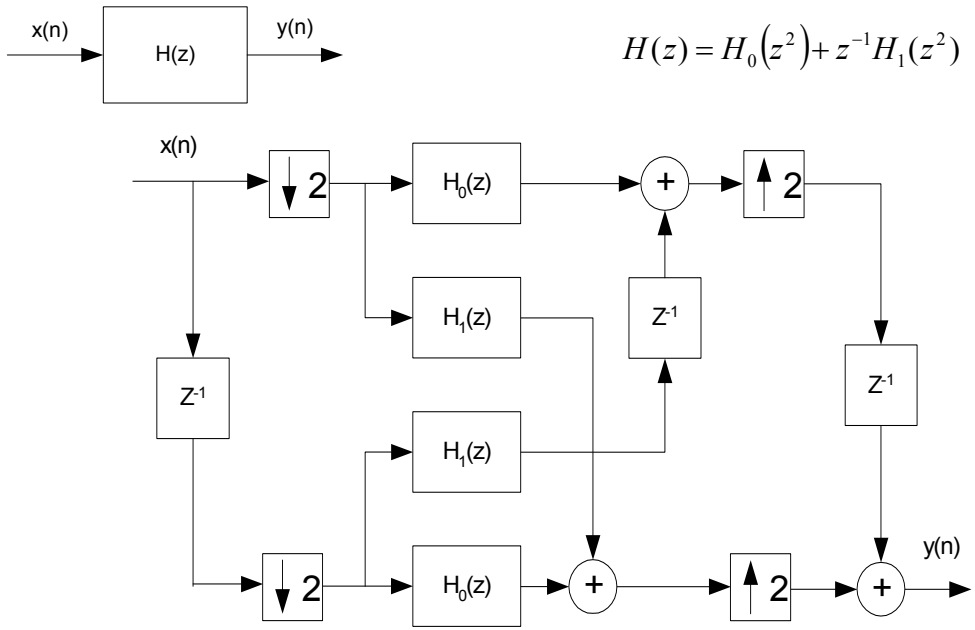
- Data recovery & Fext cancellation



- Multiuser Detector (MUD) of MIMO channel provides simultaneous data decisions & interference removal

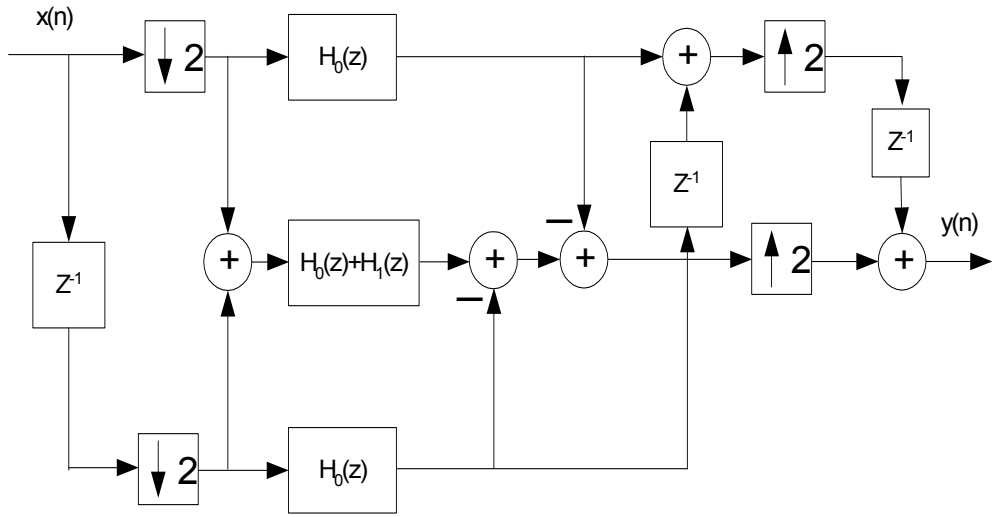
Parallelizing FIRs

- One high rate N tap filter



- Good for clock limited or high speed applications
- Four half rate N/2 tap filters
- Equivalent number of operations per unit time

Efficient Parallelization



- Four filters reduced to three
- 25% improvement in efficiency
- Greater efficiency with greater parallelism

Digital Circuit Straw Man Goals

- Puts total DSP requirements at 1.5 Tera Operations (TOps)
- Quad 1000BASE-T requires 1.0 TOps

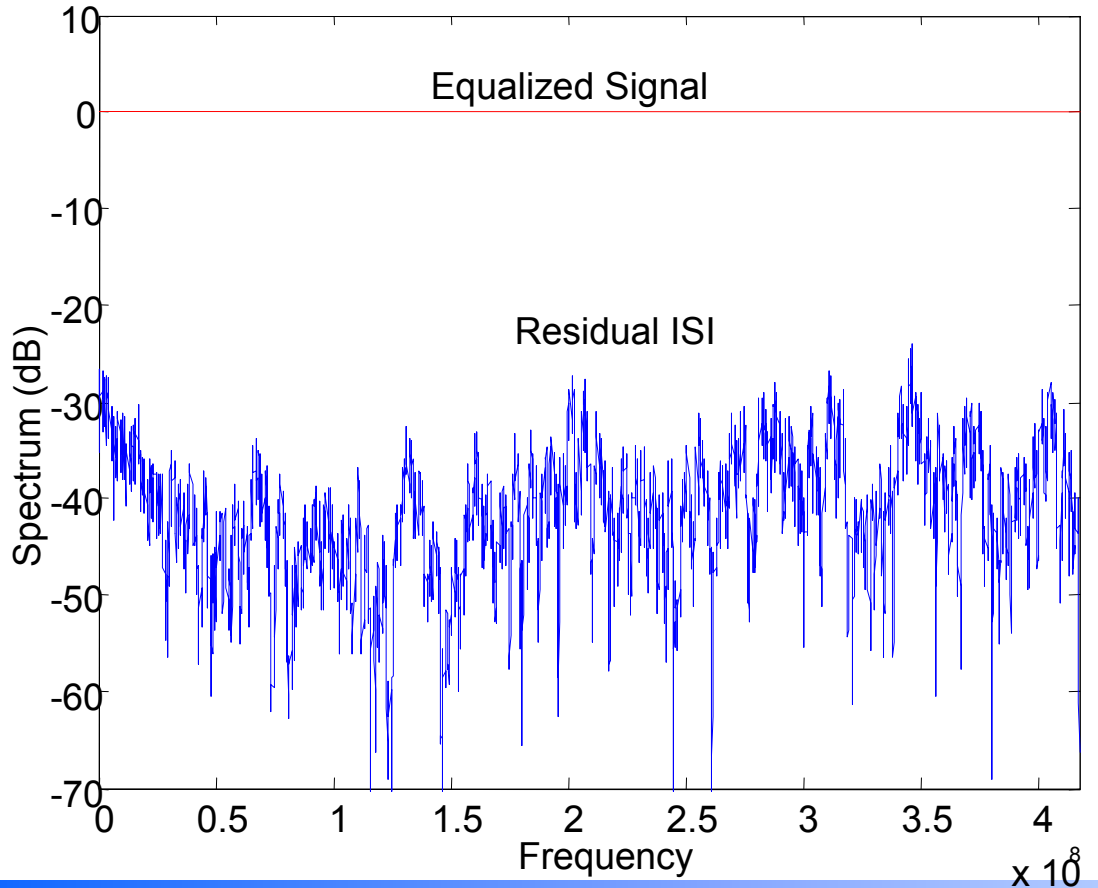
  → 150% increase in possible aggregation with 50% increase in complexity today!

- CMOS technology

Analog Circuit Straw Man Goals

- Transmitter: DAC & Line driver
  - >40 dB Linearity
  - 450 MHz Bandwidth
- Receiver: Hybrid, LNA & ADC
  - >8 bits ENOB
  - 833 MSPS
- Clock
  - 833 MHz
- CMOS technology

ISI Performance - After Equalization

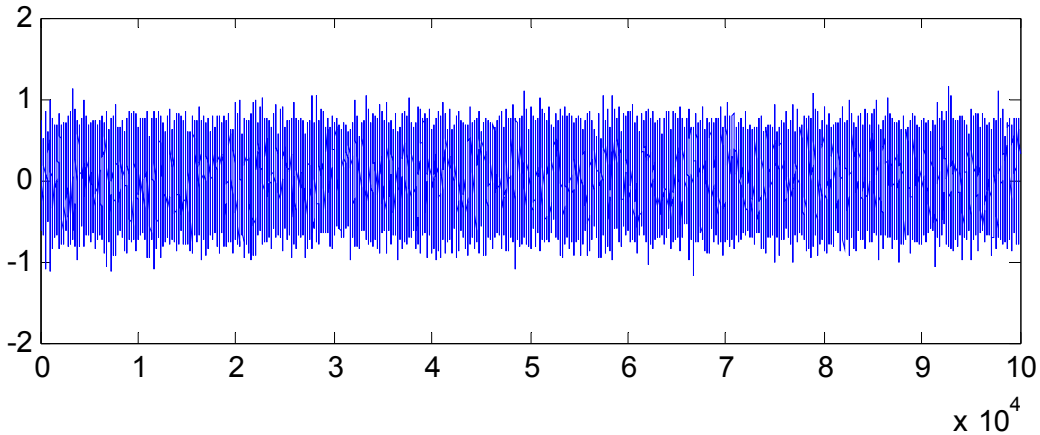


- FFE scales to produce unit variance hard decisions

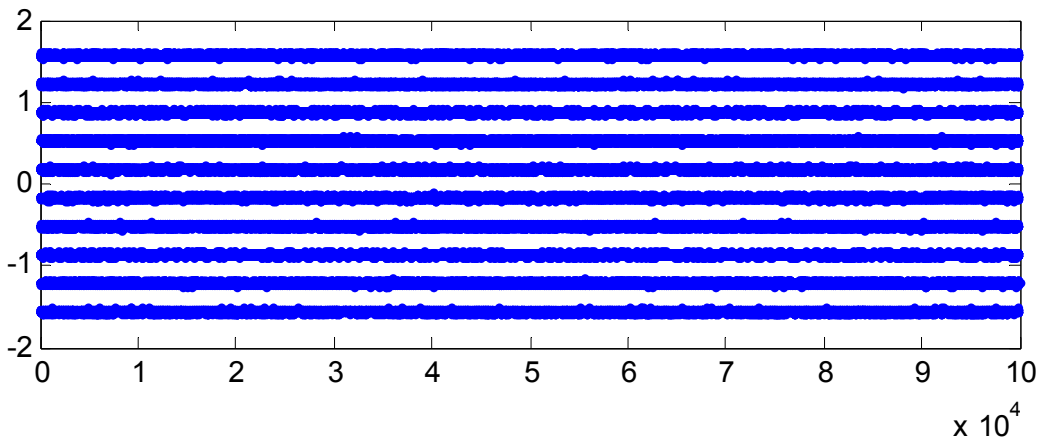
ISI Performance - Symbol Stream

a) Rx Far End Signal b) Slicer Input Vs. time

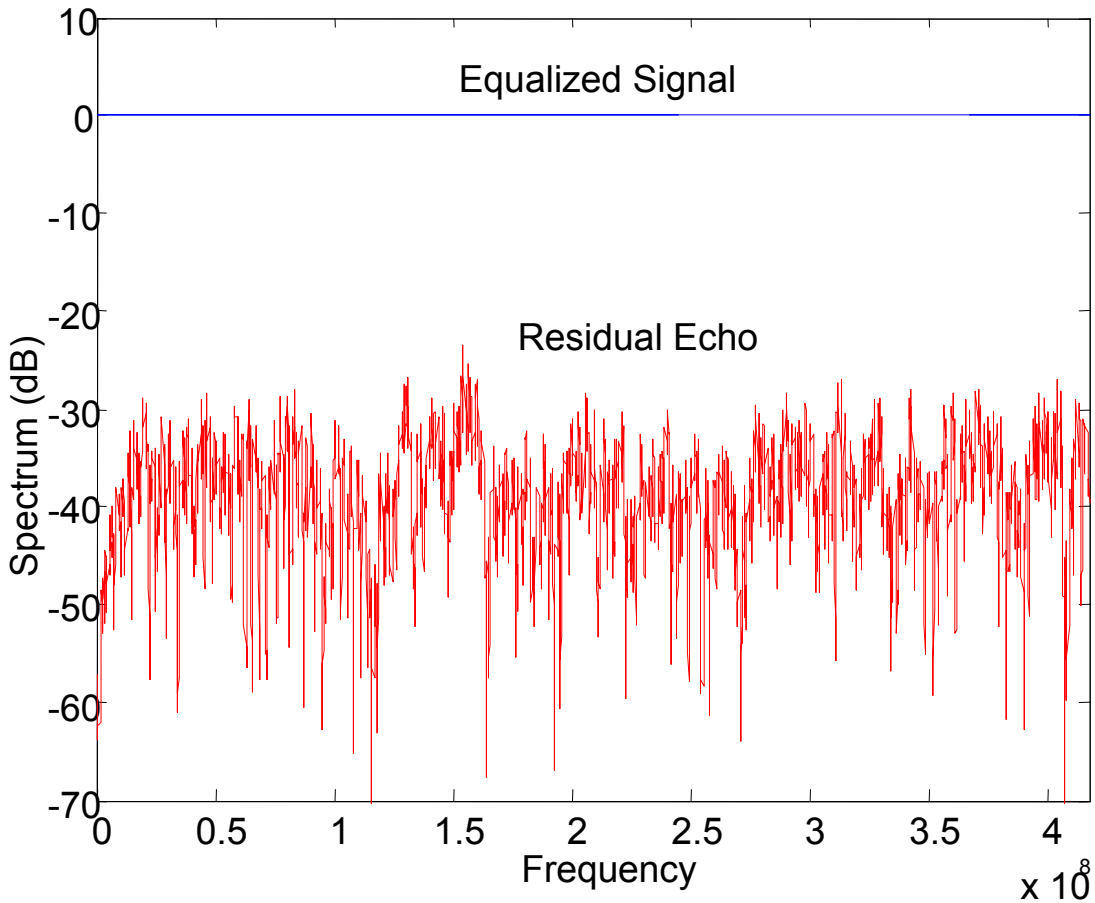
a)



b)

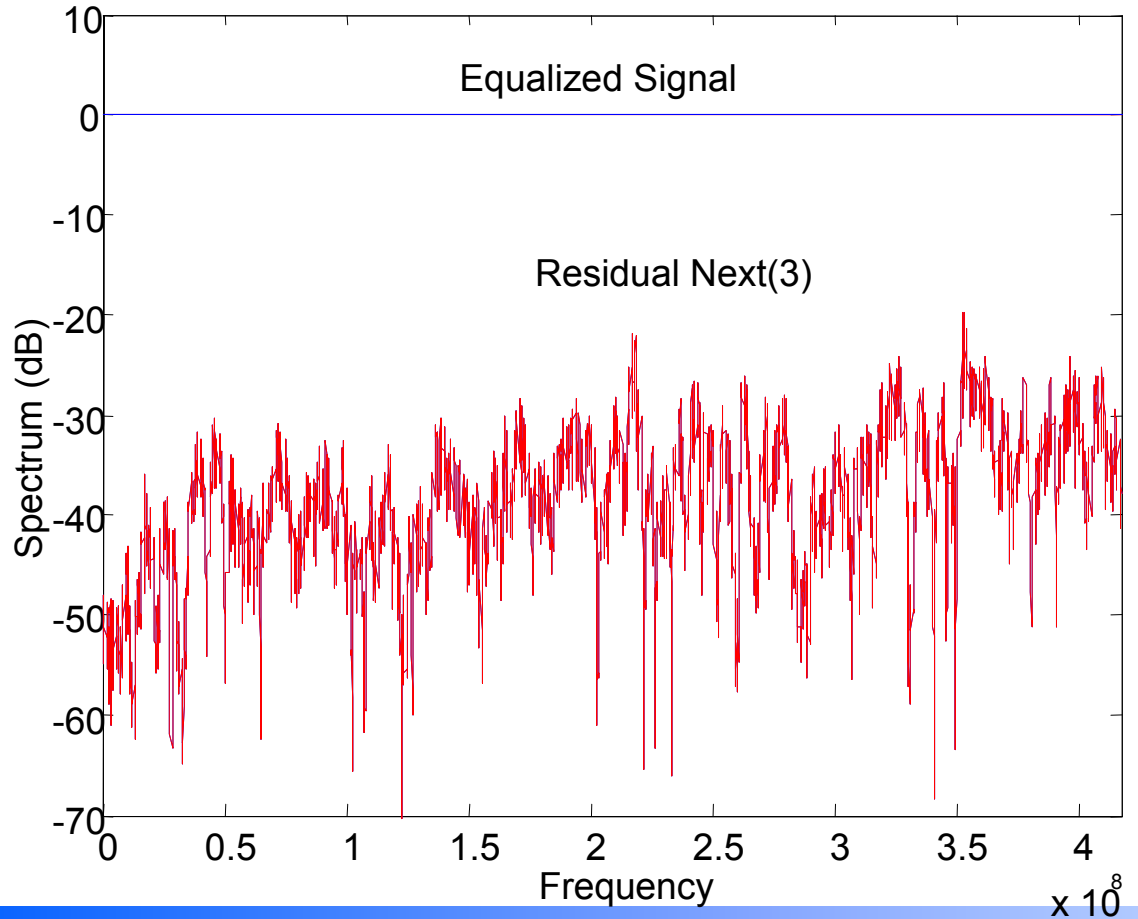


Echo Performance - SNR @ Detector



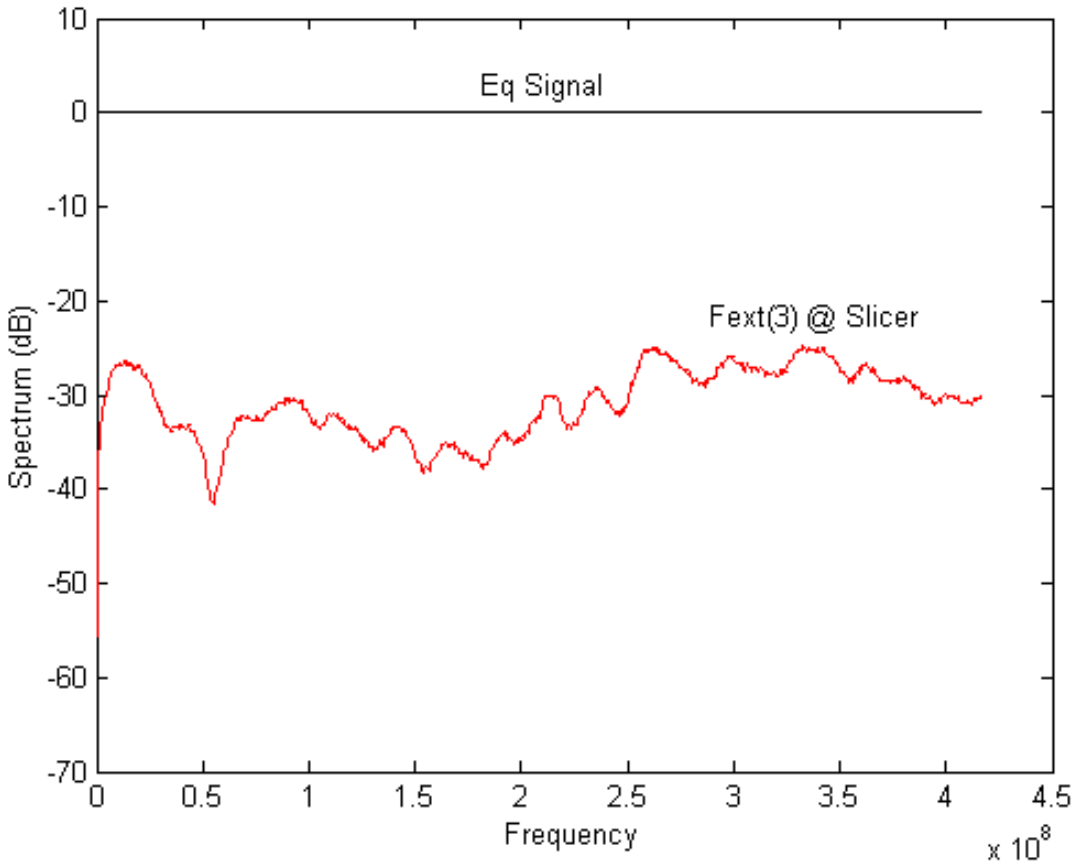
- FFE scales to produce unit variance hard decisions

NEXT Performance - SNR @ Detector



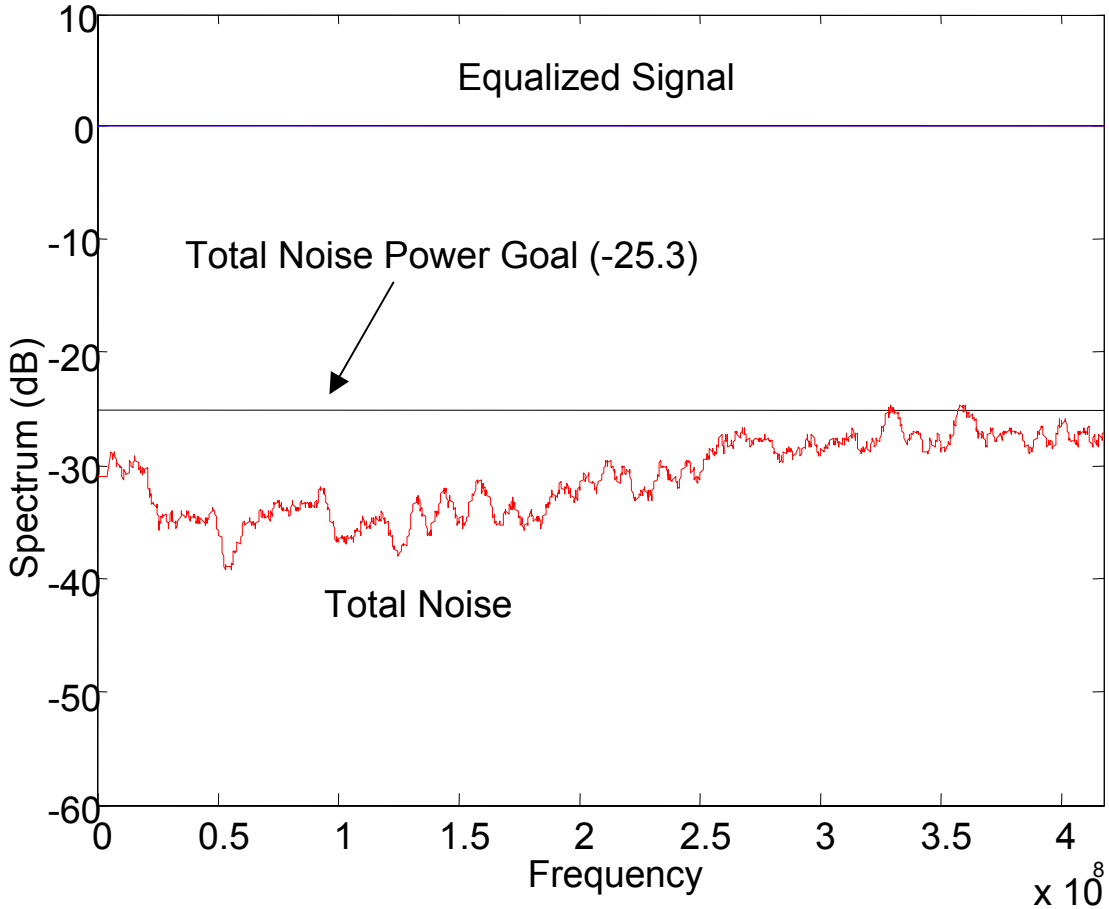
- FFE scales to produce unit variance hard decisions

FEXT Performance - SNR @ Detector



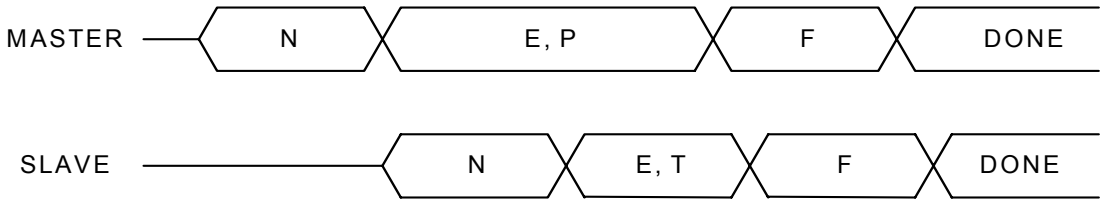
- FFE scales to produce unit variance hard decisions

Total Slicer SNR

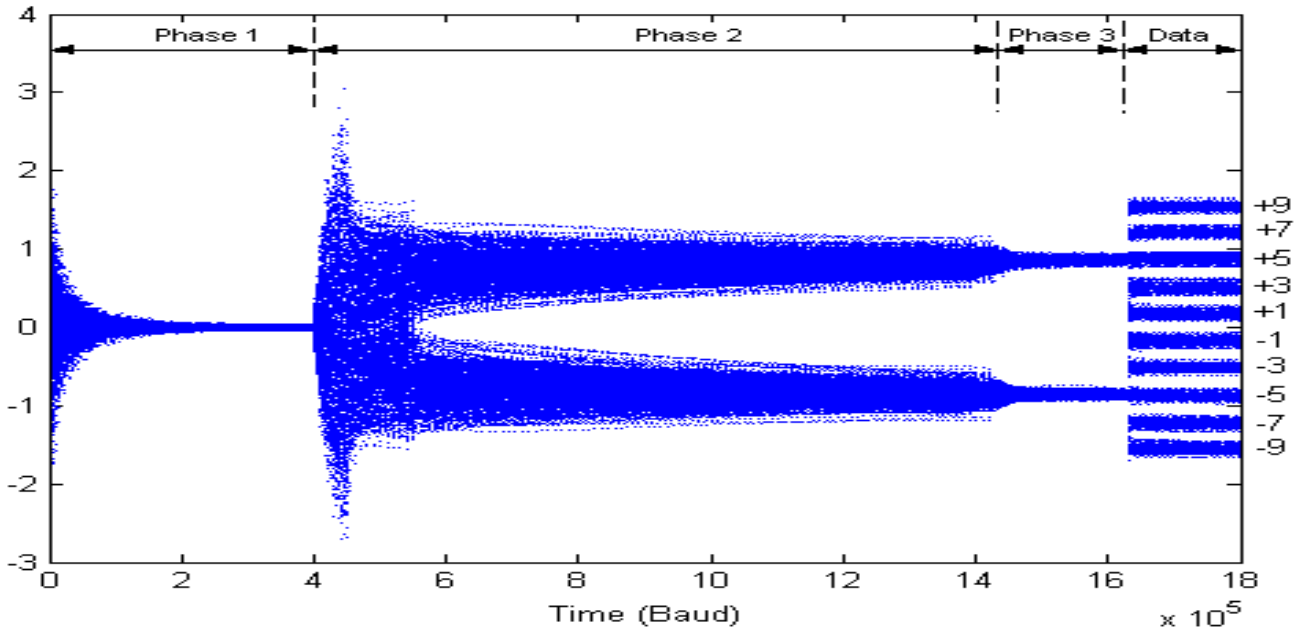


- FFE scales to produce unit variance hard decisions

Sequenced Startup



N = ECHO/NEXT Canceller Convergence
E = Equalizer Convergence
F = FEXT Canceller Convergence
T = Timing Acquisition
P = Phase Adjustment



Summary: Realizing 10GBASE-T

- Careful attention to media characterization beyond 100MHz
- Evolution of 1000BASE-T
- Modern signal processing methods
- Feasible CMOS realizations of digital & analog circuits
- Q&A