The 4D-PAM8 Proposal for 10GBASE-T

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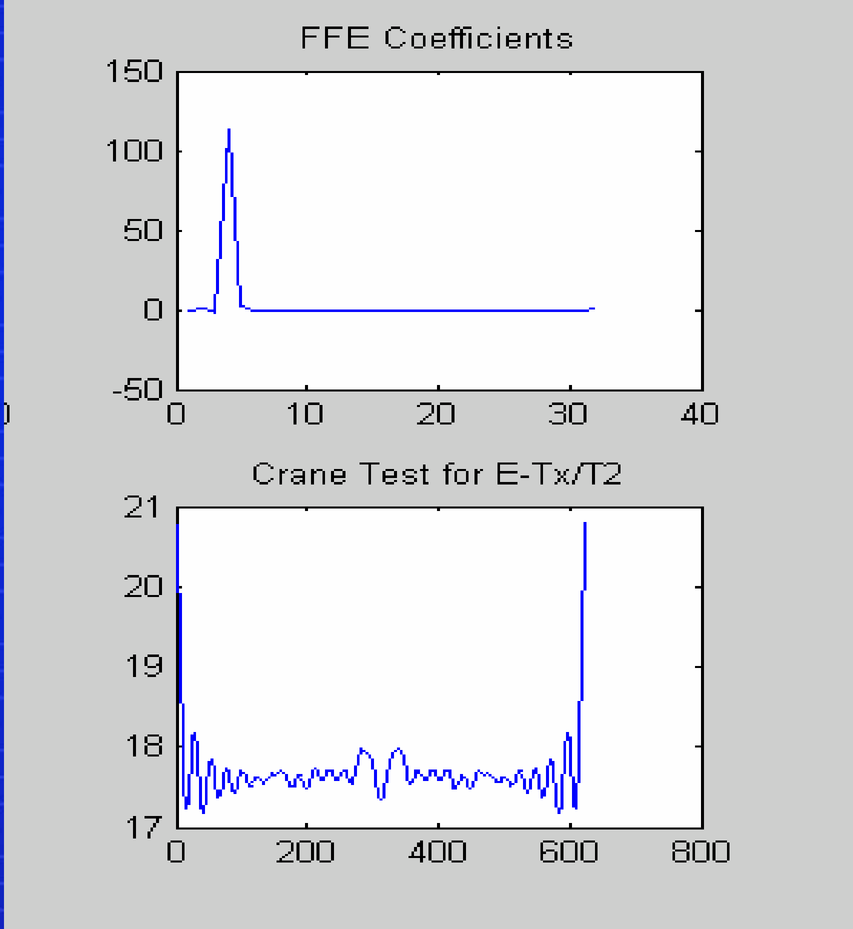
Agenda

- Current 10GBASE-T proposals
- Theoretical Noise Budgets
- Advanced techniques for 10GBASE-T
- Achieving 12dB coding gain
- Tomlinson Harashima pre-coding
- PCS Encoding
- Startup
- Concluding Remarks

Current 10GBASE-T proposals

- 625MHz PAM-20 (~Cicada), 833MHz PAM-10 (SolarFlare), 1250MHz PAM-5 (Plato Labs)
  - PAM provides the lowest peak-to-average ratio over other line code options.
  - Use PCS signaling and 4D Trellis coding of 1000BASE-T.
  - 6dB coding gain.
  - Assuming Cat-7 cabling for noise budgeting.
  - Assuming Launch voltage = 2V ptp (Plato)
    - compatible with 1000BASE-T, 100BASE-Tx
    - SolarFlare proposal uses ~3V ptp

Theoretical Noise Budget – 625MHz PAM20 = 17.2mV ptp on 100m CAT-7



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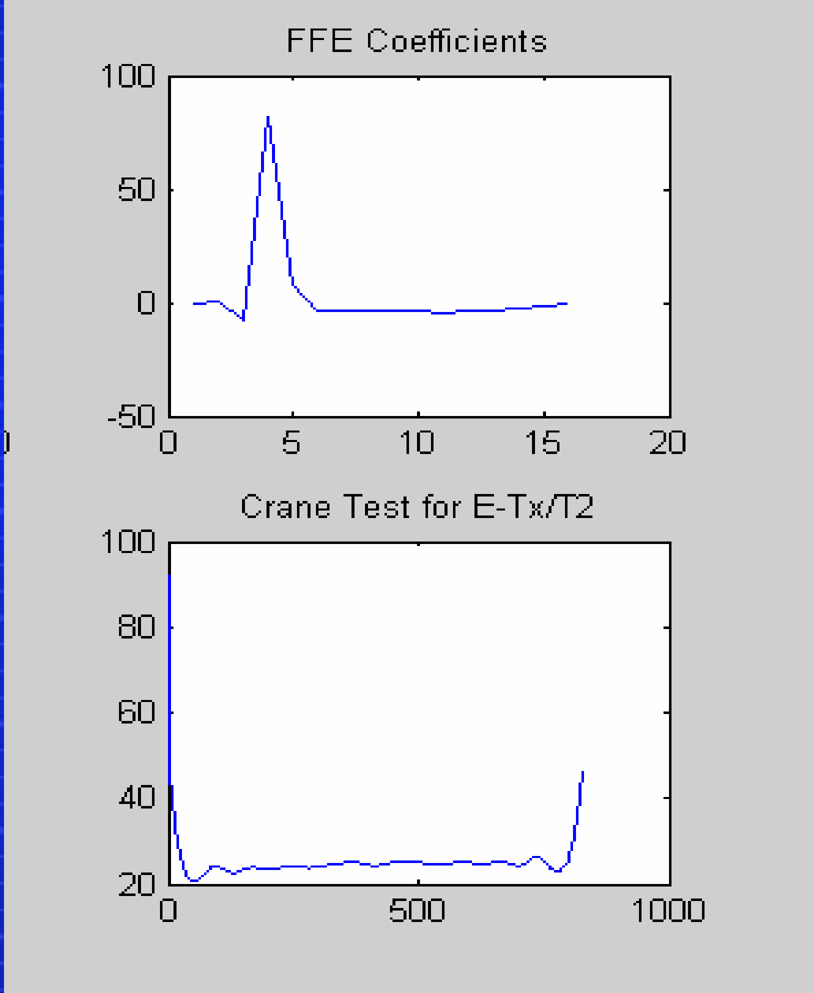
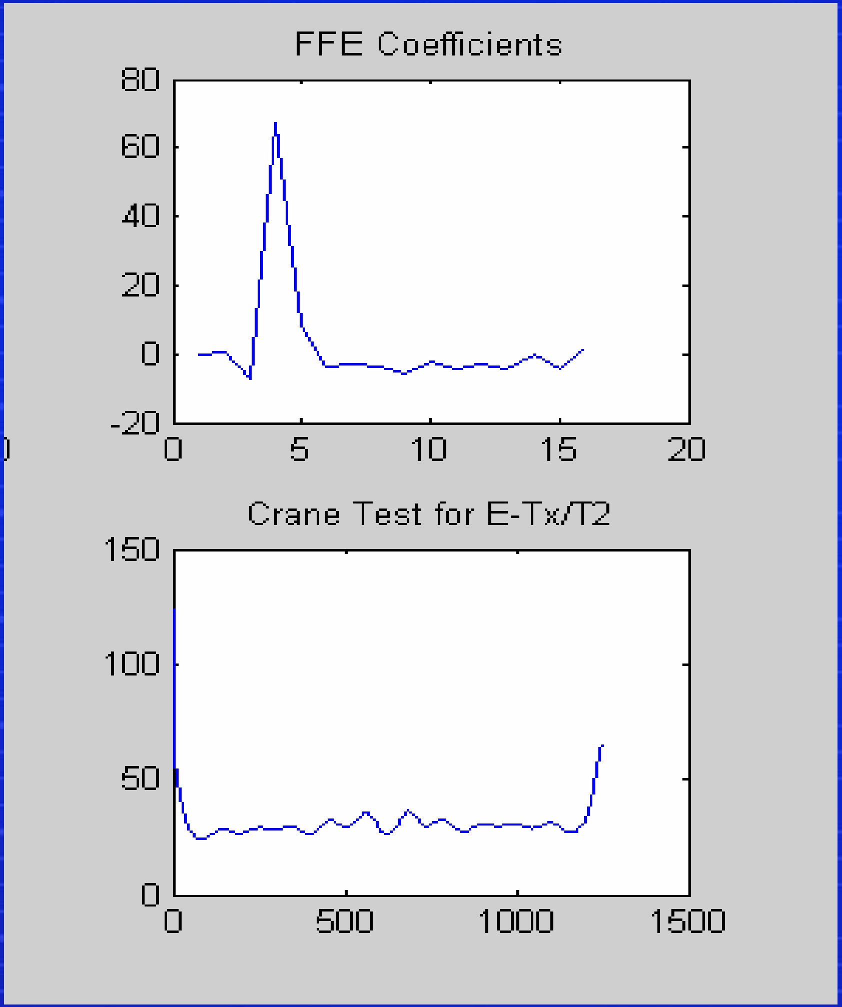
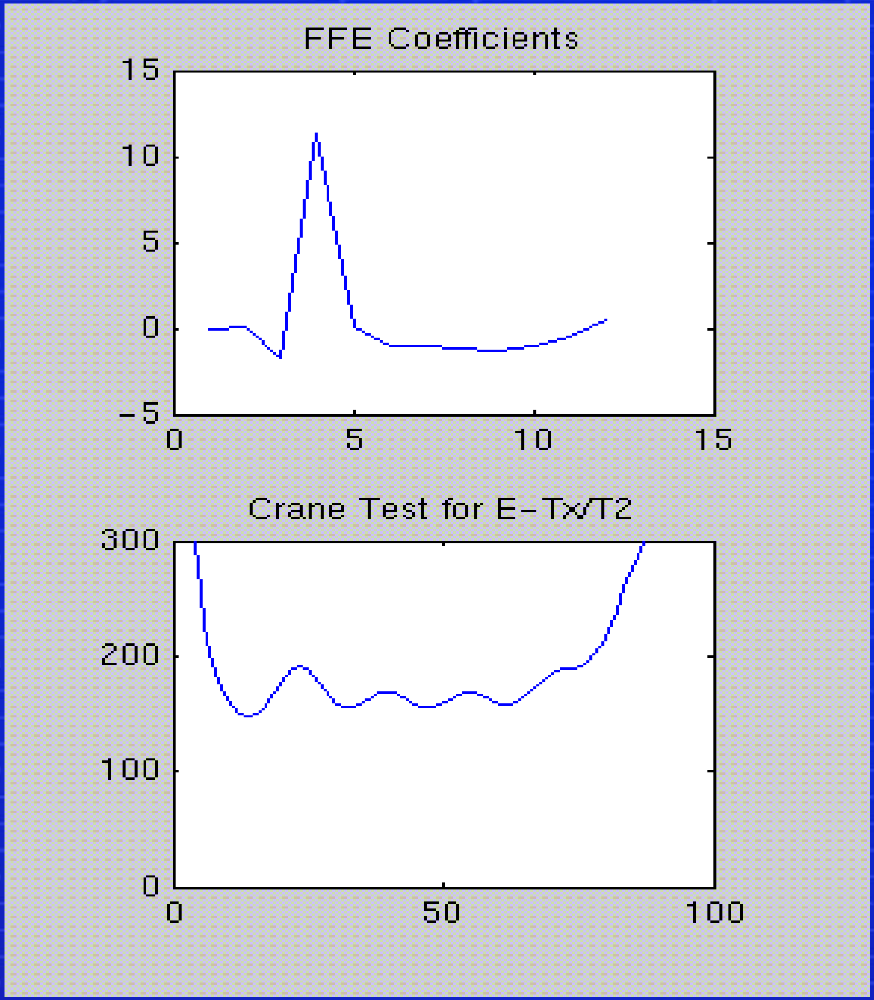
Theoretical Noise Budget – 833MHz PAM10 = 20.2mV ptp on 100m CAT-7



Theoretical Noise Budget – 1.25GHz PAM5 = 25mV ptp on 100m CAT-7



Theoretical Noise Budget – 125MHz PAM5 = 149mV ptp on 100m CAT-5



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On Current Proposals

- Need to improve coding gain of 10GBASE-T system to improve noise immunity!
- Much better system than 1000BASE-T can be designed with less stringent latency requirement
  - 880ns MDI-MDI round trip latency specified in 1000BASE-T for back-to-back operation.
  - if MDI-MDI round trip latency budget is on the order of 1us for 10GBASE-T, we can use significantly more powerful techniques to improve robustness of 10GBASE-T
- 1000BASE-T line code and Forward Error Correction (FEC) code were designed for half-duplex operation
  - Strict latency budget requirements of CSMA-CD necessitated simple FEC codes
    - 4D TCM used in 1000BASE-T shows weak Bit Error Rate reduction as a function of receiver Signal to Noise Ratio
- Half-duplex operation is not supported in 802.3ae 10G MAC

Advanced Techniques for 10GBASE-T

- Capacity Approaching Forward Error Correction (FEC) Code
  - Gallagher's Low Density Parity Check (LDPC) Block Code
    - Achieves strong BER reduction as a function of SNR
- 12dB co-set partitioning for improved noise tolerance
  - 6dB co-set partitioning used in 1000BASE-T
  - Doubles noise tolerance over 6dB partitioned codes
- Tomlinson-Harashima pre-coding to reduce receiver complexity
  - allows spectral shaping in the transmitter to reduce alien cross-talk coupling
  - eliminates Decision Feedback Equalizer (DFE) error propagation, even with large DFE coefficients

Capacity Approaching Code

- Gallagher's Low Density Parity Check (LDPC) Code
  - First introduced in Robert Gallagher's MIT PhD thesis in 1960
  - Re-discovered by Mackay and Neal in 1995. Since then,
    - used in high performance optical networking systems
    - Proposed by JPL for use by Consultative Committee for Space Data Systems (CCSDS)
  - Receiver uses an iterative belief propagation decoder to achieve waterfall reduction of BER as a function of SNR.
  - uses sparse matrix techniques to minimize decoder complexity
    - reasonably low latency requirement in the decoder
    - allows block processing to reduce receiver complexity
  - can be based on provably good block codes to maximize Hamming distance between code words.
    - (2048,1723) Reed Solomon based LDPC code ensures regularity of encoder and decoder architecture, while allowing for 12dB coding gain.
    - Reference: Ivana Djurdjevic, Jun Xu, Khaled Abdel-Ghaffar, and Shu Lin, "A Class of Low Density Parity Check Codes Constructed Based on Reed-Solomon Codes with Two Information Symbols," IEEE Communications Letters, Vol. 7, No. 7, Jul. 2003, pp. 317-319.

12dB Co-set Partitioning

6dB co-set partitioning in 4DPAM-5 1000BASE-T (transmit 5 levels, but achieve noise immunity of 3 level transmission)

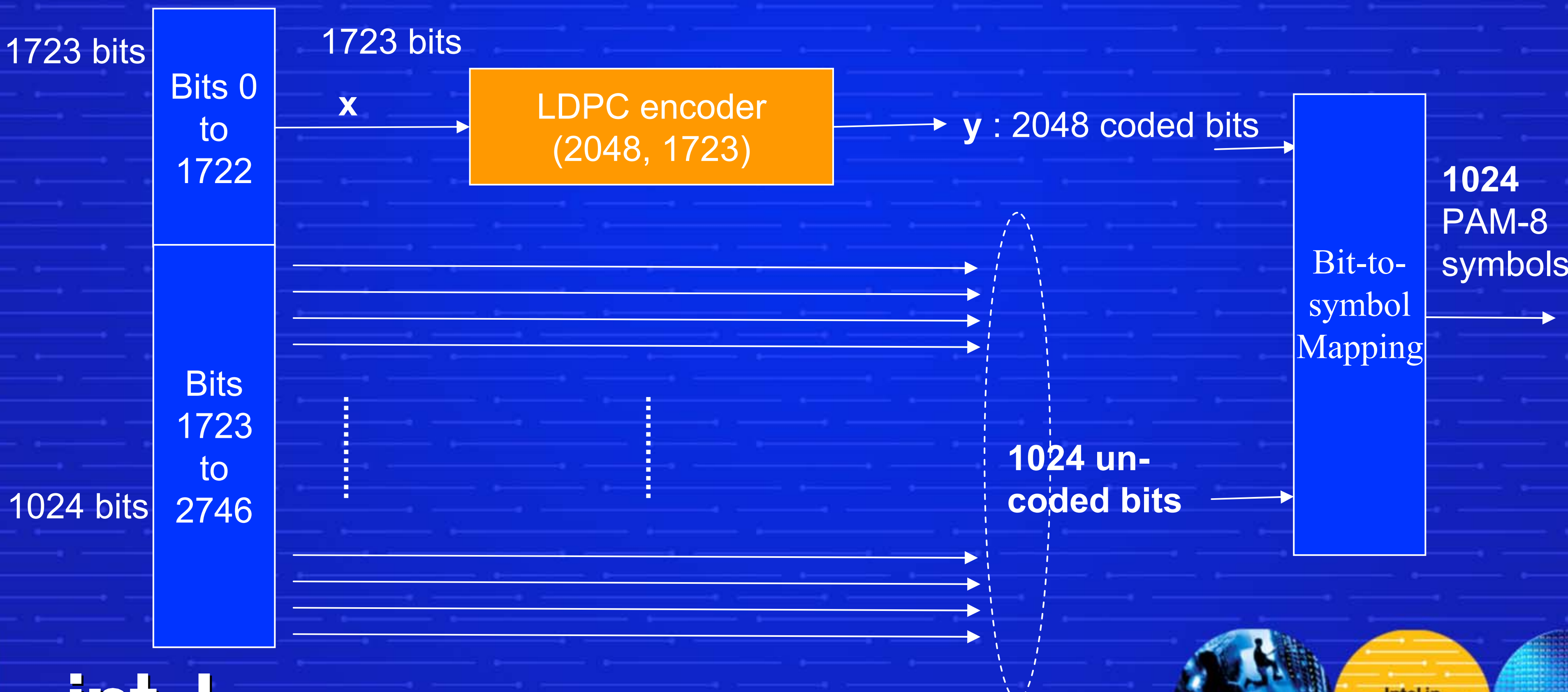
12dB co-set partitioning in 4DPAM-8 10GBASE-T (transmit 8 levels, but achieve noise immunity of 2 level transmission)

LDPC Co-set Encoding

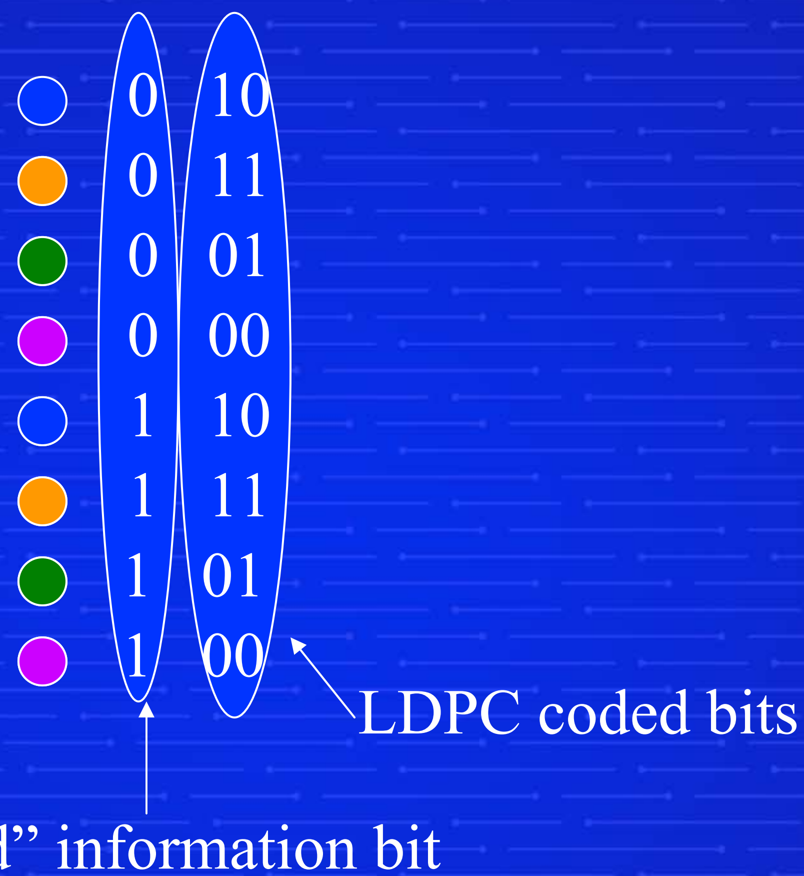
Data block size = 2560 bits over 256 symbols

Control block size = 187 bits

Information block size = 2747 bits = 1723+1024 bits



Bit-to-Symbol Mapping



Each coded bit difference contributes an Euclidean distance of 4.

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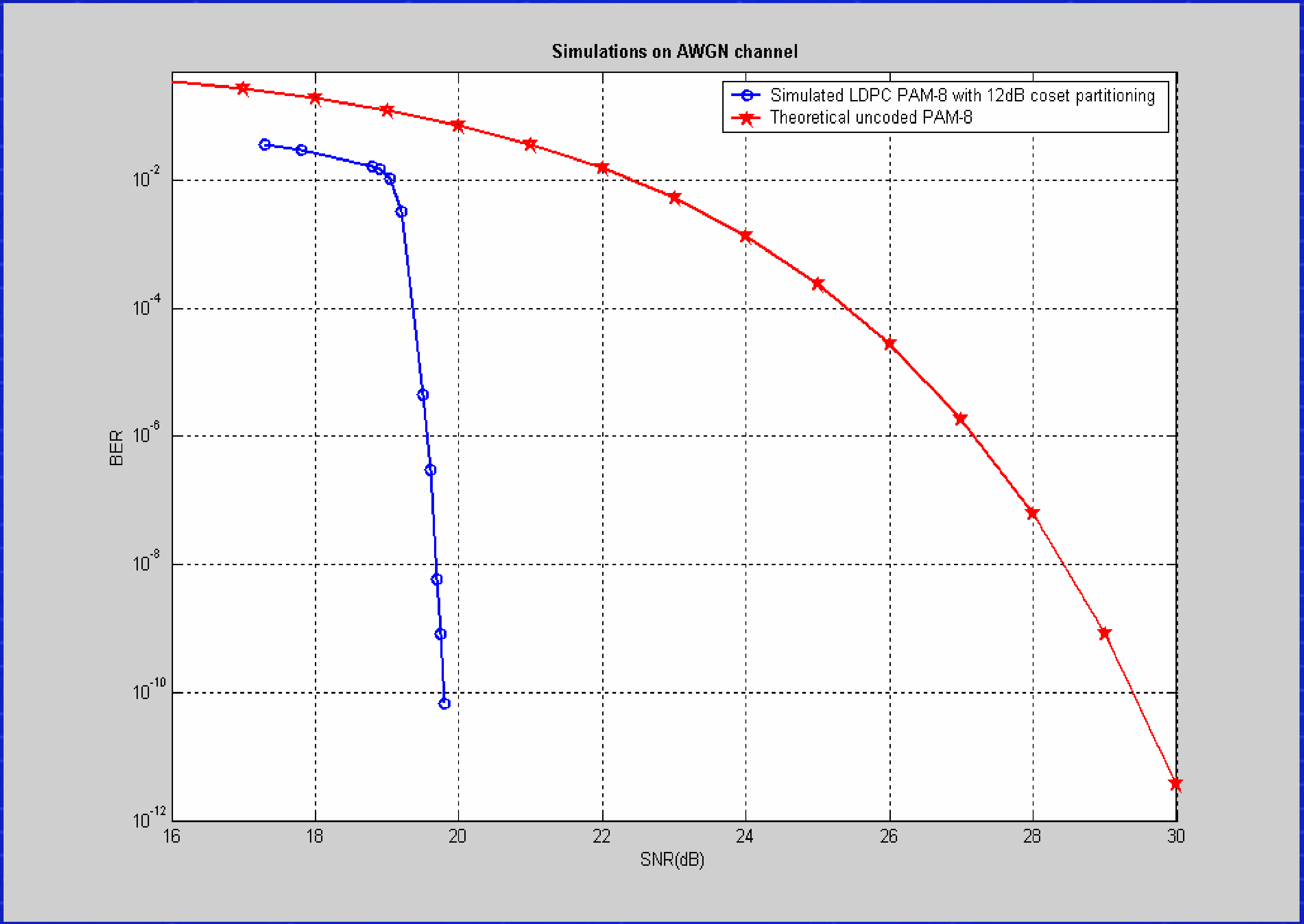
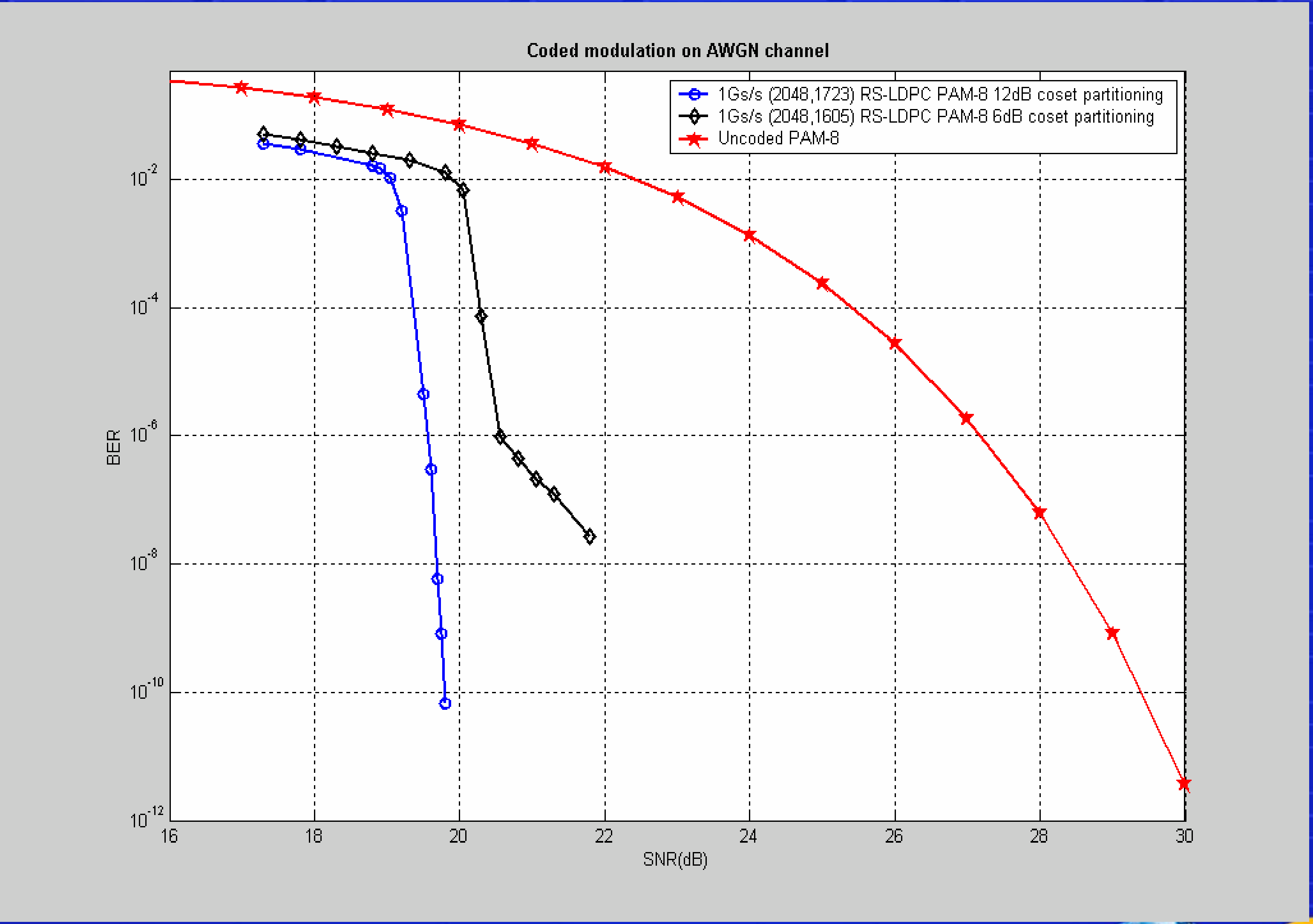
(2048,1723) RS-LDPC Code Properties

- Girth of the Tanner graph = 6
- Degree of each variable node in Tanner graph = 6
- Degree of each check node in Tanner graph = 32
- Hamming distance of the code = 8
- Minimum Euclidean distance between 4D PAM-8 code words >= 16
- Euclidean distance between points in each co-set is 16.
- Therefore coding gain over un-coded PAM-8 is 12dB.

Example Simulation results

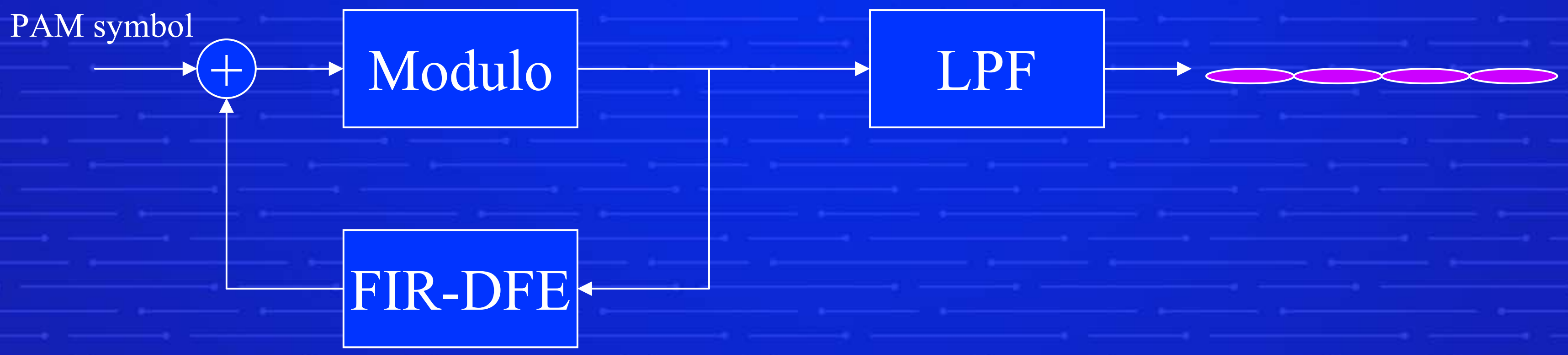


Simulation results

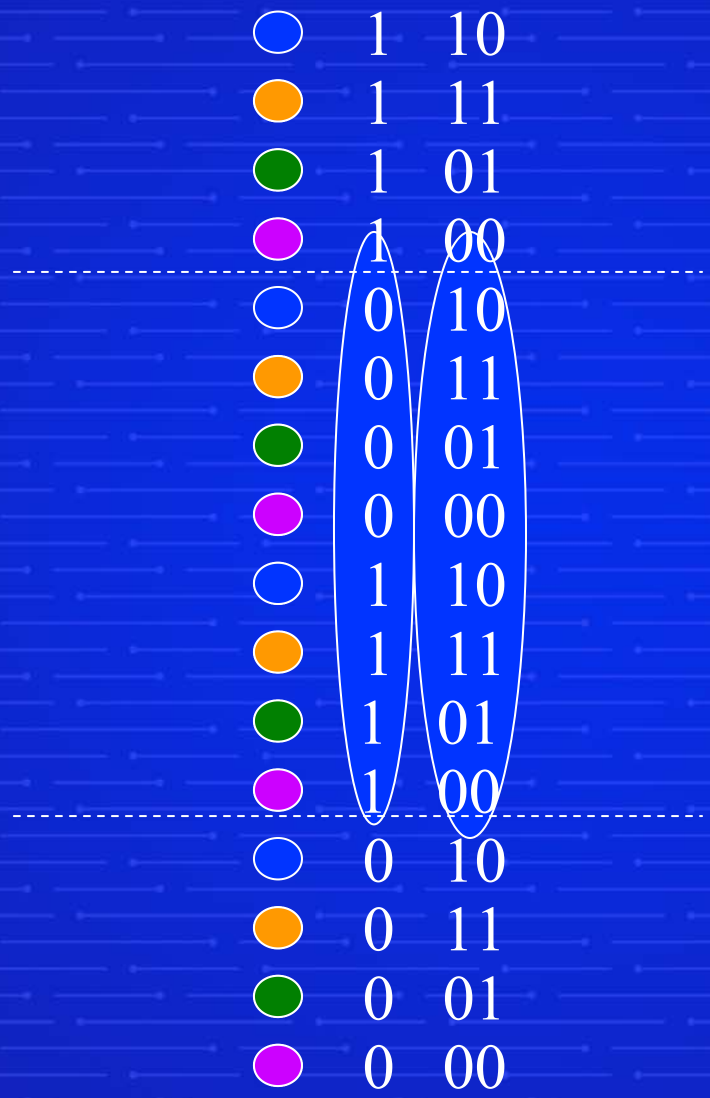


Tomlinson-Harashima Pre-coding

- Independently developed by Tomlinson and Harashima in 1971.
- Uses a Decision Feedback Equalizer at the transmitter instead of the receiver
  - receiver computes DFE coefficients during startup and sends coefficients over to transmitter
  - advantage - allows for block processing and decoding at the receiver.
  - advantage - reduces complexity of receiver analog front end.
  - drawback - increases complexity of transmitter.



Extended Lattice Mapping



Extended lattice preserves the properties of the RS-LDPC code…

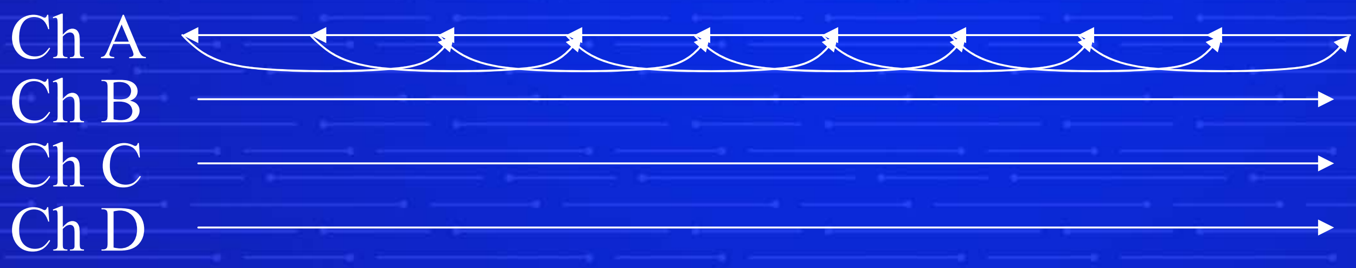
PCS Encoding

- Data words transmitted as is in each block of 256 4D symbols
- Control block of 187 bits:

5 Start packet delimiters	5 End packet Delimiters + TxER encoding	DFE Update Valid	DFE Coefficient Update	CRC
40 bits	50 bits	1 bit	64 bits	32 bits

Startup

- Initial startup using 2-level transmission
  - Corresponds to +/- 4 level.
  - Recover timing and adaptive filter coefficients
  - Establish polarity correction, pair swap
  - Establish 256-symbol block boundaries
  - Exchange initial DFE coefficients
  - Switch to Block coded transmission.



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Concluding Remarks

- Presented outline of a 4D-PAM8 proposal
  - Uses RS-LDPC code and belief propagation decoder to achieve waterfall reduction of BER as a function of SNR.
    - Expect waterfall reduction of BER to continue until ~1E-20 BER limit...
  - Double the noise immunity and coding gain of existing 4D TCM based proposals
  - Tomlinson-Harashima pre-coding to eliminate DFE error propagation
  - Uses CRC protected control blocks to transmit delimiters.
  - Allows for block processing to reduce complexity of receiver.

- Allows for 100m worst-case, extended CAT-6 operation…