Brief overview of 10GbE interfaces

Eric Lynskey

10Gb/s PHY for EPON Study Group Meeting

May 24 – 25, 2006 Austin, TX

UNIVERSITY of NEW HAMPSHIRE
INTEROPERABILITY LABORATORY

Purpose

- Quickly overview the 10 Gigabit interfaces defined in IEEE 802.3ae-2002.
- Start people thinking about what interfaces may be used and possible modifications that may be necessary

10 Gigabit clauses

- MAC defined in Clause 4
- Management is defined in Clause 45
- RS/XGMII defined in Clause 46
- XAUI defined in Clause 47
- 8B/10B PCS defined in Clause 48
- 64B/66B PCS defined in Clause 49
- XSBI defined in Clause 51

Clause 4 MAC

- 10 Gigabit MAC is full duplex only
- ifsStretchRatio is used to increase idle between frames to adapt to different rates
- All other MAC functionality is the same as for 1 Gigabit systems

Clause 45 Management

- All 10 Gigabit management is contained within Clause 45
  - (currently being amended by 10GBASE-T, LRM, and Backplane Ethernet)

Clause 46 RS and XGMII

- XGMII uses a 32-bit clocked data bus with 4 logical lanes and one control bit for each
- RS adds preamble and SFD (always 8 bytes)
- Deficit Idle Count can reduce minimum IPG to align start to lane 0
- Link fault signaling will transmit prevent frames from being sent while fault condition exists
- Fault conditions last for 128 columns
- Possibility exists to add other sequence ordered sets

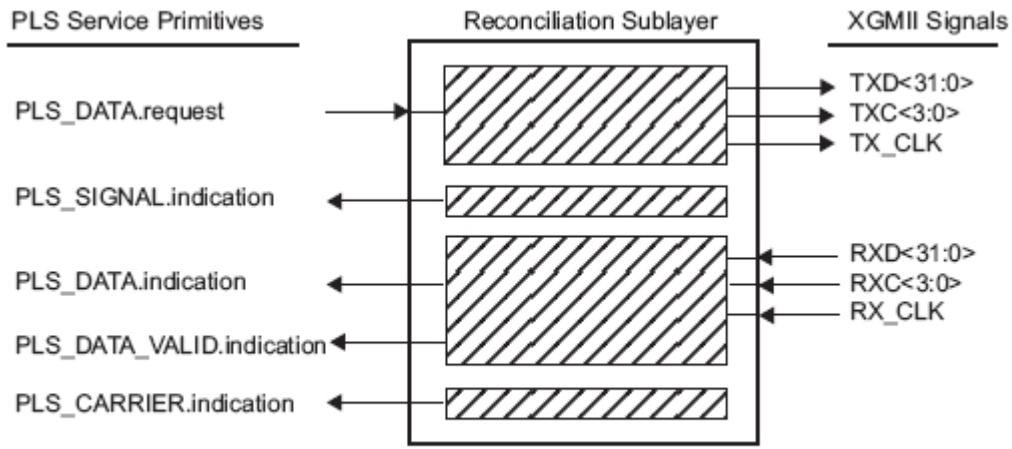

Figure 46–2—Reconciliation Sublayer (RS) inputs and outputs

Clause 47 XAUI

- XAUI is used to extend the XGMII up to 50cm
- Defines electrical characteristics and channel
- Uses Clause 48 PCS at both ends (PHY XGXS and DTE XGXS)
- Common interface for 10Gb pluggable modules

Clause 51 XSBI

- 16-bit interface connecting serial PCS to PMA/PMD
- PCS adapts between 66-bit and 16-bit interface

Clause 48 PCS

- Based off of Clause 36
- 4 lanes of 8B/10B
- Each lane is 3.125 Gbd
- “Random A/K/R” idle between frames, but there are several explicit rules
- On receive side, need both comma synchronization and then lane alignment (currently unbounded)

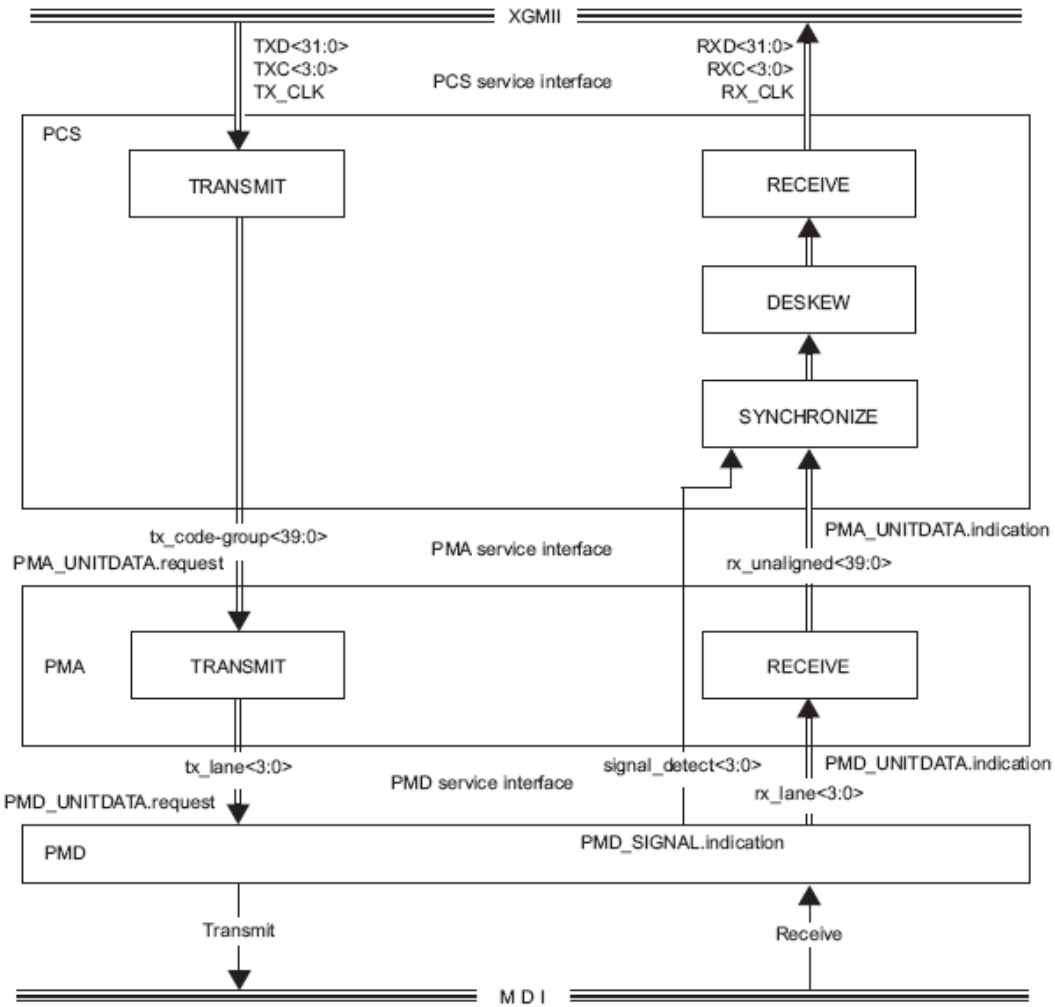

Figure 48–2—Functional block diagram

Clause 49 PCS

- Serial, using 64B/66B at 10.3125 GBd
- 64 bits of scrambled data and 2 bits of header information
- Receiver synchronizes to header bits (unbounded time) and then descrambles
- Built in BER monitor that disables receiver if certain error rate is met
- Fairly strict TX and RX state diagrams

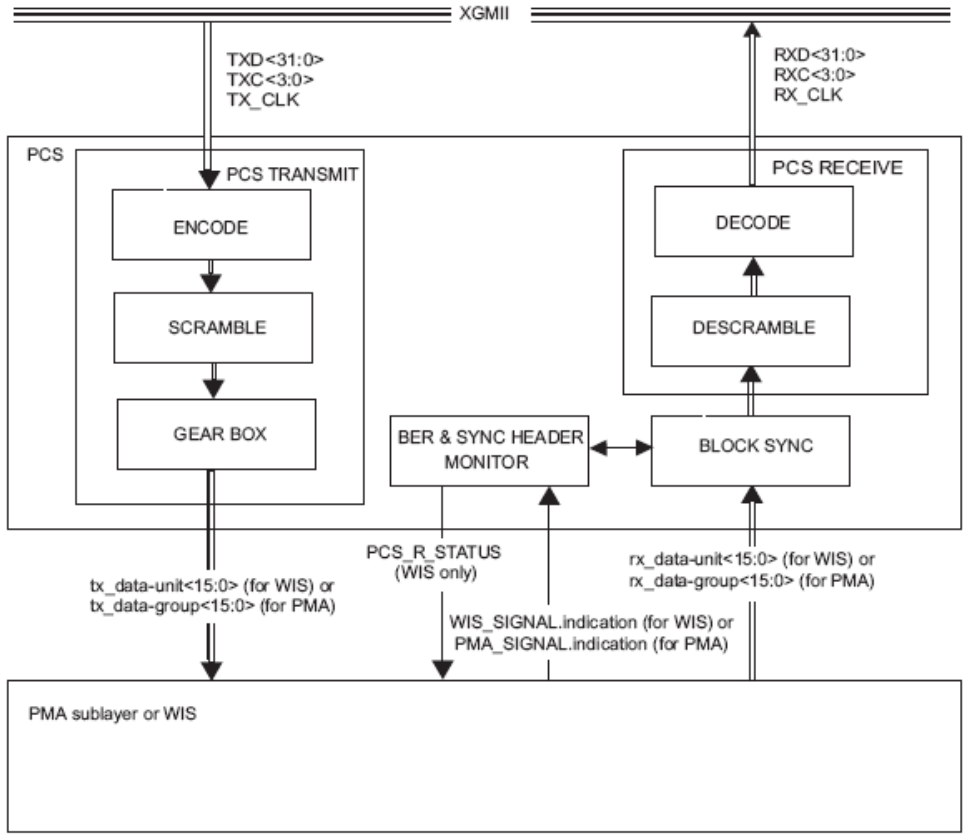

Figure 49–4—Functional block diagram

What needs to be chosen

- We need to work with MAC
  - Do we need to change anything here?
- We need to work around RS/XGMII
  - Look at possible problems with fault signaling and unidirectional behavior
- We need to choose a PCS layer
  - Clause 48, 49, something new
  - Possible minor modifications to existing PCS
  - Look at FEC options (likely will be different than EPON)
- We need to start discussion on reflector

Where to find more information

- http://www.ieee802.org/3/ae/index.html
- Section 4 of IEEE 802.3-2005