Multi-Gigabit Interfaces for Communications/Datacomm

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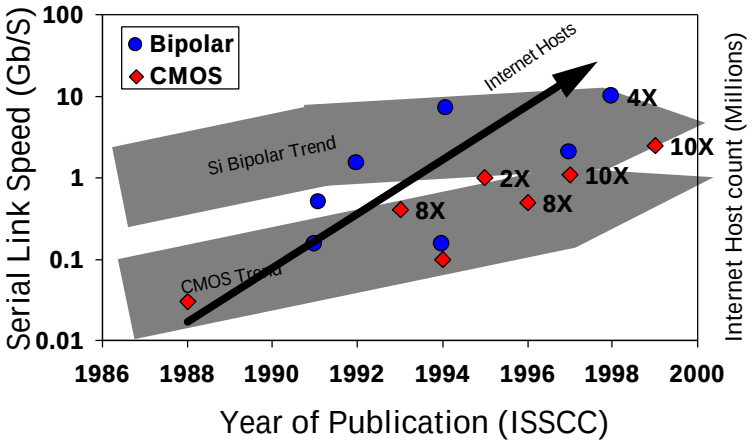
Outline

- Silicon trends
- 10Gb/s options
- Physical component infrastructure
- Coding
- Jitter
- Conclusions

Silicon trends in data links



After R. Walker "Clock and Data Recovery for Serial Digital Comm", BCTM98

General silicon trend

- Current Bipolar technology can handle data rates in excess of 10Gb/s
  - Oversampling can push this even higher
  - Rates will continue to increase with SiGe process development
  - Electronics is challenging, but not the gating item at 10Gb/s
- CMOS is progressing at approximately Moore's Law pace
  - High interleaving rates may adversely effect jitter performance
- Electronics are not keeping pace with bandwidth demand
  - Aggregation of multiple serial channels are going to be necessary for backplanes, servers, etc

10 x ~1Gb/s channel aggregate link

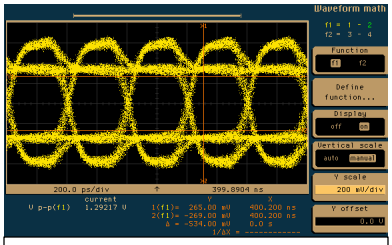
- 10 channels at ~1Gb/s/channel
  - Technology and specs (1000BASE-X) available today for electronics
  - May allow CMOS implementation
  - Can be used over backplane using FR4 and standard connectors
  - Parallel fiber offers long distance extension

4 x ~2.5Gb/s aggregate link

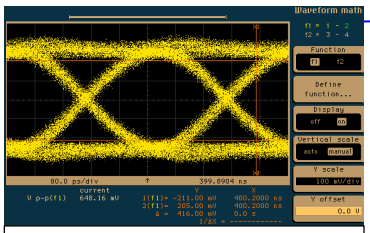
- 2.5 Gb/s links available today
  - Bipolar and GaAs in production
  - May be within CMOS reach in future
- Backplanes with FR4 and low cost connectors may be implemented at these rates
- Copper cable distances of >15 meters are reasonable
- Multiple market segments at this rate will accelerate development and lower cost
  - Backplanes, OC48, Fiber Channel, Server links

Copper cable operating at 2.5 GBd

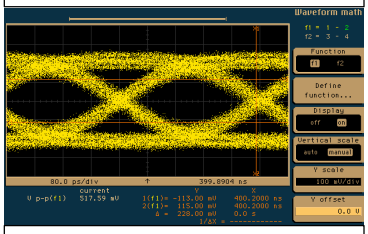
Si Bipolar process (HP25)



No cable (eye only) 2^7-1 PRBS



10m uneq'zed cable



20m eq'zed cable

- Signals are PRBS (2^7 -1) from 2.5 GBd SerDes which includes pre-emphasis output.
- Two different lengths of BERG MetaGig™ cable 10m (unequalized cable) and 20m (equalized cable)
- MetaGig is shielded quad cable with HSSDC-style connectorization.

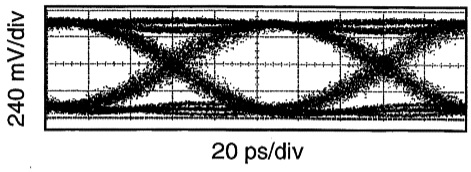
1x ~10Gb/s serial link

- Electronics may not be gating item at 10Gb/s
  - SONET OC192 links working today
  - SiGe will extend range of Bipolar links
  - BUT media capability will be challenged
    - Low cost optics available?
    - Copper cables, PCB performance limitations will constrain applications and reduce volume
    - Jitter performance in optical links?

10 Gb/s SERDES performance

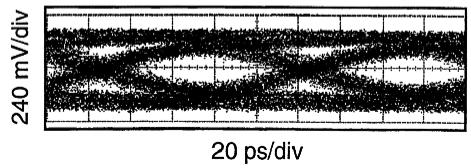
Si Bipolar process (HP25)

Eye Diagrams



Eye at package Pin

- 3ps (RMS) / 18ps (p-p)
- systematic jitter < 3ps (peak)



Eye after 21' of 0.19" coax

- BER < 10^{-14}

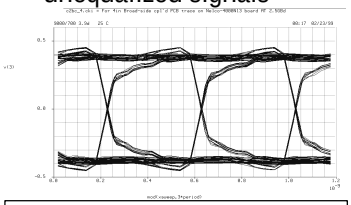
After R. Walker et al, "A 10Gb/s Si-Bipolar TX/RX chipset for Computer Data Transmission", ISSCC 98

Physical component infrastructure

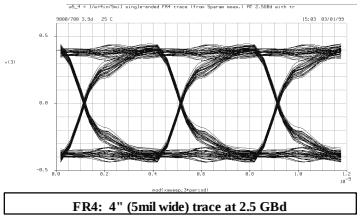
- PBC, connectors, and cables need to be examined closely at these higher rates
- Jitter budgets will be affected by PCB lengths, connectors, etc
- Distance requirements need to be defined
  - PCB to PCB distance for backplane
  - PCB to cable connector distance
  - Minimum required cable length = ?? m
- Implications at 2.5 Gb/s vs. 10 Gb/s

2.5 GBd PCB performance

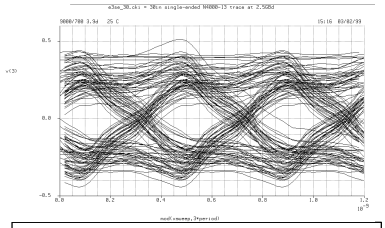
- Both FR4 and N4000-13 show > 24 inch performance with unequalized signals



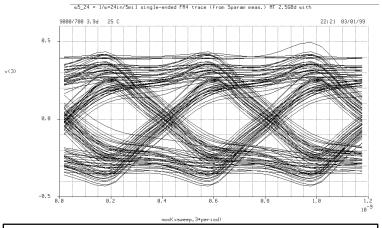
N4000-13: 4in (5mil) trace at 2.5 GBd



FR4: 4" (5mil wide) trace at 2.5 GBd



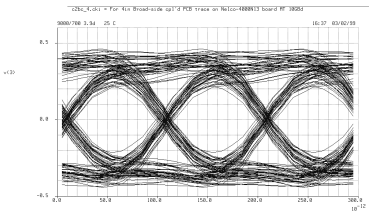
N4000-13: 30in with input=2.5GBd



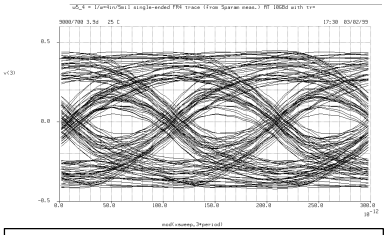
FR4: 24in, 2.5GBd, input tr=50ps

10 GBd PCB performance

- FR4 limited to ~4 inches (unequalized signals)
- N4000-13 significantly improves performance
  - Tx pre-emphasis could improve eye margin



N4000-13: 4" (5mil wide) trace at 10 GBd



FR4: 4" (5mil) trace at 10 GBd

Coding options

- 8b/10b code requires 25% bandwidth overhead
  - 2.5Gb/s --> 3.125Gbd
  - 10Gb/s --> 12.5Gbd
    - Silicon can accommodate rate increase
    - PCB, connector performance will degrade slightly
- 16b/18b codes, others?
  - May affect jitter budgets due to run lengths, balance specifics, etc.
  - Any candidate code needs to be examined ASAP

Scaled optical jitter budget requirements

- SERDES scaled transmitter requirements (@ TP1):
  - 2.5 Gbd extrapolation: RJ = 56ps, DJ = 40ps, **TJ = 96ps**
  - 10 Gbd extrapolation: RJ = 14ps, DJ = 10ps, **TJ = 24ps**
- Typical measured data:
  - 2.5Gbd: RJ ~ 84ps , DJ ~ 20ps, **Total ~ 104ps**
    - including PCB trace
  - 10Gbd: RJ ~ 42ps , DJ ~ 10ps, **Total = 52ps**

Jitter requirements

- All elements of a design need to be considered in link budget
  - PCB material, connector loss greatly increased
- 2.5 Gb/s designs appear to have adequate jitter performance
  - link budget modifications possible?
  - SERDES may be built into optical module?
- 10 Gb/s Si Bipolar SERDES designs will not meet current scaled optical link budget restrictions without modifications
  - Retiming must be done inside optical module
  - SiGe may be needed if optical jitter budget cannot be modified
  - Jitter budget too restrictive?

Conclusion

- 10x 1.0 Gb/s aggregate channel is quickest, lowest cost silicon solution
  - Requires parallel fiber for longer distance
- 4x 2.5 Gb/s aggregate channel is reasonable today for backplane, cable, or optical applications
- 10Gb/s serial electrical performance has been shown for >1 year, but may have application issues
  - Not suitable for backplanes with FR4
  - Short cable lengths possible (1 m - 10m range)
  - Optical jitter budget may demand SiGe, as well as packaging improvements