Application of SiGe HBT's to Datacom and Wireless

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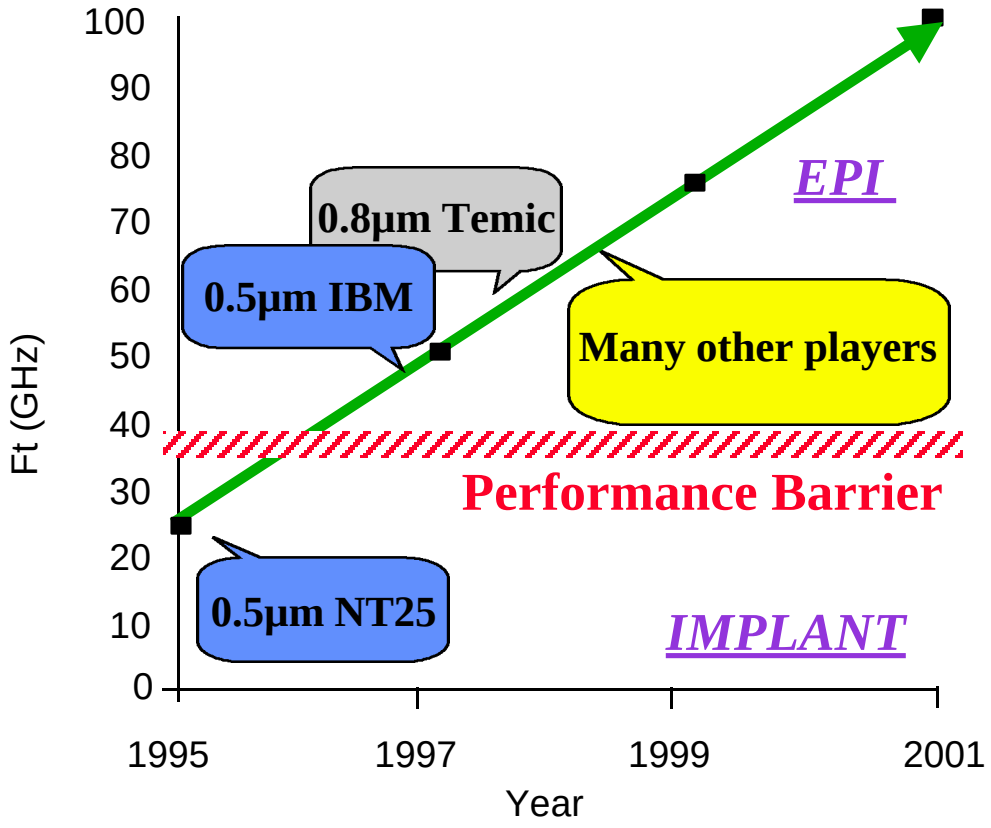
Agenda

- Introduction
  - silicon bipolar roadmap
  - technology competition
- SiGe Myths and Truths
  - dispelling some performance myths
  - product directions
- Components
  - available and needs
- Circuits
  - datacom and wireless examples
- Summary

Introduction

Silicon Bipolar Roadmap

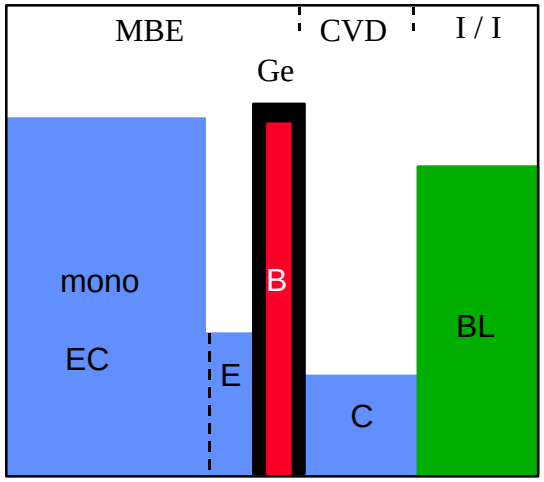


- 25+GHz technology has been available for years
- base layer epi created a significant improvement in performance
- some design rule leveling provided by epi design
- IBM and Temic have pioneered the effort
- many other players have joined the race

Epi-base transistors are becoming the next stop on the silicon bipolar roadmap!

SiGe Myths and Truths

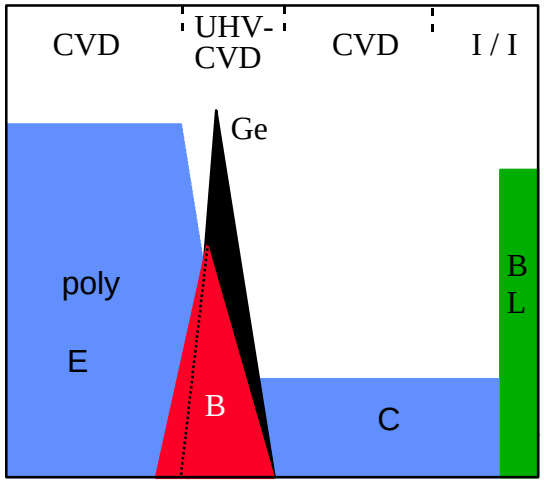
Not all Transistors are created equal



> 100GHz record Ft!

Temic / Daimler Benz (original)

- replicates GaAs HBT's
- 'true' heterostructure
- attempts higher base doping
- lower Rb, NF & higher Fmax
- some design rule levelling (Rb degrade?)
- *discrete to low integration*



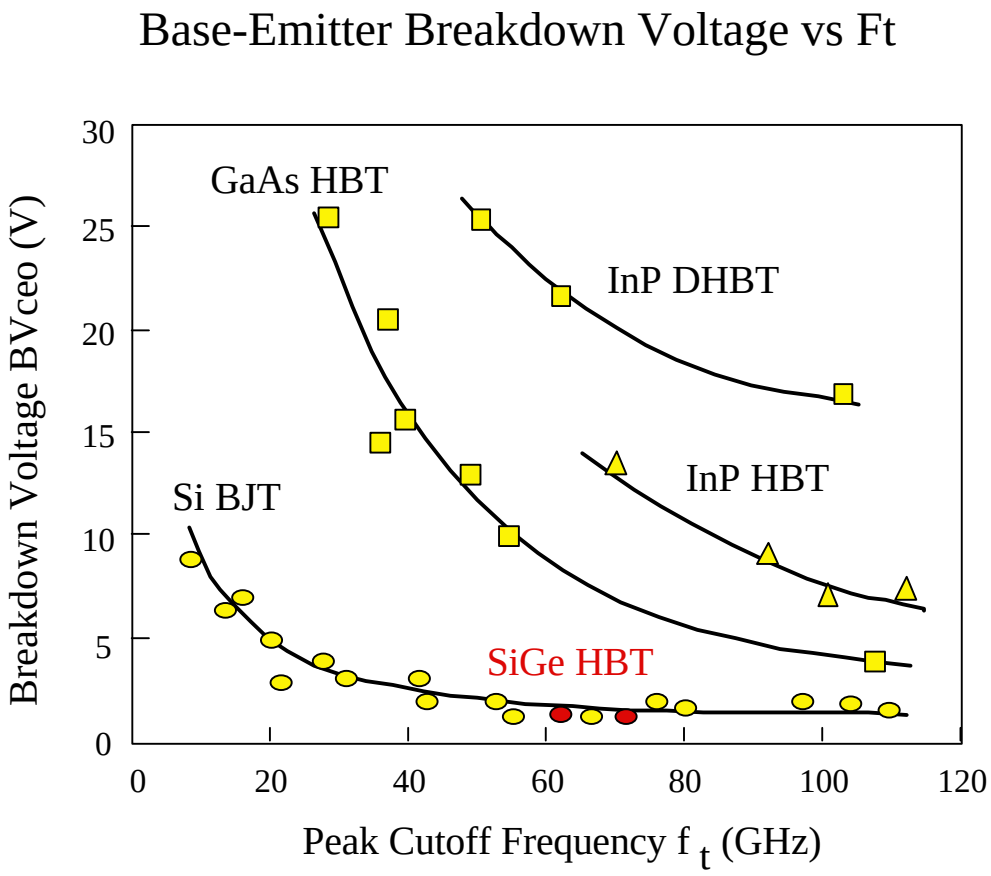
> 100GHz record Ft!

IBM

- replicates poly emitter homojunction
- 'pseudo' heterostructure
- moderate valence-band offset
- some improvement in base doping
- compatible ULSI CMOS (Rb improve?)
- *moderate to high-level integration*

SiGe Myths and Truths

Breakdown voltage is a key operating parameter



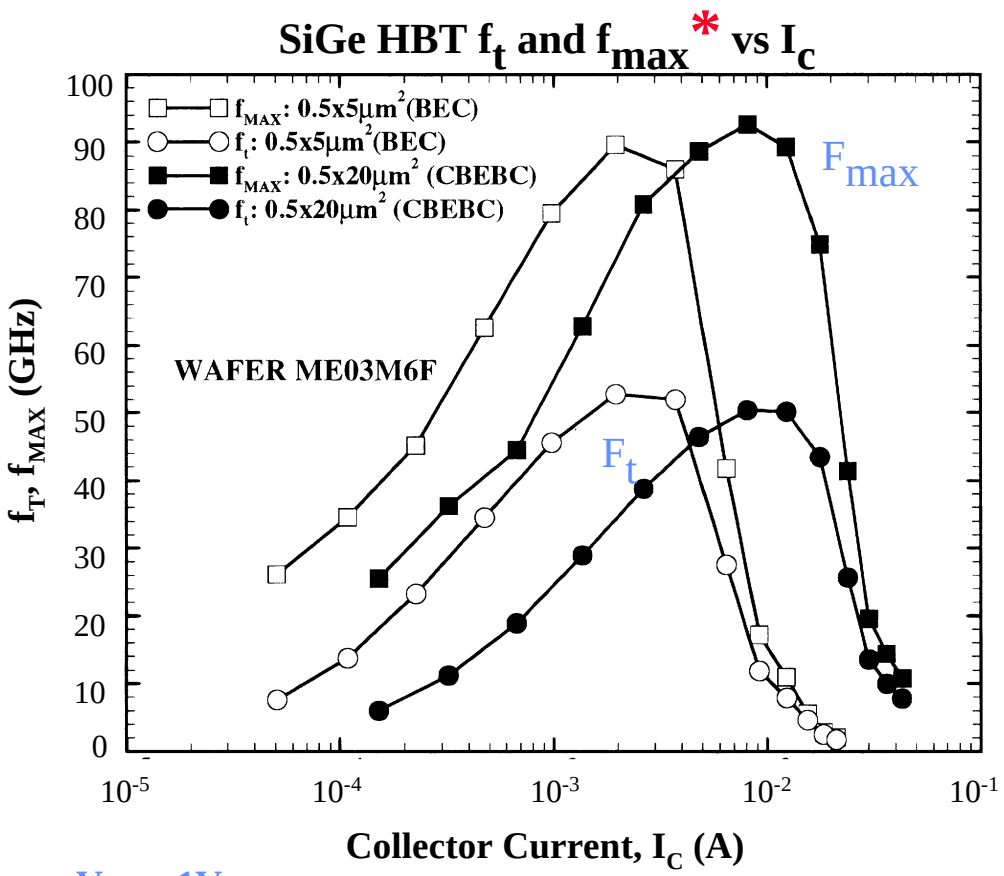
BVCEo vs Peak Ft courtesy of TRW

- materials systems define many key characteristics
- BVceo is considerably lower for silicon
- > 100GHz performance demonstrated @ <2V Bvceo
- low-voltage benefit for low-power dissipation
- > 5V still required for long haul opto components (metro?)
- 3.3 V RF terminals require >6 V BVceo for antenna matching (VSWR)

Manufacturers have 50 & 30GHz SiGe devices.

Components

Transistors



* Fmax obtained from U(f); unilateral power gain

Measured Results

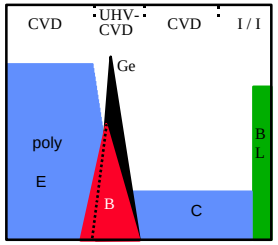
- standard device (f_T / f_{max} are 50 / ***90*** GHz)
- no degradation of f_T and f_{max} for very small devices
- no degradation of f_{max} for long devices with proper number of base contacts

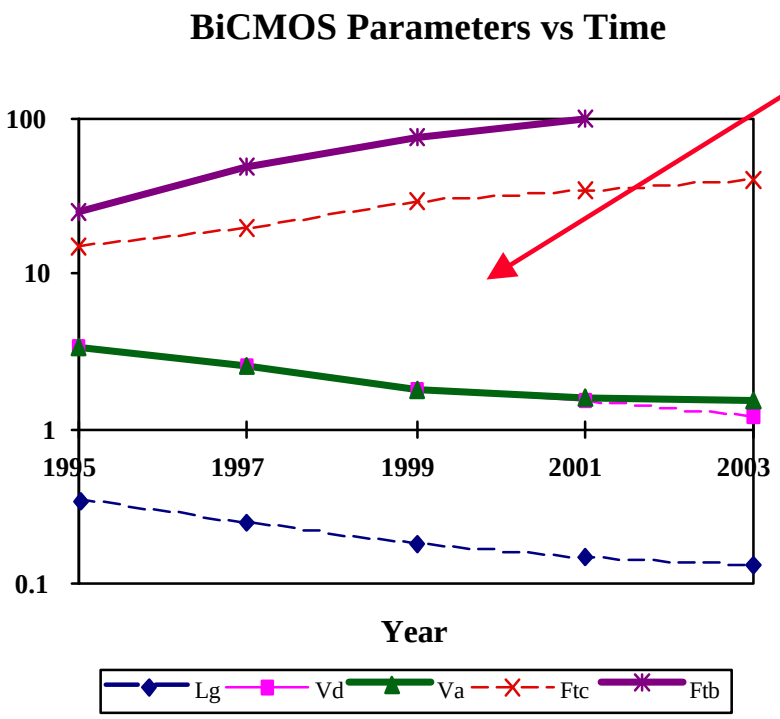
Simulation Accuracy

- geometry scalable device characteristics
- per die extracted device characteristics model very accurately
- optimized thermal model parameters included

SiGe Myths and Truths

What are the significant advantages offered by SiGe?





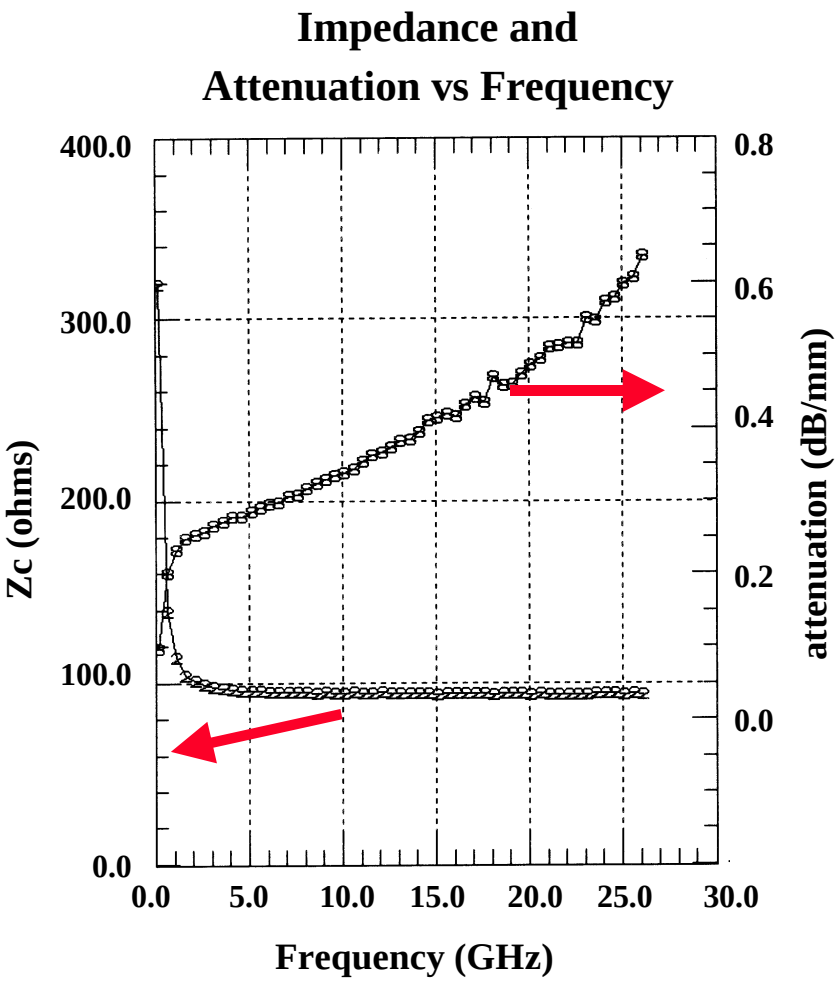
- BiCMOS compatible
- follows Si roadmap
  - obeys CMOS scaling (VDD)
  - utilizes silicon investment
- some performance advantage over GaAs
- wafer cost advantage; 8” vs 4”
- systems-on-a-chip integration
  - reduce interfaces, power and packaging costs
- emerging (and existing) market

Capture some GaAs and homojunction market share!

discontinuity is good, but predictability helps define product thrusts, CR and customer value

Components

Transmission Lines



Measured Results

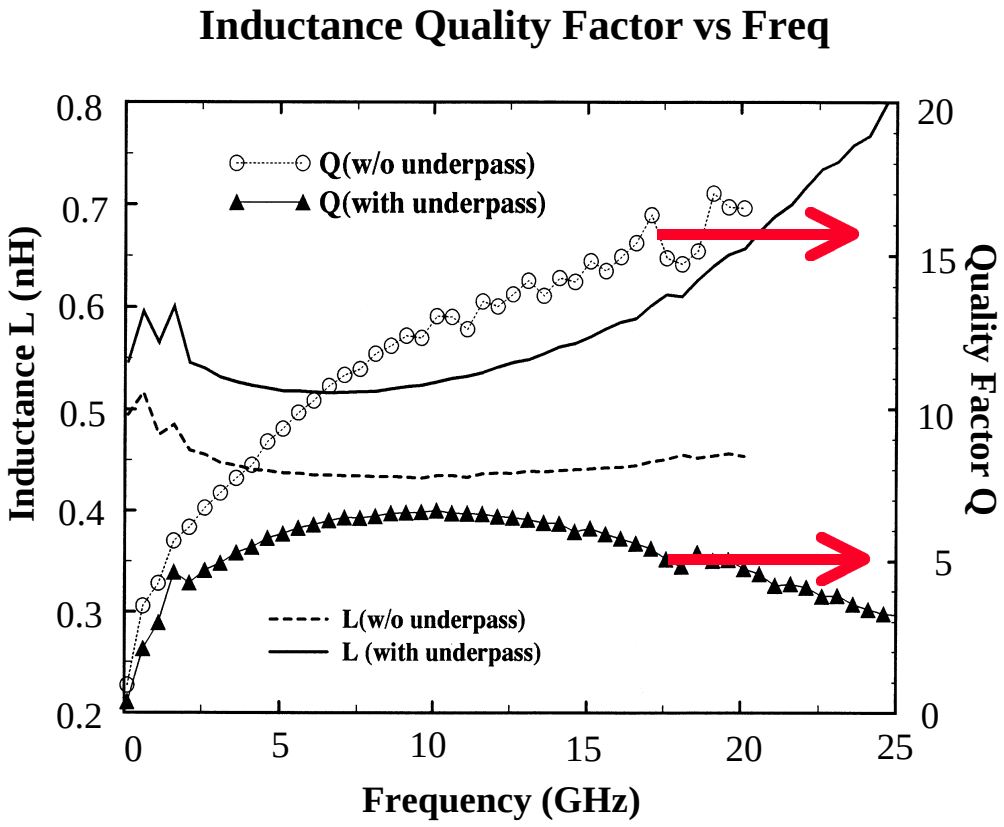
- innovative metal over “special” silicon transmission line
- key to circuits from 2 - 20 GHz
- no dispersion; Zc is constant with frequency to 26GHz
- reasonable 0.3 dB/mm loss
- losses better than for metal3 over metal1 lines and/or metal3 over silicon substrate
- no process change required

Simulation Accuracy

- better than 10%

Components

Spiral Inductors



2.25 Turns, 30 µm Width, 175 X 175 µm^2

Measured Results

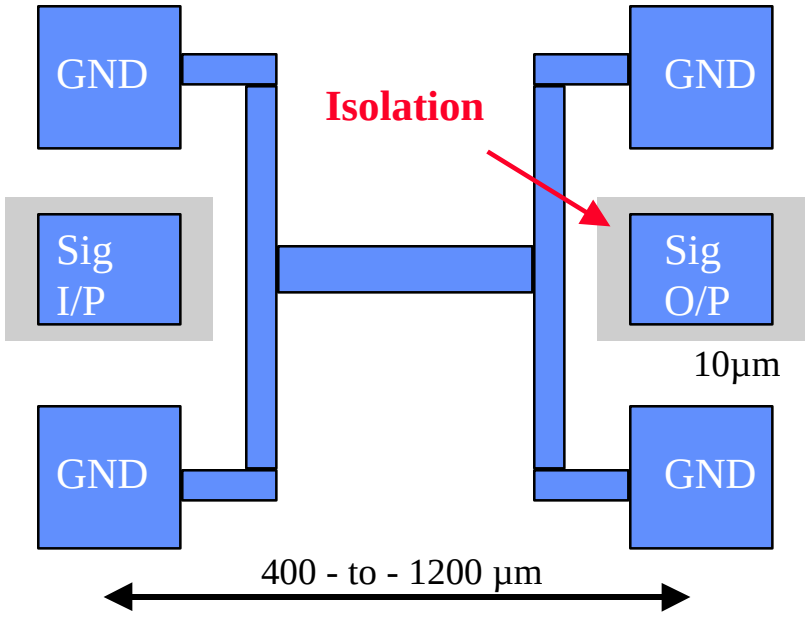
- metal3 spiral inductor (0.45nH @ 10GHz)
- high-current flow (120mA) enabled by metal1 / metal2 underpass
- underpass lowers Quality Factor (12 to 7 @ 10GHz)

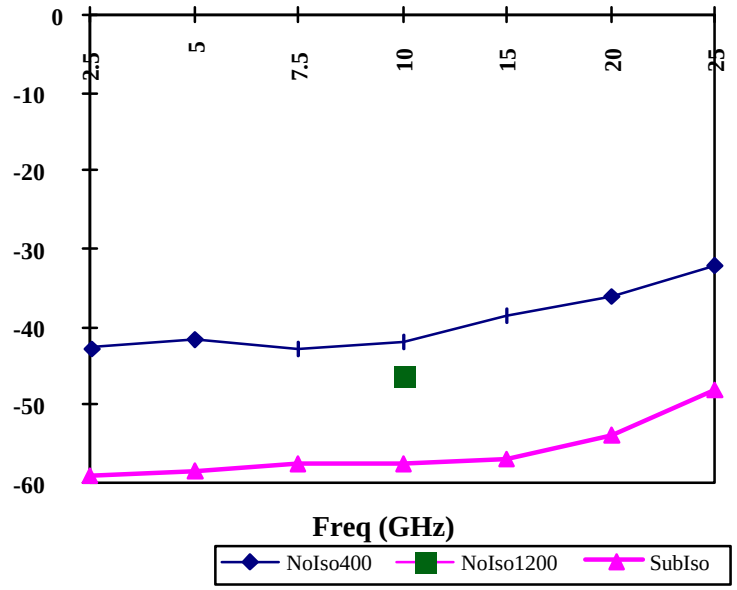
Simulation Accuracy

- special de-embedding structures to determine underpass influence
- better than 5% inductance
  20% loss
- more work needed to accurately model losses

Components

Substrate Isolation





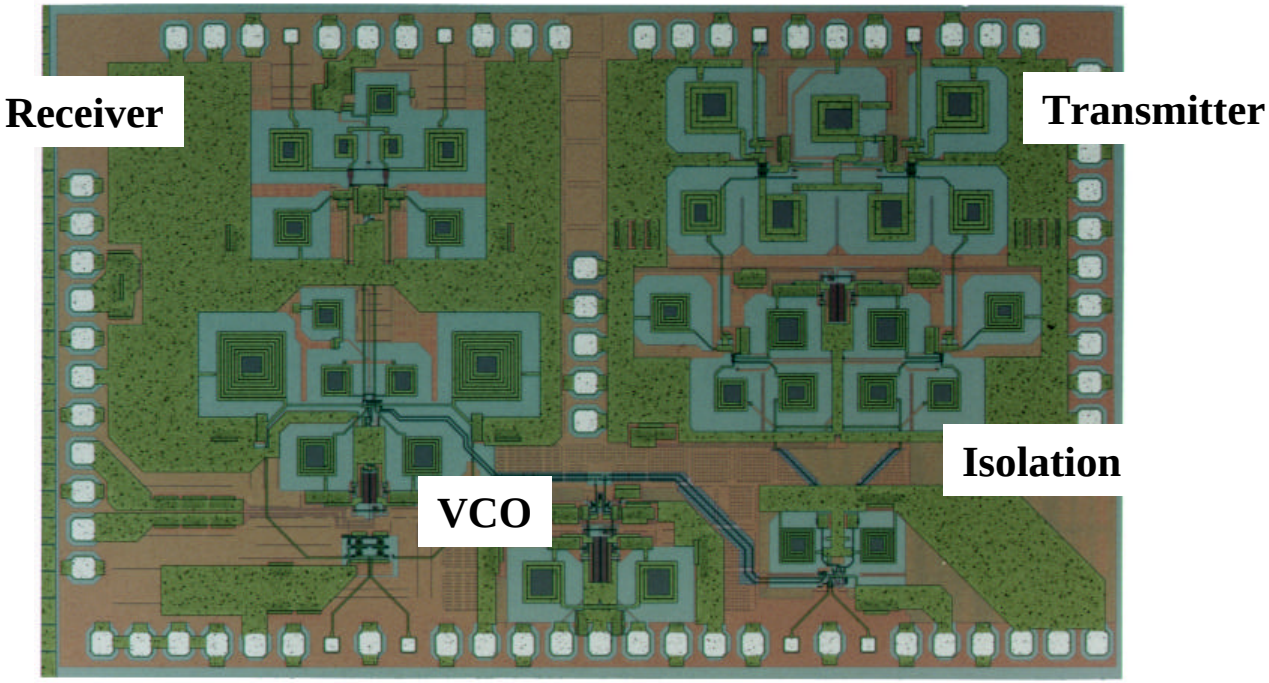
Isolations Structures

- with and without grounded substrate ring (p+)
- separation of 400 -to- 1200µm
- full s-parameter characterization

Results

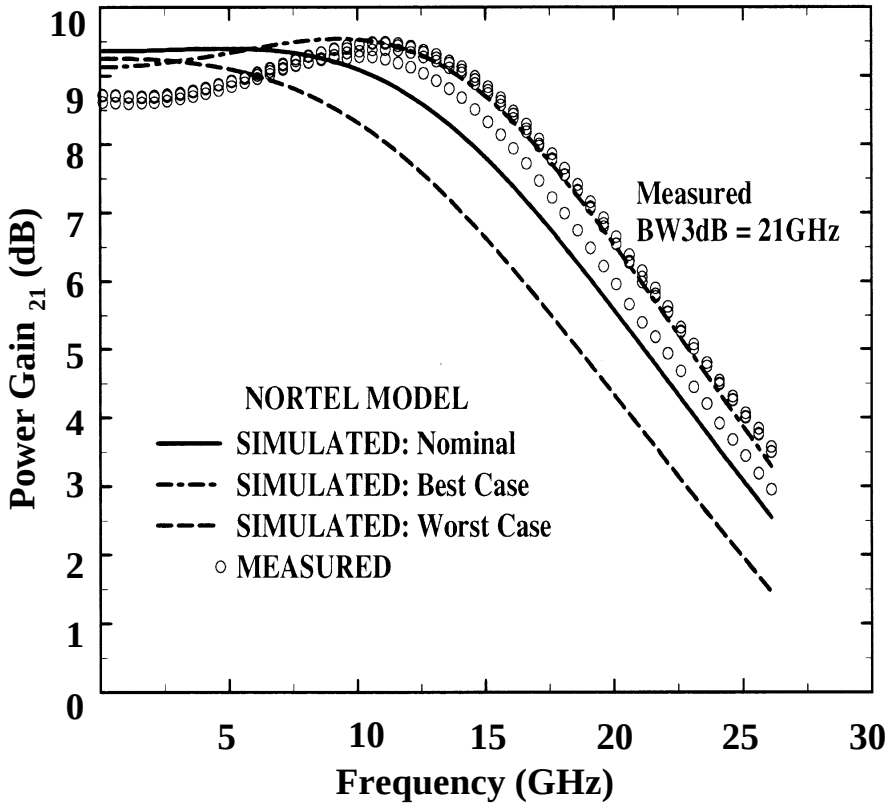
- Isolation yields -57dB @ 10GHz (no distance dependence down to 400µm)
- better than -50dB to 25GHz (outperforms SOI !!)
- full 15dB improvement over non-isolated case

5.2GHz WLAN Radio Transceiver



- Integrated Radio Transceiver using SiGe HBT technology
- Heavily exploits high quality on-chip components (L, varactor, T-line)
- Supports 20MHz bandwidth with on-chip 40dB image rejection
- SSB Noise figure of 5.9dB, IP1=-22dBm and OP1=10dBm
- On-chip VCO with -100dBc/Hz; -128dBc @ 100KHz; 5MHz offsets.
- Draws 125mA in transmit and 45mA in receive mode from 3.5V.

Broadband Darlington Amplifier - transistors



Results / Specifications

- Optimized for;
  - broadband BW3dB=21GHz
  - input match Š20dB@Š5GHz
  - P1dB 12.5dBm@5GHz
  - group delay 8 ps across band
  - NF 5.4dB; 1-to-6GHz

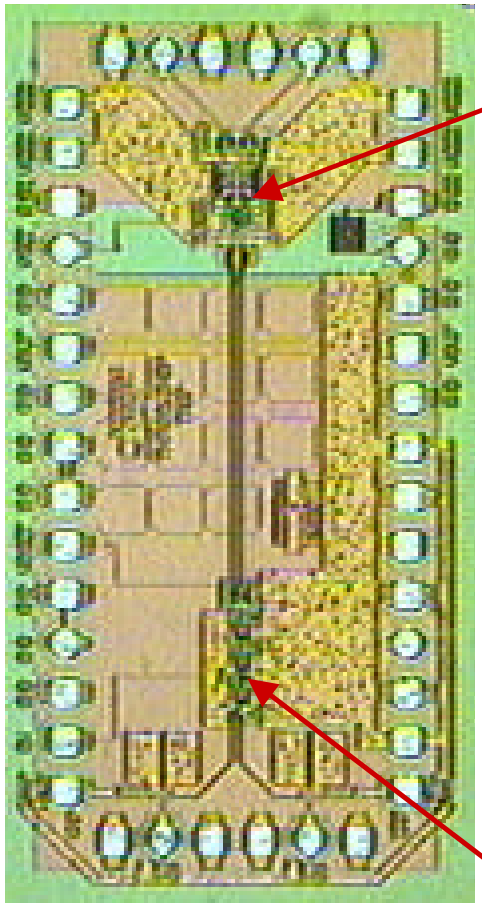
Key Practices

- simultaneous noise & impedance match
- scalable model key to optimize;
  - transistor size
  - optimum bandwidth
  - group delay
- statistical & corner model used
- measured data taken over 3 wafers (lots and lots of die)

Limiting Amplifier - transmission lines (1st level isolation)

Results / Specifications

- **Small Signal Gain > 60 dB**
- **Small Signal BW3dB >15 GHz**
- **Min IP Signal Sensitivity - 3.5 mV**
  @ BER of 10-9 (10^{-23} PRBS)
- **Output Swing (50 ohm) 2.0 V**
- **Saturation IP V @10Gb/s 1.0 mV**
- **Voltage supply 5.0 V**
- **Power Dissipation 0.6 W**
  core = 100mW



Key Practices

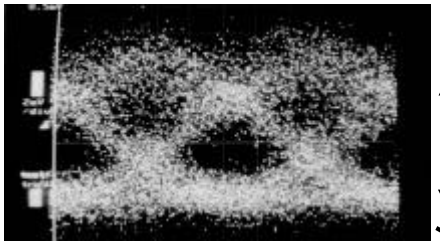
50ž O/P buffer
- **2 volt swing**

Isolation
- **Inductor ground separation**
- **Transmission line decoupling from input to output**
- **On-chip capacitive decoupling**

50ž I/P buffer
- **3 gain stages**

Circuits

Optical receiver application



8 mV

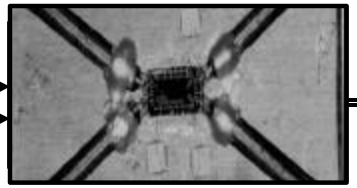
10 Gb/s

MZ

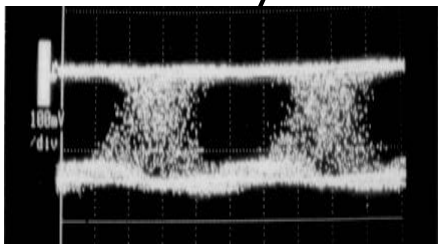
PIN

Tz amplifier

Mounted Lim. Amp.



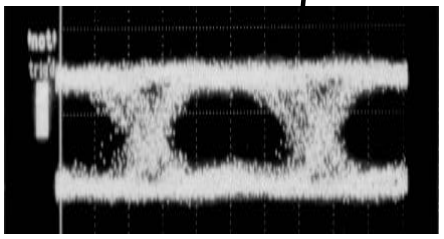
BERT



Slicing level control

Fiber length	Sensitivity BER=10^{-9}
50 km	-19.6 dBm
100 km	-18.5 dBm

All waveforms are at 100 km span BER=10^{-9}



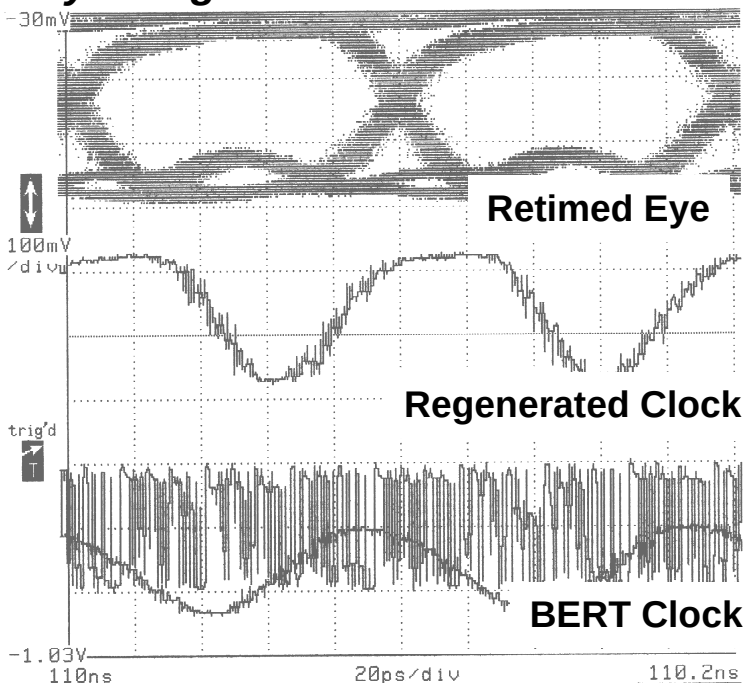
0.5 V

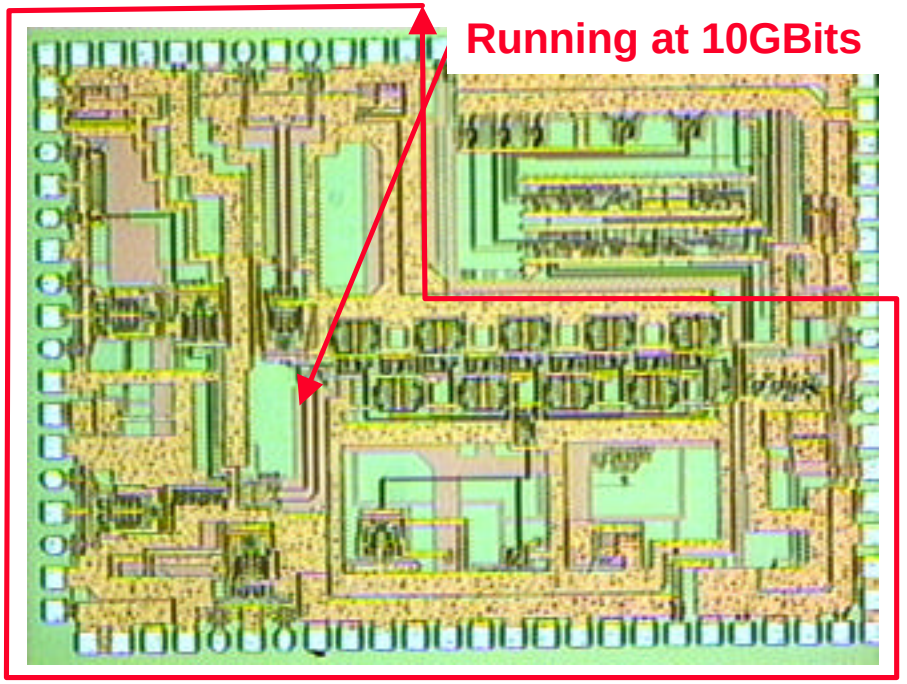
100 ps

Circuits

Highly Integrated Burst Mode Optical Receiver- complexity

Eye Diagram





Results / Specifications

- **1450 transistors; 3mm X 3.5mm**
- **30ps Output Rise/Fall Times**
- **15mV input sensitivity**
- **BER < 10^{-10} at 2^7-1 pattern at 10 GB/s**
- **> 200db signal path gain - STABLE**

Key Practices

- **fully isolated**
- **10 - 20GB/s ECL cell library**
- **analog decision circuit (limiting amp)**
- **Full ESD protection**

SiGe Tests Results Above 10Gb/s

- Limiting amplifier / Decision circuit: 20Gb/s
- 2:1 MUX: 20Gb/s
- 8:1 MUX: 16 Gb/s
- 1:8 Demux: 12.5Gb/s

Other 10Gb/s Circuits

- Transmit LC VCO
- AGC Amplifier
- Clock and Data Recovery

Summary

- **Silicon epi-base technology has extended transistor performance**
  - **now encompassed on everyone's roadmap**
- **Different heterostructure implementations share constraints**
  - **BVceo, lithography, emitter structure**
- **Stiff competition for discrete components**
  - **silicon has materials and wafer cost advantage**
  - **packaging / assembly eliminates some of this advantage**
- **High-levels of integration provides unique product opportunity**
  - **most applicable to > 2.4 - to - 12.5GHz operating frequencies**
- **Understanding of passives critical to success**
  - **inductors, transmisson lines and isolation**
- **Imminent very high-performance datacom and wireless systems-on-a-chip solutions**

SiGe BiCMOS Technology for 10Gb/s Ethernet

PETER SCHVAN, NORTEL NETWORKS

- SiGe technology can support high speed components for 10Gb/s Receiver and Transmitter Ic's.
  - Tz, Limiting, AGC amplifier
  - Integrated PLL based CDR, 1:n Demux, n:1 MUX
  - Low phase noise VCO (sub-ps jitter)
  - Up to 3V laser/modulator driver
- BiCMOS option allows system-on-chip implementation
  - 0.25 (soon 0.18)um CMOS logic/memory can be integrated
  - High cross-talk suppression demonstrated
- Economics of Si technology guaranties commodity like component cost that follows standard cost reduction curve