IEEE 802.3
Higher Speed Study Group

10Gig MII update

Kauai, HI
9-November-1999

Howard Frazier - Cisco Systems

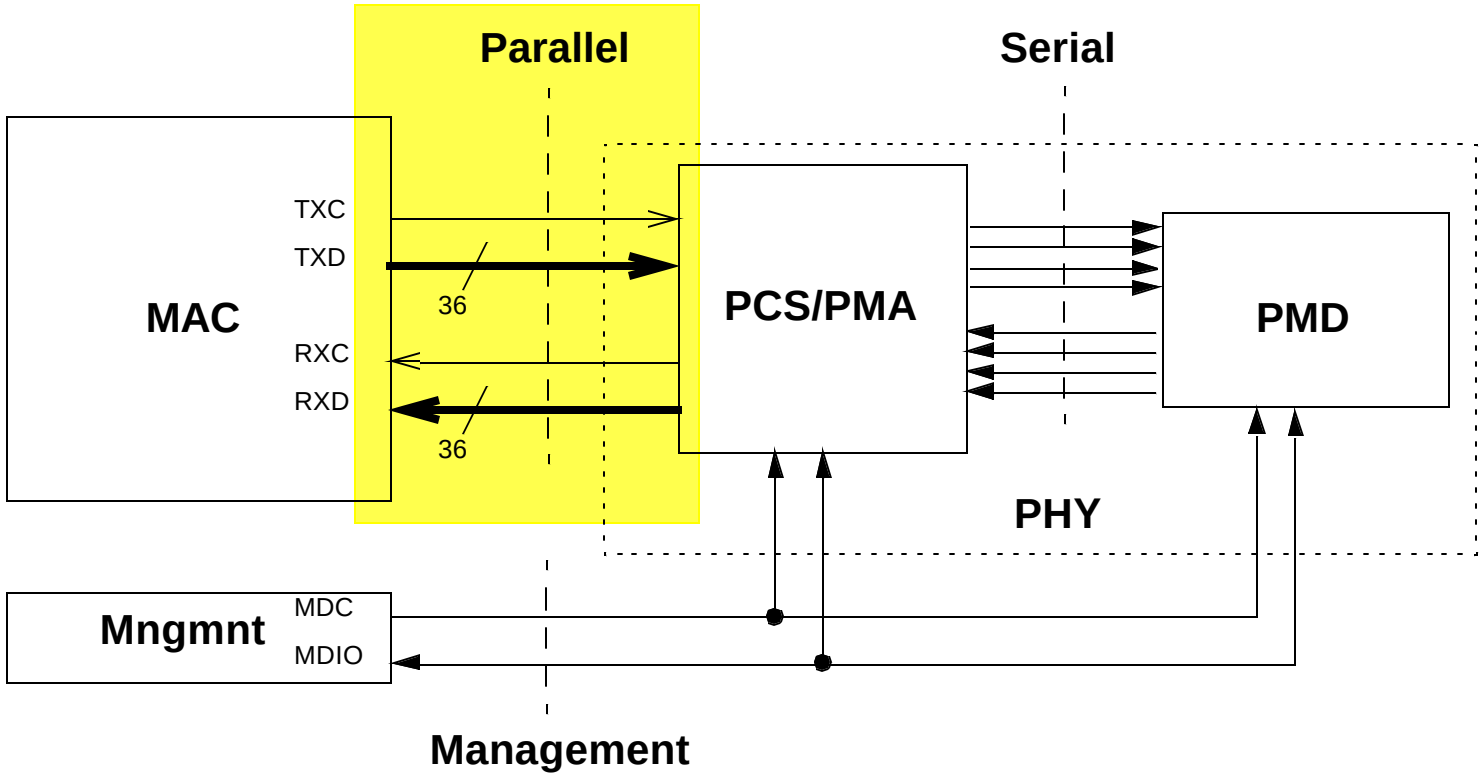
Outline

- Goals and Assumptions
- Interface Locations
- Parallel Interface
- Serial Interface
- Inter-Packet Gap
- Serial Transceiver Support
- Management Interface
- Scaling, Integration, Flexibility
- Summary

Goals and Assumptions

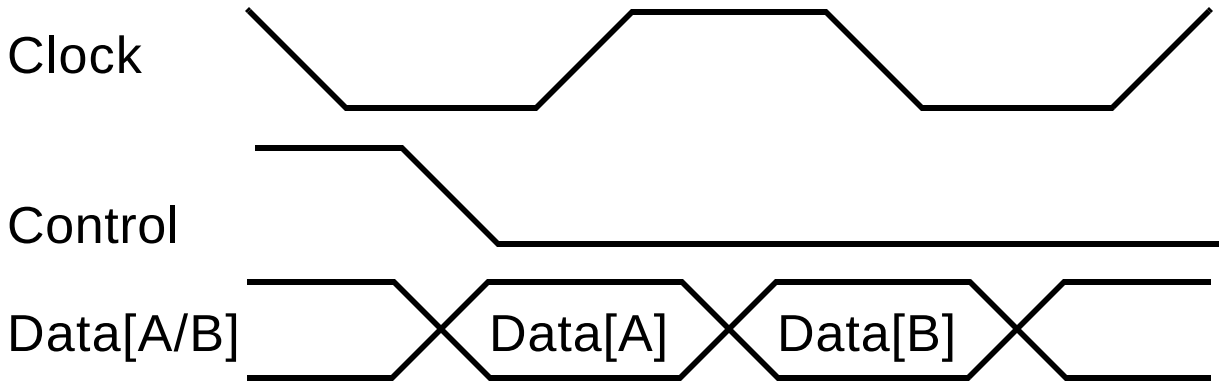
- Allow multiple PHY and PMD variations
- Provide a convenient partition for implementers
- Provide a standard interface between MAC and PHY
- Provide a standard interface between PHY and PMD
  - Potential for use in other applications, e.g. Fibre Channel
- Interfaces must be scalable in speed and width
  - Keep up with technology development
  - Allow implementation flexibility
- PMD components can be arbitrarily complex
  - Low Complexity: Parallel fiber
  - Moderate complexity: CWDM, Serial fiber
  - High complexity: SONET, MAS

Interface Locations



Parallel Interface

- 32 data bits, 4 control bits, one clock, for transmit
- 32 data bits, 4 control bits, one clock, for receive
- Dual Data Rate (DDR) signaling, with data and control driven and sampled on both rising edge and falling edge of clock



- 32 bit data paths are divided into four 8 bit “lanes”, with one control bit for each lane

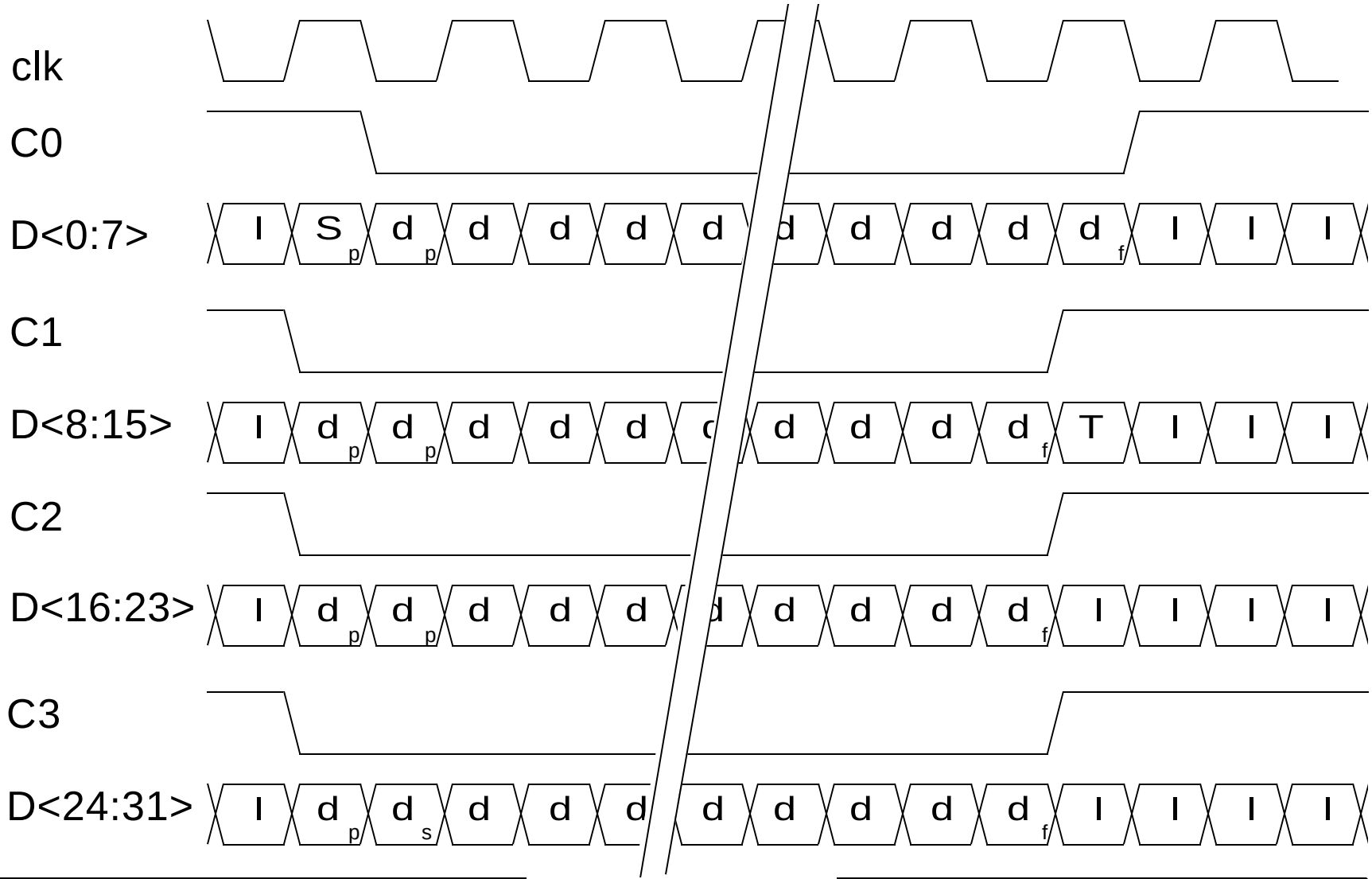
Parallel Interface - Coding

- Use embedded delimiters rather than discrete signals
- Control bit (C) is “1” for delimiter and special characters
- Control bit (C) is “0” for normal data characters
- Delimiter and special character set includes:
  - IDLE, SOP, EOP, ERROR
- Delimiters and special characters are distinguished by the value of the 8 bit data lane when the corresponding control bit is “1”
- Data (d) symbols are striped on lane 1, lane 2, lane 3, lane 0, etc.
  - Frames (packets) may be any number of symbols in length subject to minFrameSize and maxFrameSize

Parallel Interface - Coding

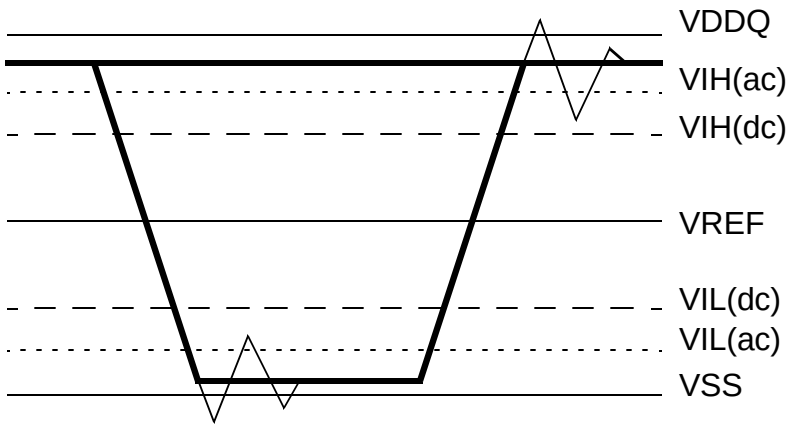
- IDLE (I) is signaled
  - during the Inter-Packet Gap
  - when there is no data to send
- SOP (S) is signaled
  - for one byte duration at the beginning of each packet
  - always on lane 0
- EOP (T) is signaled
  - for one byte duration at the end of each packet
  - may appear on any lane
- ERROR (E) is signaled
  - when an error is detected in the received signal
  - when an error needs to be forced into the transmitted signal

Parallel Interface - Example



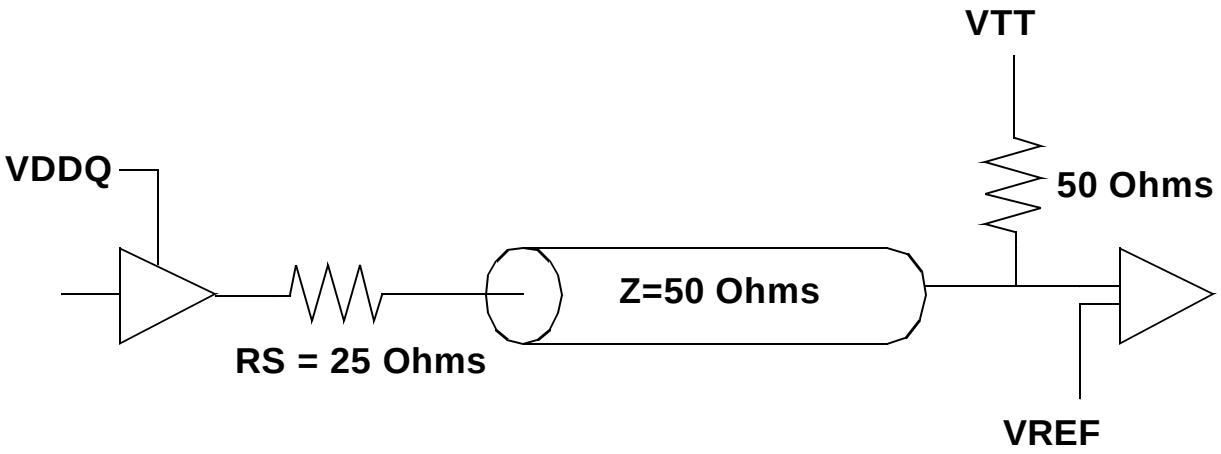
Parallel Interface - Electrical Characteristics

- Use Stub Series Terminated Logic for 2.5 Volts
  - SSTL_2
  - EIA/JEDEC Standard EIA/JESD8-9
  - Class I (8 ma) output buffers

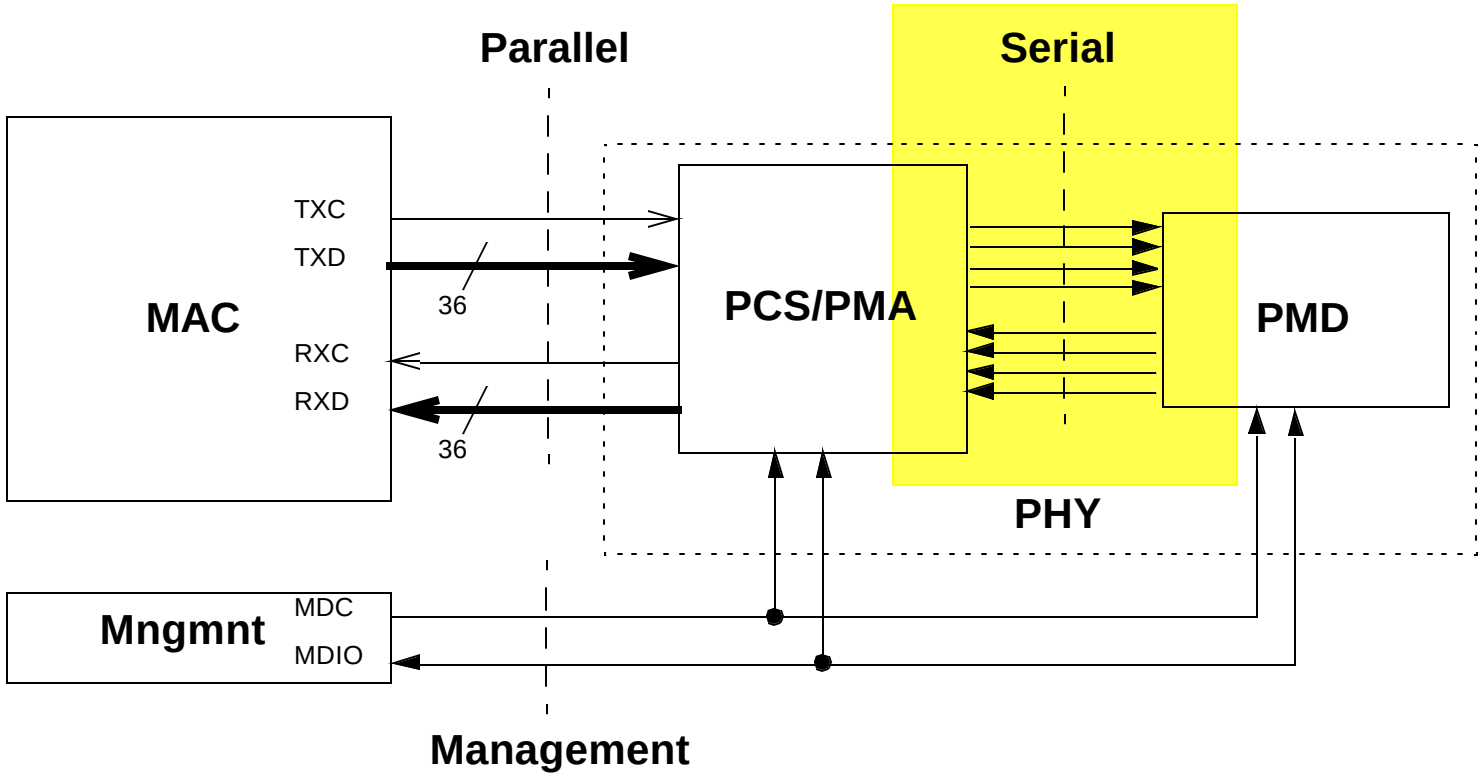


Symbol	Parameter	Min	Typ	Max
VDDQ	Supply Voltage	2.3	2.5	2.7
VREF	Reference Voltage	1.15	1.25	1.35
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04
VIH(dc)	dc input logic high	VREF+0.18		VDDQ+0.3
VIL(dc)	dc input logic low	-0.3		VREF-0.18
VIH((ac)	ac input logic high	VREF+0.35		
VIL(ac)	ac input logic low			VREF-0.35

Parallel Interface - Circuit topology example



Interface Locations



Serial Interface

- 4 x 2.5 Gbps
- Transmit and Receive data signals
- Data and clock signals are:
  - Differential
  - CML “like”
- Control signals provided via MDIO/MDC
  - RX_LOS (signal detect)
  - TX_DISABLE
  - Device ID
  - Other PMD specific control functions

Serial Interface - Coding

- Use 8B/10B NRZ encoding
  - well understood, widely implemented, robust
  - simple to implement in CMOS, BiCMOS, SiGe
  - excellent run length and DC balance characteristics
- Use 3.125 GBaud signaling rate
  - within limits of FR-4 PCBs
  - SerDes within limits of 0.25 micron CMOS
- Directly map and encode bytes from parallel interface
  - Parallel Lane 0 <=> Encode/Decode <=> Serial Lane 0
  - Parallel Lane 1 <=> Encode/Decode <=> Serial Lane 1
  - Parallel Lane 2 <=> Encode/Decode <=> Serial Lane 2
  - Parallel Lane 3 <=> Encode/Decode <=> Serial Lane 3

Serial Interface - Coding

Code Key

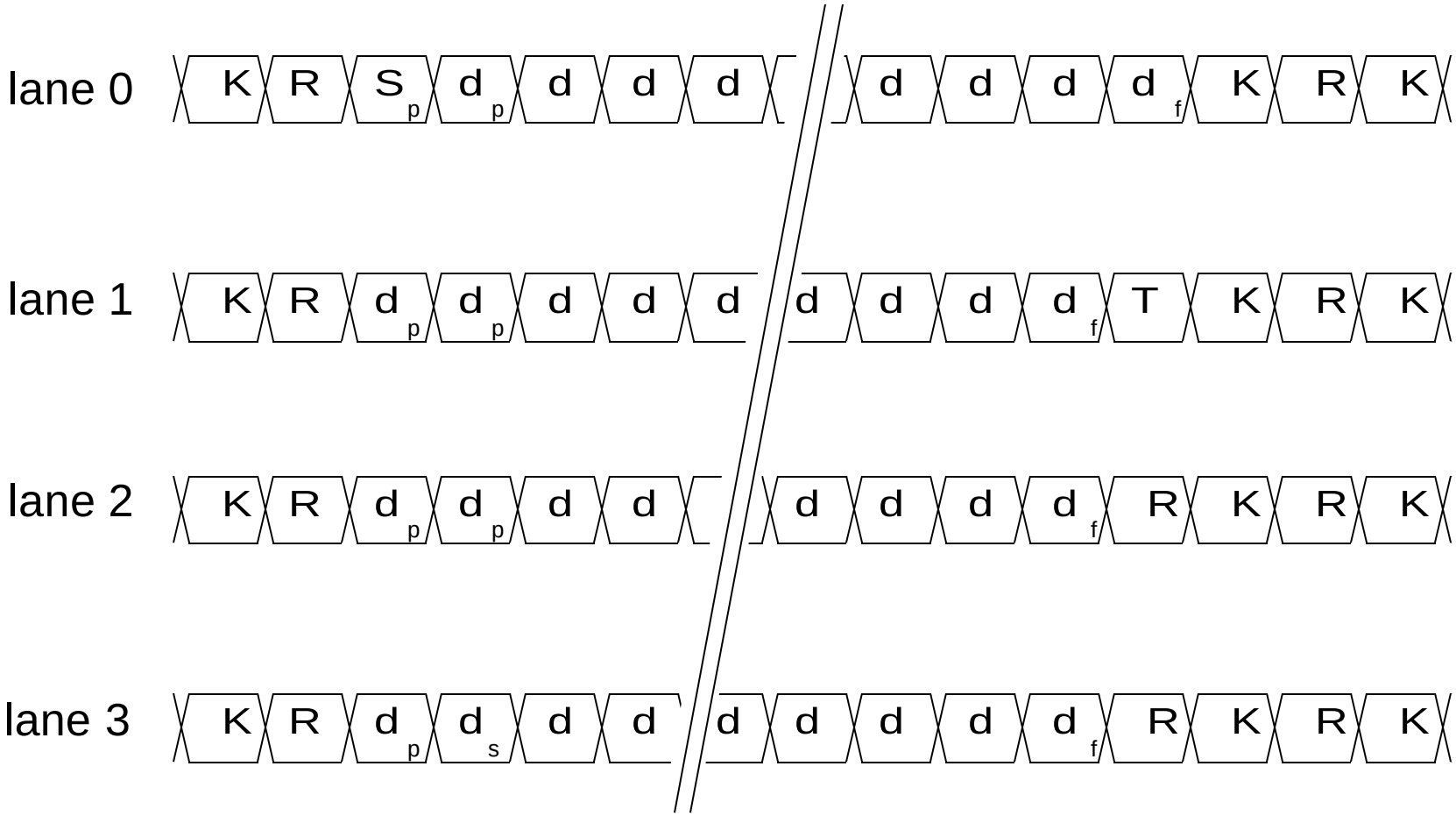
Symbol	8B/10B Code	Description
K	K28.5	Idle/even cycles
R	K28.0	Idle/odd cycles
S	K27.7	Start of Packet
T	K29.7	End of Packet
E	K30.7	Error
d	Dxx.y	Data

- K28.5 contains a comma, used to establish synchronization
- K28.5/K28.0 produces an IDLE with good spectral characteristics

Hamming Distance

	K28.0	K28.5	K27.7	K29.7
K28.0	-	3	4	4
K28.5	3	-	5	3
K27.7	4	5	-	2
K29.7	4	3	2	-

Serial Interface - Example



Inter-Packet Gap

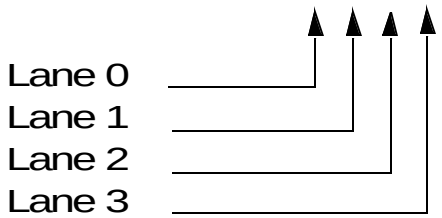
- Assume that clock tolerance compensation is performed in the PCS or MAC, at the decoded data level
  - Eliminates concerns about preserving disparity
  - Eliminates concerns about granularity of Idle insertion/removal
- IPG needs to be longer than the number of bits accumulated during frame reception with worst case clock mismatch
- Assume +/- 100 ppm oscillators
  - Worst case mismatch equals 2.5 bits for 1518 byte Ethernet packet

Inter-Packet Gap

- Minimum Transmit IPG = 12 bytes
  - Transmitters may emit longer IPGs
  - 64 bit implementations may prefer 8 or 16
- Minimum Receive IPG = 4 bytes
  - 64 bit implementations may prefer 0 or 8
- SOP (S) is not included in the IPG, because it replaces the first byte of the Ethernet preamble
- EOP (T) is included in the IPG

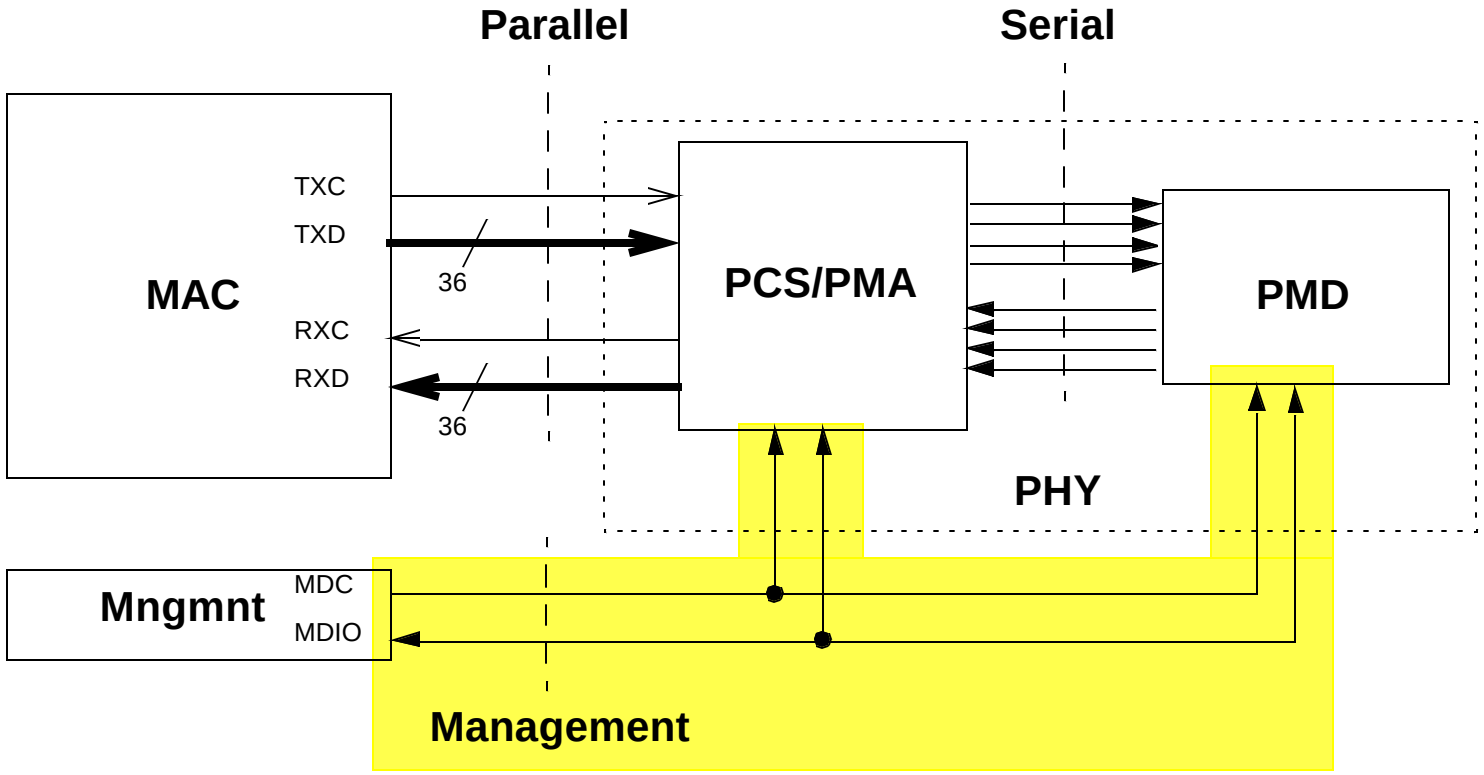
Serial Transceiver Support

- Allow development of serial 12.5 GBaud optical transceivers
  - Multiplex data at the symbol level, not the bit level
  - Must correct running disparity to avoid comma synthesis
- Identify lanes by scanning for KRKRKRKRKRKRKRKR which looks like KKKKRRRRKKKKRRRR in a serial stream



- The Start of Packet symbol (S) can be used to sort out the lanes in the event they get rotated
- Lane identification is not a problem for parallel fiber or CWDM
  - Lane to lane connections are controlled by connector keys or “color coding”

Interface Locations



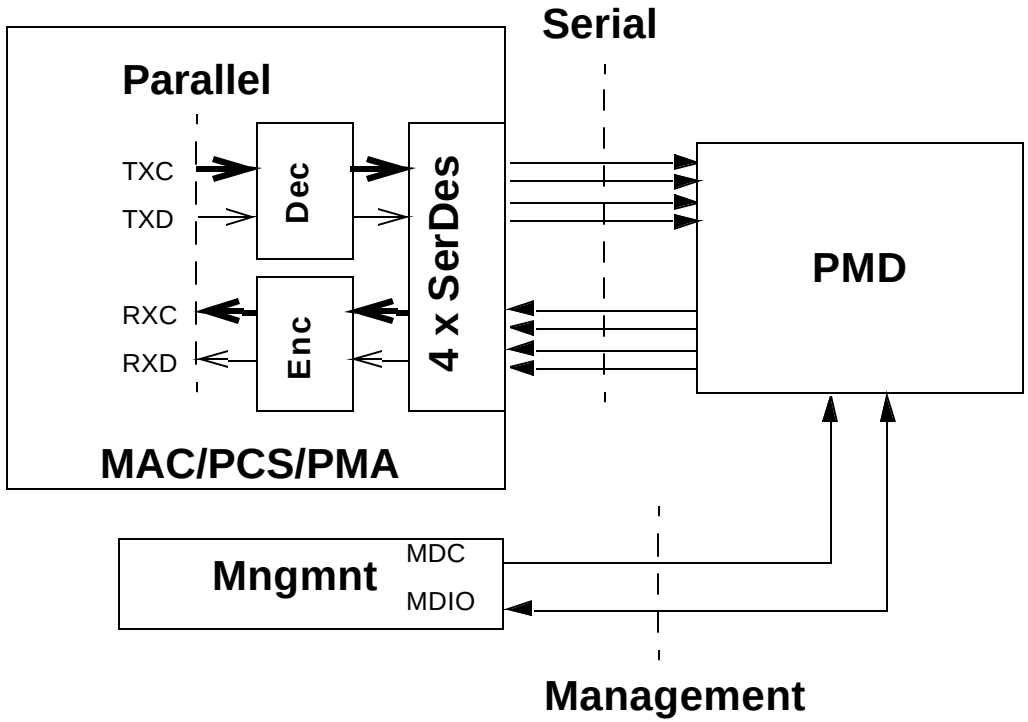
Management Interface

- Reuse management interface protocol from 802.3u clause 22
- Define new bits and registers as needed for 10 Gbps operation
  - Need to be careful about bit and register consumption
- Propose use of the ST sequence (00) for transactions with PMD
  - Use of a new ST sequence opens up a fresh set of registers
  - PHY and PMD registers can be defined independently

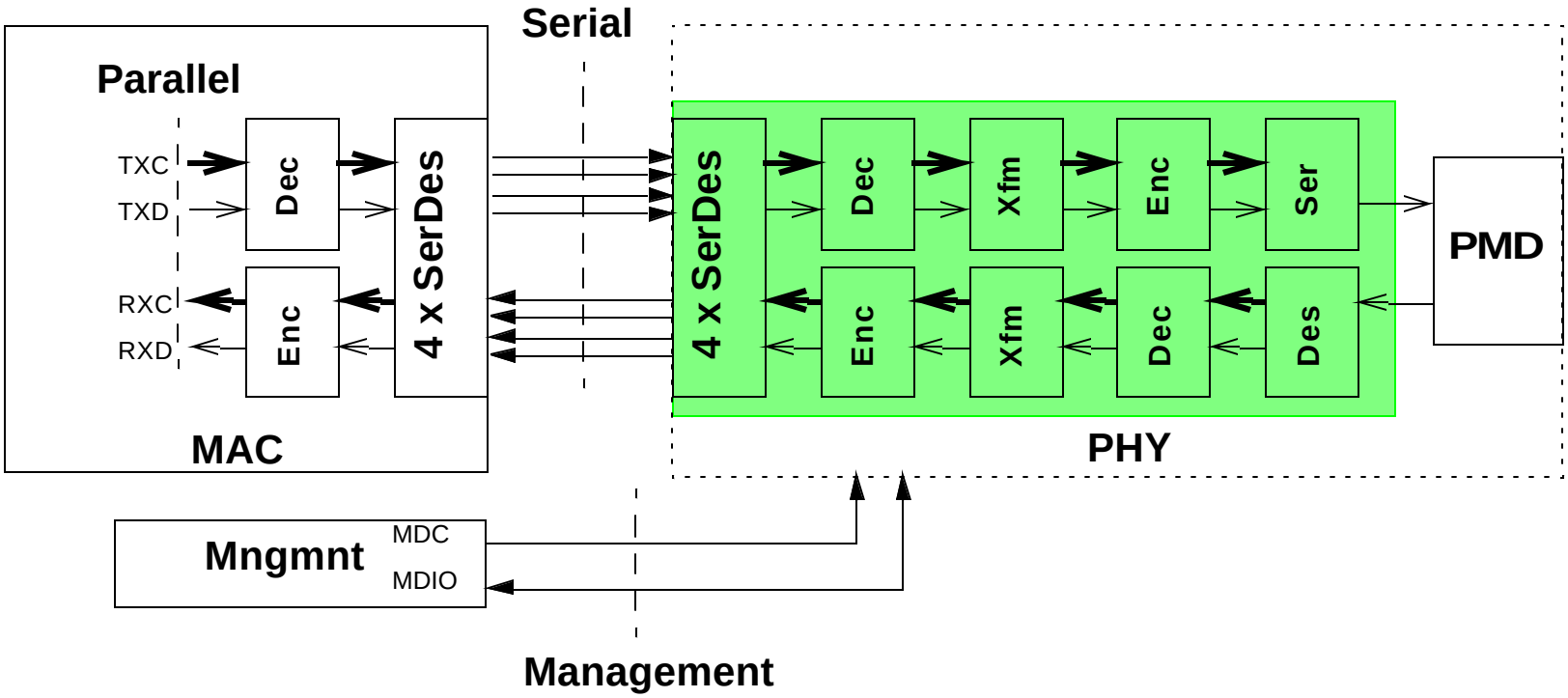
Scaling, Integration, Flexibility

- The parallel interface can be scaled in speed and width
  - 32 data bits, 4 C bits
  - 16 data bits, 2 C bits
  - 8 data bits, 1 C bit
- The delimiter and special character definitions remain constant
- Since this is not an exposed interface (no connector), the speed and width choice is up to the implementer
- No need to “negotiate”, monitor, or control the speed and width

Scaling, Integration, Flexibility



Scaling, Integration, Flexibility



Summary

- Together, these two interfaces provide lots of flexibility
- Both interfaces can be scaled in speed and width without changing the protocols
- The EIA/JEDEC SSTL_2 standard can be referenced for the parallel interface electrical specification
- The existing clause 22 management interface can be reused and extended to manage PMDs