Hari The Universal Electrical Interface

Contributing Companies*: Agilent, AMCC, Broadcom, Brocade, Giga, Extreme Network, Gadzoox, IBM, LSI, Picolight, Sun Microsystems, Vitesse

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* Companies participated in the conference calls.

Key Issues

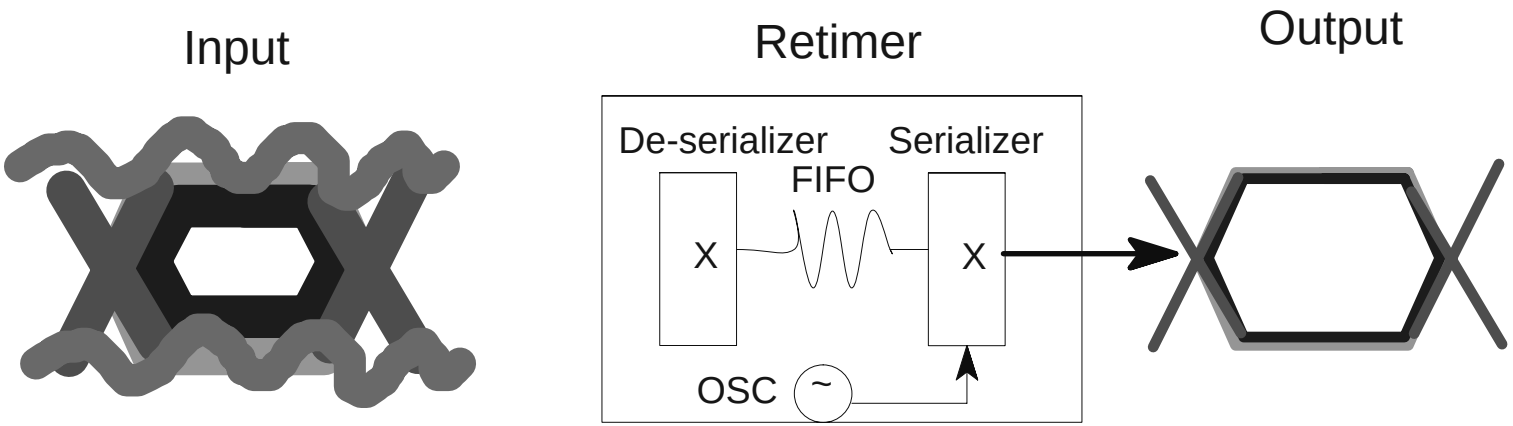
- Hari Concept
- High Speed electrical interface
- I/O amplitude
- Interconnect specification
- Implemention
- Golden PCB
- Hari compliance point
- Hari Jitter proposal
- Mask Compliance
- Skew

Hari Electrical Overview

- Hari provides flexible interconnect from ASIC to PMD or from ASIC to ASIC.
- Hari provides jitter isolation between the system and PMD.
- Hari links are designed to be user friendly and compatible with future generation of ASICs.
- Each Hari link provides BER of 1E-13.
- Hari electrical I/O may be used as a generic backplane technology.

Hari PMD Concept

- Hari PMD provides jitter and noise isolation.
- The jitter resets to a local reference oscillator or gets attenuated by the use of a high quality repeater.



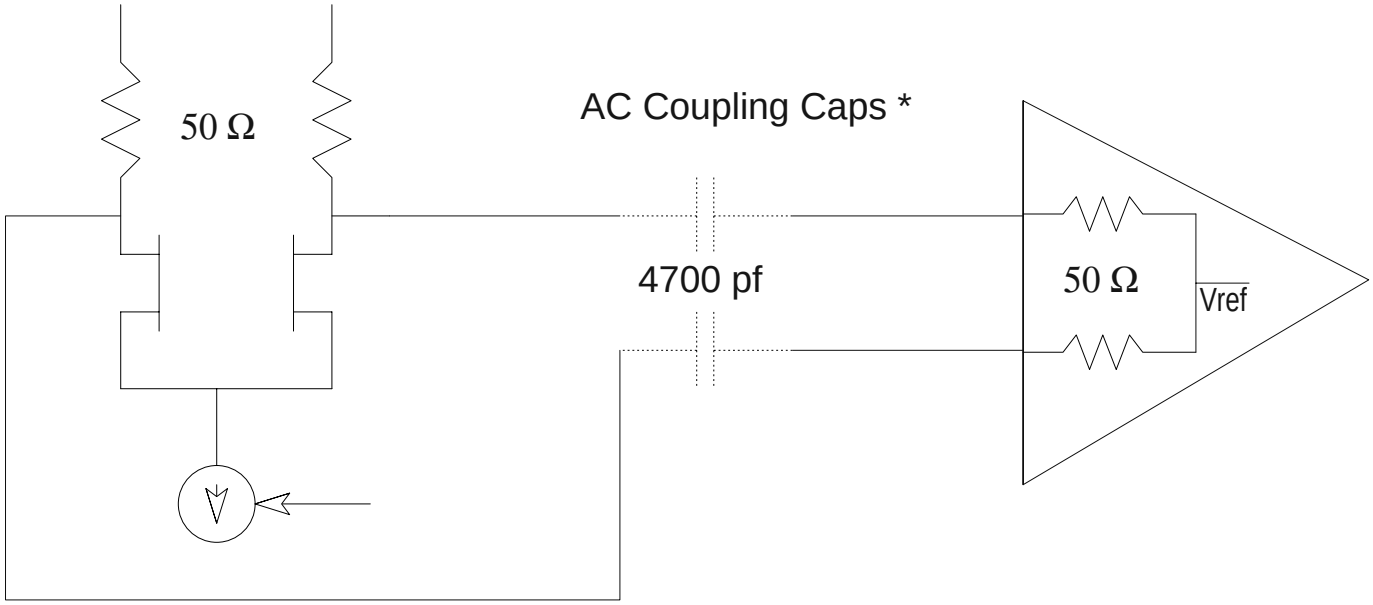
Comparison of the HS I/O and Hari Interface

Item	PECL	LVDS/short	Hari*
Transmitter			
Vo Dif(max)	2000 mV	400 mV	800
Vo Dif(min)	1200 mV	250 mV	500
Voh	AC	1475 mV	AC
Vol	AC	925 mV	AC
Iout nominal	16 mA	3.25 mA	6.5 mA
Receiver			
Vin (max)	2000 mV	400 mV	1000 mV
Vin (min)	200 mV	200 mV	175 mV
Loss 50Ω	15.56 dB	1.94 dB	9.1 dB

Hari electrical interface is based on low swing AC coupled differential interface.

Hari Suggested Termination

- Hari Interconnects are AC coupled at the receiver inputs.

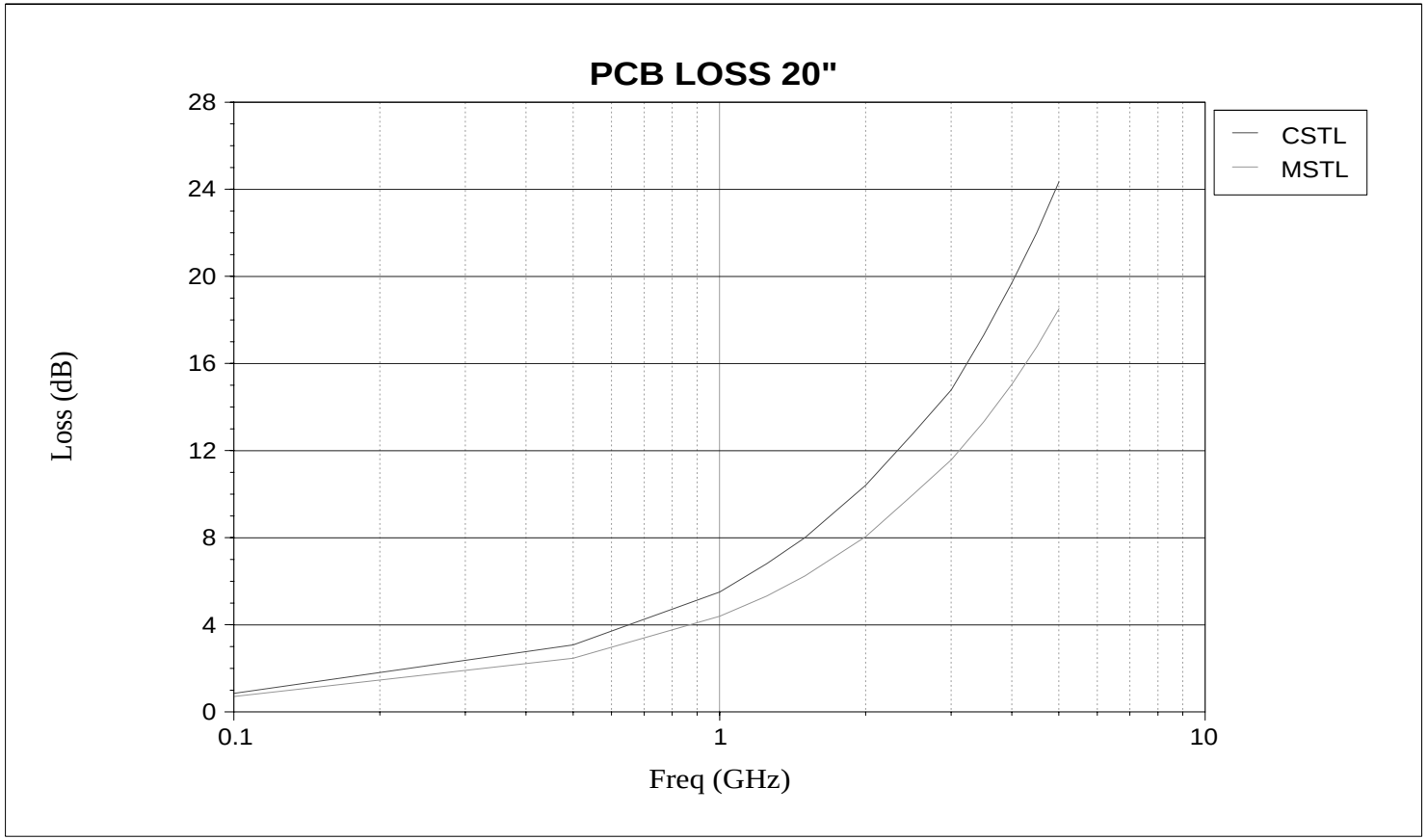


* It is recommended were possible to use 0.75V for the common mode voltage to allow the user for possible direct connect in backplane applications.

Hari Measurement Methodology

- Hari links compliance point is at the receiver.
- Transmitter may use equalization as long as it does not exceed max receiver input.
- A pre-emphasis driver will use a golden PCB to test for compliance. Drivers must meet jitter and eye mask from 0.25" to Golden PCB maximum distance ~20-24".
- Standard drivers are not required to use the Golden PCB for transmitter compliance.
- Transmitter jitter specification are provided for reference.
- A probe with equivalent response of the PCB can be developed for improved measurement accuracy.

Golden PCB



MSCTL: 5 / 5 / 5 mils

T=0.7 mil

h= 3.5* mil

CSTL: 5 / 5 / 5 mils

h= 14 mil

T=0.7 mil

* Z will change as silkscreen is added

Source HP Microwave Design System (MDS) Er=4.4, TanD=0.022, 0.5 oz

Hari Loss Budget

Baud Rate	2.12 Gb/s	2.5 Gb/s	3.125 Gb/s
Connector Loss (dB)	1	1	1
Next+Fext Loss (dB)	0.75	0.75	0.75
PCB Loss (dB)	7.35	7.35	7.35
Loss Budget (dB)	9.1	9.1	9.1
PCB Condition [1]	Normal/Worst	Normal/Worst	Normal/Worst
MSTL Loss Max (dB)/in	0.22 / 0.29	0.26 / 0.35	0.32 / 0.43
Max Distance (in)	33.4 / 25.3	28.3 / 21	23 / 17.1
PCB Condition	Normal/Worst	Normal/Worst	Normal/Worst
STL Loss Max (dB)/in	0.29 / 0.39	0.34 [2] / 0.46	0.41 / 0.55
Max Distance (in)	25.3 / 18.8	21.6 / 16.0	18 / 13.4

1. Normal PCB was assumed with loss tangent of 0.22, worst case it was assumed high temerture and humidity 85/85. Better grade of FR4 may reduce the loss by as much as 50%.

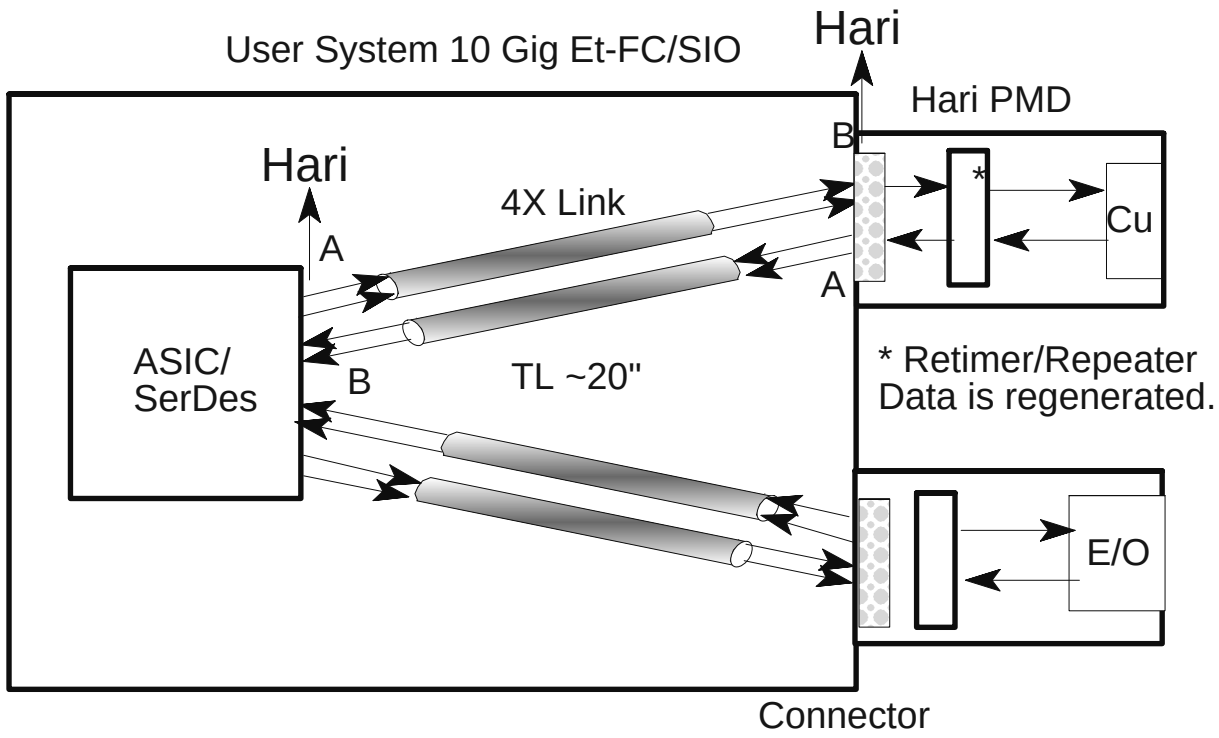
2. HP test measuremnt for 20" line showed 5.2 dB loss or 0.26dB/in based on the eye loss, the loss assumed here is very conservative.

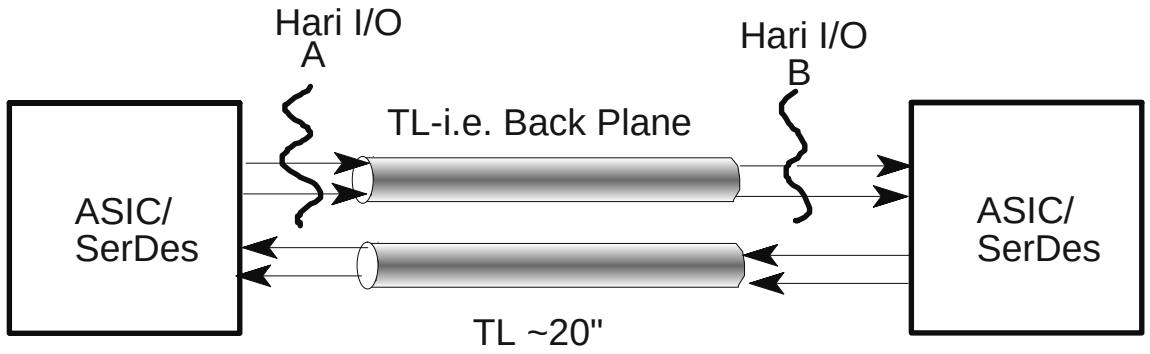
Hari Proposed Interconnect

Item	FC	FC-2Gig	GLM	GBE	Hari
Tr/Tf Min (ps) 20%-80%	100	75		85	60 [1]
Tr/Tf Max (ps) 20%-80%	385	192	400	327	131 [1]
Cable Impedance (Ω)	150+/-10	150+/-10	100 + RL	150+/-10	N/A
PCB Impedance (Ω)	150+/-15	150+/-15	100 + RL		100+/-10
Connector Impedance (Ω)	150+/-30	150+/-30	100 + RL	150+/-30	100+/-30
Source Impedance (Ω)	?	?	100 + RL		100+/-20
Load Termination (Ω)	150+/-30	150+/-30	100 + RL	150+/-10	100+/-20
Exception Window (ps)	800	N/A	NA	700	N/A [2]
Return Loss (dB)	N/A	15 [3]	8.18	N/A	10 [4]
Differential Skew TX (ps)	25	15	?	25ps	15 ps
Differential Skew RX (ps)	254ps	127	?	175 ps	75 ps

Notes:
1. Optional if the transmitter meets the receiver jitter and eye mask with golden PCB.
2. Exception not required instead return loss specified.
3. for testing inductive component such as transformer the TDR is inappropriate and should be tested with sweep frequency of bit rate/10 to x2 of the bit rate.
4. SerDes inputs must meet the return loss from100 MHz to 2.5 GHz (0.8x3.125Gbaud).

Example of Hari Interconnect



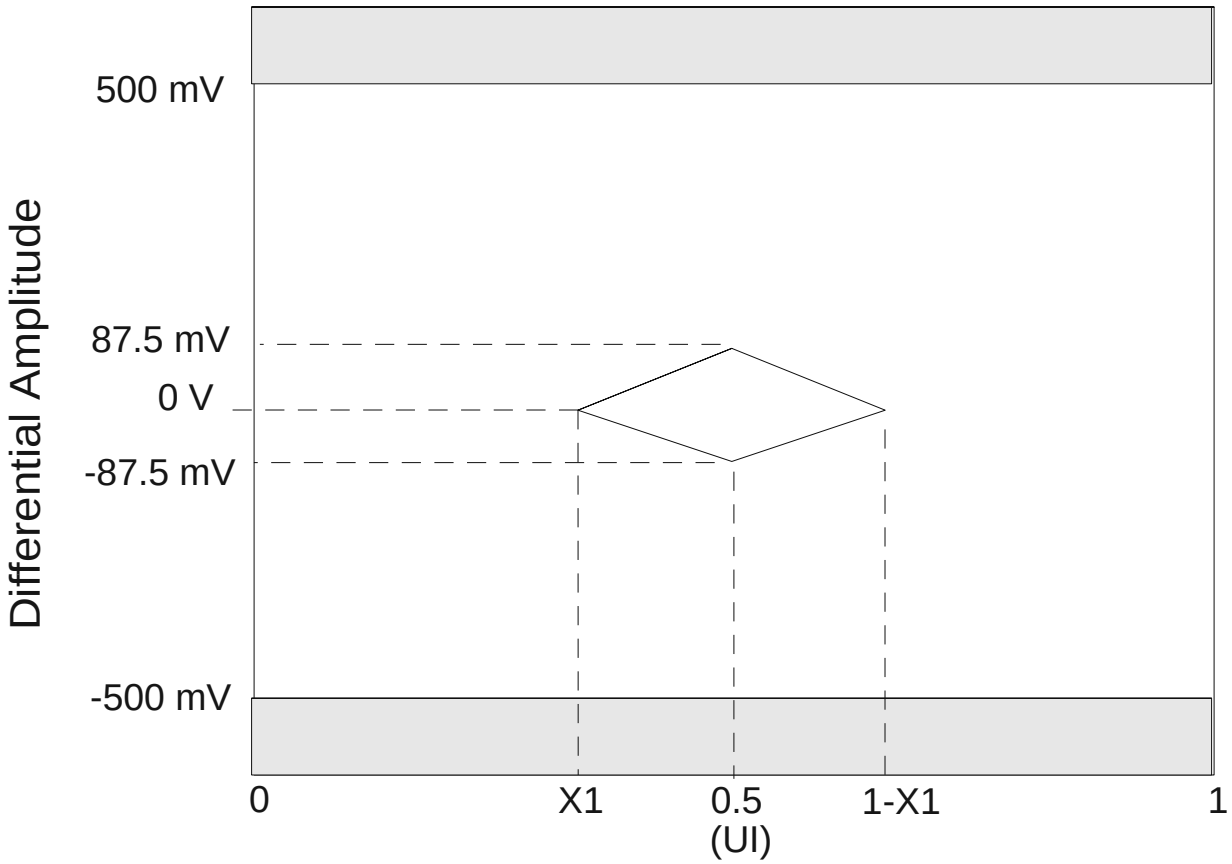


Hari Jitter Proposal

Jitter Compliance Points	A *	B *		
Proposed Hari @2.12Gb/s	471			
DJ UI	0.17	**0.41**	External PMD	
TJ UI	0.35	**0.65**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	6.06	**8.07**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	5.77	7.70		
Proposed Hari @2.5Gb/s	400			
DJ UI	0.17	**0.41**		
TJ UI	0.35	**0.65**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	5.14	**6.86**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	4.90	6.54		
Proposed Hari @3.125Gb/s	320			
DJ UI	0.17	**0.41**		
TJ UI	0.35	**0.65**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	4.11	**5.49**		
1-sigma RJ at max DJ for BER 1E-12 (ps)	3.92	5.23		

Note: * A point (TX) is for reference, but B (RX) is for compliance.
The SerDes component should have better jitter performance than specified here to allow for system noise.
1-Sigma value listed here are at maximum DJ, if the DJ value is smaller then the 1-sigma RJ may increase to the total jitter value.

Receiver Mask Compliance



X1=0.325 UI

Hari Skew Budget

Hari Skew for	2.12 Gb/s	2.5 Gb/s	3.125 Gb/s
ASIC + PCB A-B (ns)	0.5	0.5	0.5
Hari Tx PMD (ns)	0.5	0.5	0.5
Media Skew (ns)	7.42	6.0	4.25
ASIC + PCB B-A (ns)	0.5	0.5	0.5
Hari Tx PMD (ns)	0.5	0.5	0.5
Total Link Skew (ns) *	9.42	8	6.25
Total Skew in bits	20	20	20

Note: *Link skew is defined from protocol to protocol device.

Total of 2 ns of skew is allocated for the transmit and receive portion of ASIC+PCB+PMD.

Conclusions

- Hari signaling is based on low swing differential AC coupled.
- The interconnect supports ~20" of PCB at BER of 1E-13.
- The retimer reset the jitter margin allows for isolation of noise and jitter domain.
- Normative jitter specification are for the receivers or transmitters tested with Golden PCB.
- A transmitter meeting jitter specifcation and eye mask at the source is not required to be tested with Golden PCB.
- All TX output shall meet the eye mask from 0.25" to maximum PCB trace.