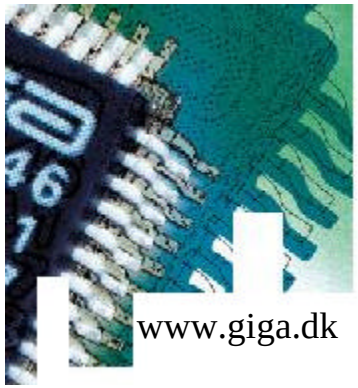


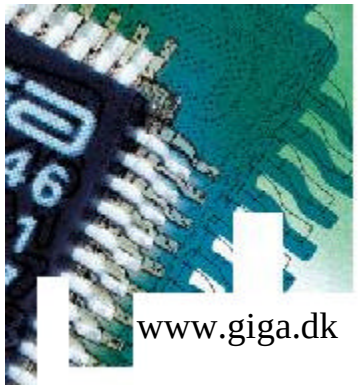
Serial LAN PMD Architecture Options

- the 10G+ IC designers perspective

Outline

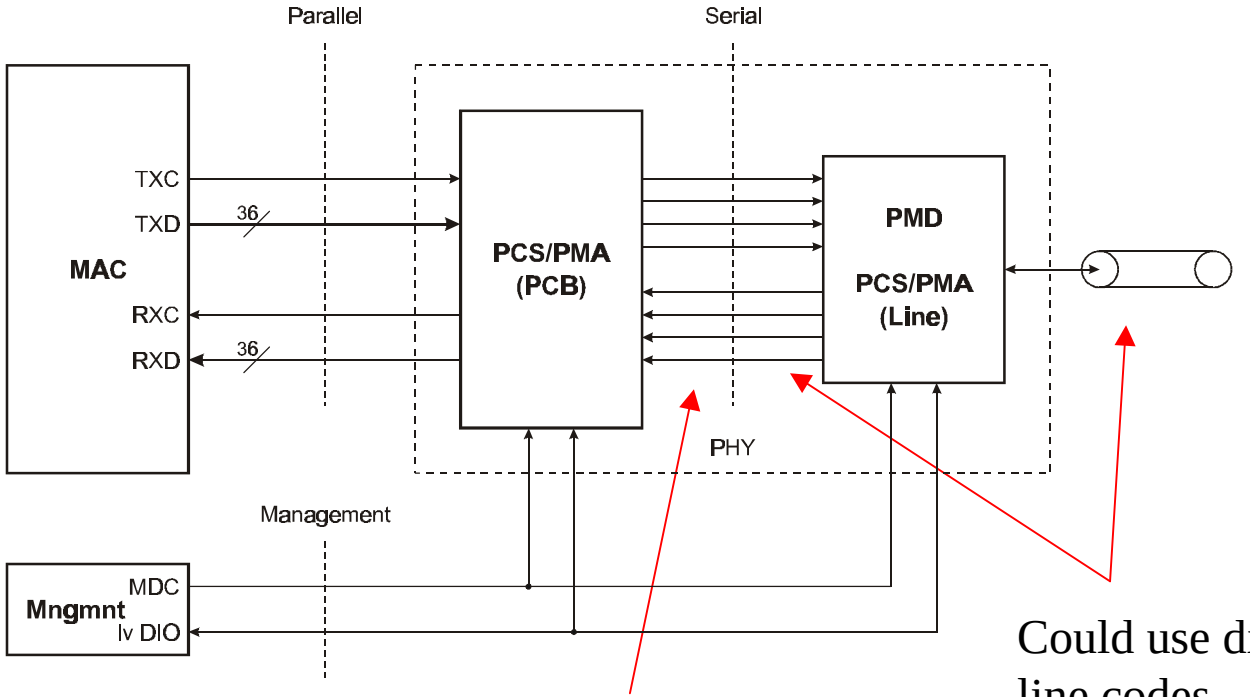
- Present various serial LAN PMD options
- ...and how they comply to the PMD evaluation criteria.
- Provide basis for serial PMD discussions.

Henning Lysdal
10GE Project Manager
GiGA A/S



10GE PMD Interface

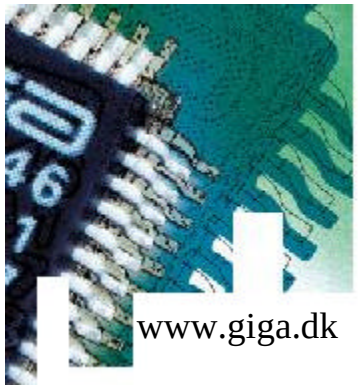
Based on the presentation “10Gig MII update”, Howard Frazier, York Interim meeting.



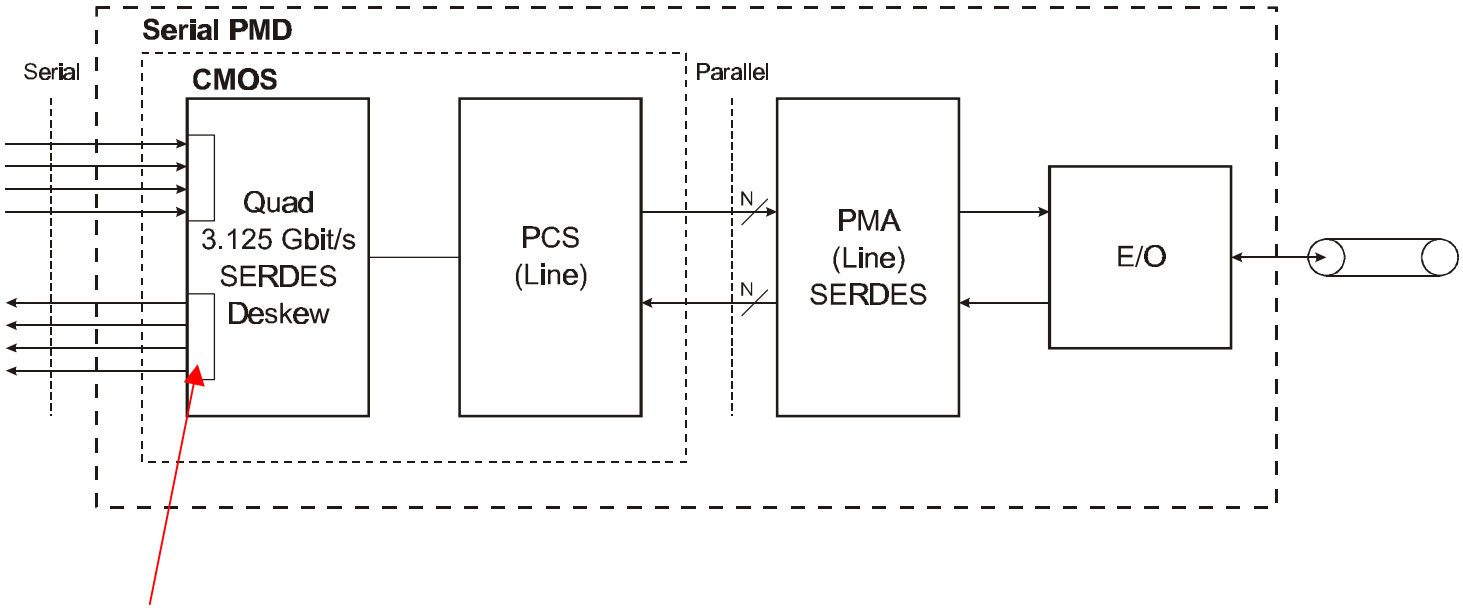
Up to 16’’
PCB-track

Could use different line codes

(8b/10b, SONET ...)



Inside the Serial PMD



Using same macrocells as in PCS/PMA and/or MAC ASIC

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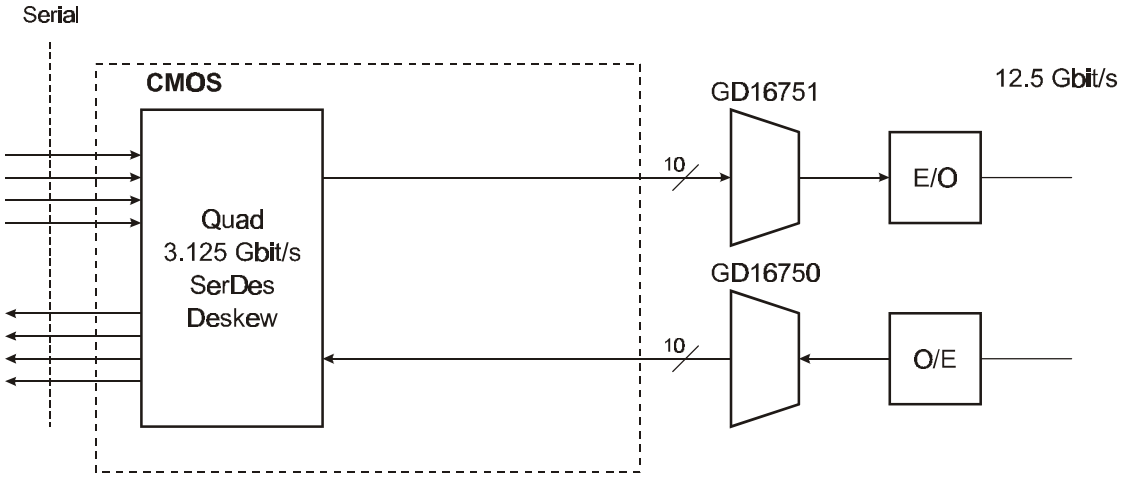
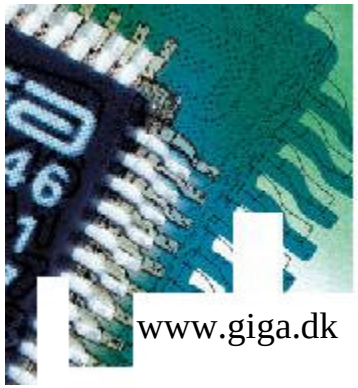
Option 1: 12.5 Gb/s Line Rate, 8b/10b



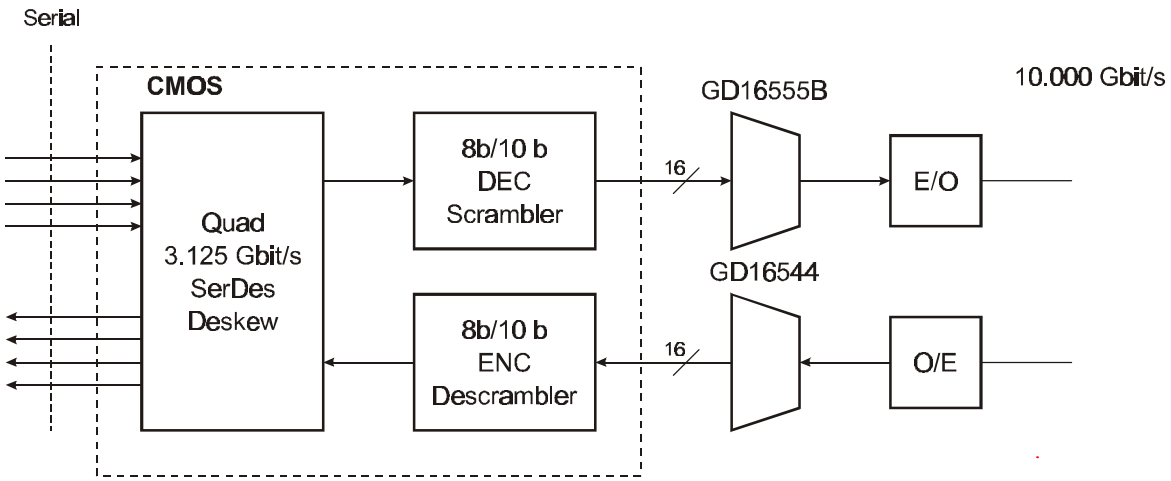
+ Uses well-known 8b/10b line code.
+ Allows 1GE-like architecture.
÷ Requires 12.5 Gb/s SerDes (SiGe) and optics.

"York" evaluation criteria

- Only applicable to LAN PHY.
- Longer time to prototype (SerDes prototypes in 2Q00, CMOS & Opto ???).



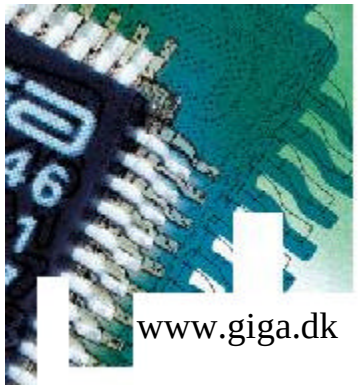
Option 2: 10.0000 Gb/s Scrambled



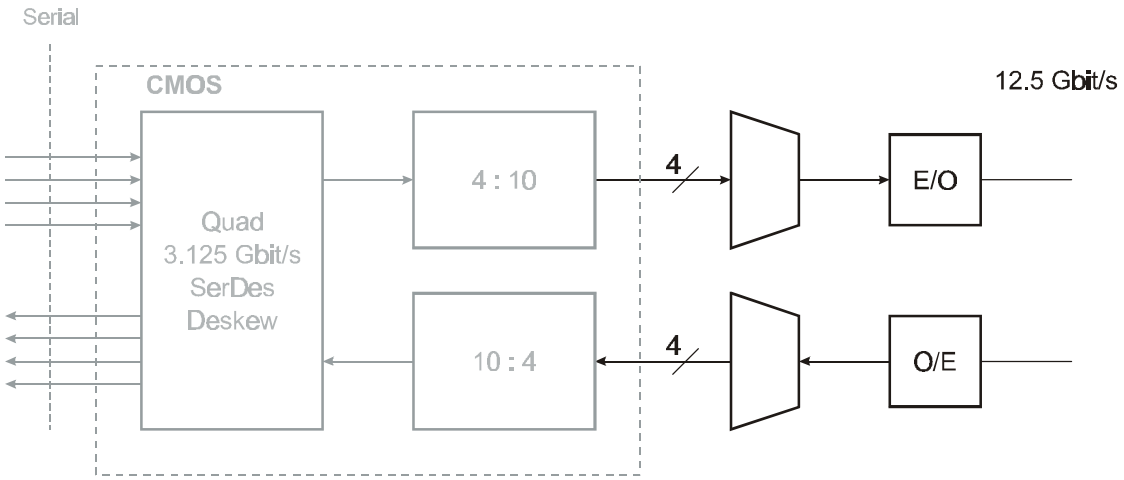
+ Full 10.0000 Gb/s data rate.
+ Uses existing SONET SerDes (Si), and only 10 Gb/s optics.
+ Uses same SerDes and optics as most likely WAN-PMD.
÷ Requires new development and verification of scrambler.

"York" evaluation criteria

- Use same hardware to both LAN and WAN PHY with selectable scrambler and reference clock (SONET rate and 10.0000 Gb/s).
- Shorter time to prototype (SerDes available now, CMOS ??).



Option 3: No CMOS in PMD



WITHOUT deskew in 12.5G SerDes

+ Lower device count in PMD.

÷ Requires 12.5 Gb/s SERDES (SiGe) and optics.

÷ Limits allowed skew on 4x serial interface.

"York" evaluation criteria

- Only applicable to LAN PHY with shorter PCB tracks.
- Longer time to prototype (New SerDes).

WITH deskew in 12.5G SerDes

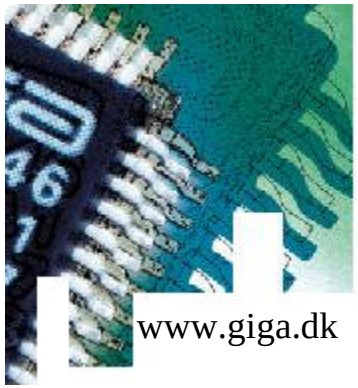
+ Lower device count in PMD.

÷ Requires 12.5 Gb/s SERDES (SiGe) and optics

÷ Power-hungry SerDes.

"York" evaluation criteria

- Only applicable to LAN PHY.
- So far no vendor support for SerDes.

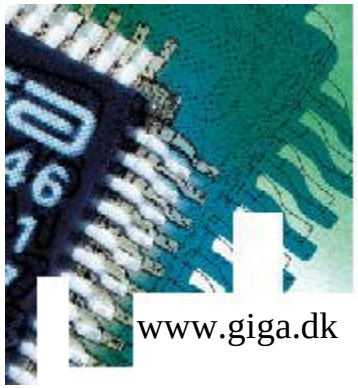


Narrowing the Serial LAN PMD Field

- Option 1: 12.5 Gb/s, Line Rate 8b/10b
- Option 2: 10.0000 Gb/s Scrambled
- Option 3: restricts PCB track length *or* requires “unrealistic” Serdes.

Major differences:

- SerDes and optics:
  - Option 1 requires 12.5 Gb/s.
  - Option 2 uses existing SerDes and only 10 Gb/s optics.
- Line code (En/Dec):
  - Option 1 uses well-known 8b/10b.
  - Option 2 requires new scrambler.



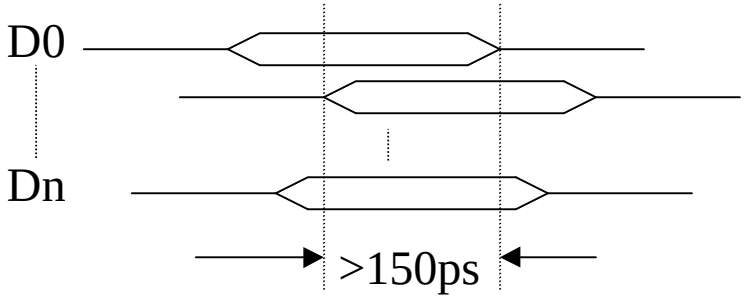
SerDes Parallel Width

- why 10-bit and 16-bit resp.

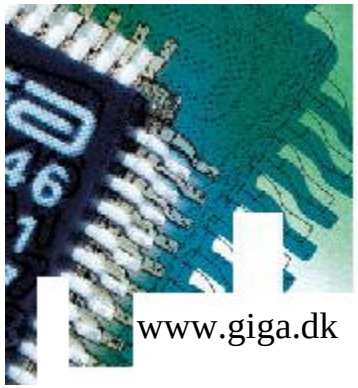
Reducing width tightens timing requirements, but reduces size.

The minimum width is determined by:

- A high-speed mux will require an estimated 150ps data valid window where all data can be registered on the same clock:



- The 10-bit interface of option 1 lends itself to 1GE-like architecture.
- The 16-bit interface of option 2 leverages existing SONET devices.



Preliminary SerDes Conclusions

- 16:1 is a serious LAN PMD option and doesn't require SONET overhead and framing, and offers full data rate.
- ... it does however require a new scrambler, which might not be feasible.
- The CMOS chip inside the PMD offers opportunities to add functionality to the transceiver modules.
- ... and to move complexity from the power hungry high-speed SerDes into the CMOS.
- There will be a need for both 10:1, 12.5 Gb/s and 16:1, 9.95/10.0000 Gb/s.