IEEE 802.3, HSSG – 10 Gigabit Ethernet MINUTES
Study Group Plenary Meeting
November 8 – 12, 1999
Kauai, Hawaii

Prepared by:
Jeff Warren – Extreme Networks

Administrative:

The meeting convened at about 8:41AM, November 9th, 1999. Jonathan Thatcher, the High Speed Study Group Chairman, opened the meeting with a presentation of the agenda, now available at the IEEE web site
http://grouper.ieee.org/groups/802/3/10G_study/public/nov99/index.html.

Jonathan then volunteered Jeff Warren to act as recording secretary for the meeting and went on to review the agenda. A motion to approve agenda by Bob Grow, passed by acclamation.

The next meeting is in Dallas, TX from Jan 18th – 20th, and is hosted by TI. After that the next Plenary is in Albuquerque, NM from March 6th – 10th. This March meeting will be the first official meeting of the 10 GE task force.

An e-mail reflector has been set up for the HSSG, stds-802-3-hssg@mail.ieee.org To be added to the reflector, send an e-mail to majordomo@ mail.ieee.org with the following line, subscribe stds-802-3-hssg <your email address>. To send a message to the HSSG reflector use the email address, stds-802-3-hssg@ieee.org

The voting rules can be found at http://grouper.ieee.org/groups/802/3/rules/member.html
The 802.3 patent policy can be found at http://grouper.ieee.org/groups/802/3/patent.html

The PAR, Five Criteria and Objectives will be published on HSSG web site. Thank you to all for the presentations, please use the reflector. The HSSG meeting was adjourned at 3:43PM on Wednesday the 10th of November.

Outline:

Meeting Goals:

The major goals for this November 1999 Plenary Meeting were to:

1. Get the PAR and 5 Criteria approved, submit draft to SEC
   - **Results:** The HSSG unanimously approved forwarding the PAR and 5 criteria to 802.3. Also 802.3 approved unanimously forwarding the PAR and 5 criteria to the 802 Exec. The 802 Exec approved unanimously forwarding the PAR and 5 criteria to NesCom. NesCom approval can happen as early as end of January 2,000 – that would mark the official start of the High Speed Working Group.
2. Start to consolidate our thinking (concepts) on what 10 Gig E should be
   - **Results:** We had an efficient, professional meeting with 31 presentations laying the ground work for many topics and challenges to come over the next 6 to 8 months.
3. Organize (plan) for the January 2,000 Interim meeting in Dallas, TX.
   - **Results:** An interim is planned to begin narrowing the focus of this High Speed Working Group.

HSSG Objectives:

1. Preserve the 802.3/Ethernet frame format at the MAC Client service interface.
2. Meet 802 Functional Requirements, with the possible exception of Hamming Distance.
3. Preserve minimum and maximum FrameSize of current 802.3 Std.
4. Support full-duplex operation only.
5. Support star-wired local area networks using point-to-point links and structured cabling topologies.
6. Specify an optional Media Independent Interface (MII).
7. Support proposed standard P802.3ad (Link Aggregation).
8. Support a speed of 10.000 Gb/s at the MAC/PLS service interface.
9. Define two families of PHYs
   - A LAN PHY, operating at a data rate of 10.000 Gb/s
   - A WAN PHY, operating at a data rate compatible with the payload rate of OC-192c/SDH VC-4-64c
10. Define a mechanism to adapt the MAC/PLS data rate to the data rate of the WAN PHY.
11. Support fiber media selected from the second edition of ISO/IEC 11801 (802.3 to work with SC25/WG3 to develop appropriate specifications for any new fiber media).
12. Provide Physical Layer specifications which support a link distances of:
    – At least 100 m over installed MMF
    – At least 300 m over MMF
    – At least 2 km over SMF
    – At least 10 km over SMF
    – At least 40 km over SMF

Agenda:

Speaker		Topic	Time Allc	Actual Start Time
Jonathan Thatcher		**Opening Business**	0:25	8:41 AM
Jonathan Thatcher	C	Introduction to the common PMD Interface ("Hari")	0:30	9:00 AM
Rich Taborek	C	"Hari" Coding Functions; Features & Rules	0:30	9:33 AM
		Break	0:25	10:22 AM
Howard Frazier	C	10Gig MII Update	0:45	10:47 AM
Richard Dugan	C	"Hari" Electrical Specifications	0:30	11:05 AM
Howard Frazier	C	Applying "Hari" to Ethernet	0:10	11:35 AM
Mike Hackert		TIA FO-2.2.1; Status Update	0:10	11:40 PM
		Lunch	1:15	11:50 AM
Tom Palkert		Optical Interoperating Forum Report	0:15	1:12 PM
Bruce Tolley		Update on Fiber Survey	0:15	1:22 PM
Steven Haddock		Economic feasibility (Link Aggregation Vs 10GbE)	0:10	1:30 PM
Ed Cornejo		Economic feasibility of Serial 10GE	0:10	1:40 PM
Paul Bottorff		Economic feasibility of WAN-Access Soln	0:10	1:43 PM
Mike Jenkins		Feasibility of CMOS at 3.125G	0:15	1:53 PM
Mark B. Ritter		Word Striping on Multiple Serial Lanes	0:20	2:02 PM
		Break	0:25	2:33 PM
Fred Weniger		10 GbE - OC-192 Compatible Serial Framing	0:15	3:00 PM
Iain Verigin		SerDes Interface	0:20	3:18 PM
Henning Lysdal		Serial LAN PMD Architecture Options	0:20	3:29 PM
Gary Nicholl		Packet-Over-SONET: A Technical Primer	0:30	3:40 PM
Richard Dugan		Low overhead coding proposal for 10GbE serial	0:20	4:18 PM
Greg Copeland		Coding for the optical channel	0:20	4:41 PM
ChanGoo Lee		Jitter Considerations of MB810	0:20	4:57 AM
		Adjourn	0:25	5:13 PM
Wed, 10 Nov				
		Reconvene		8:38 AM
David Dolfi		10 GbE Fiber Optic Links – Link Model Update	0:15	8:40 AM
		Break	0:25	AM
Ed Cornejo		Serial PHY update - 15min	0:15	8:55 AM
John Crow	B	Serial, 12.5 Gbaud, 10 km, SMF Link with CDR	0:20	9:11 AM
Israel Ury	B	Optical Components for 12.5 Gbaud Serial Links	0:20	9:30 AM
Jens Fiedler		PMD Considerations and Results for 10 Gig Serial	0:10	10:25 AM
Edward Chang		Design of 300 m Installed 62.5 MMF at 1300 nm	0:20	10:15 AM
Jaime E. Kardontchik		300 meter on installed MMF	1:00	10:42 AM
		Lunch	1:15	11:27 AM
Richard Kriese		VCSEL-Based Solutions for 10 Gig Ethernet	0:10	1:10 PM
Del Hanson		WWDM Interface Specification Proposal	0:20	1:20 PM
Rich Taborek		Multilevel Serial PMD Update	0:30	1:45 PM
Norival Figueira		10 Gigabit Ethernet WAN PHY Alternatives	0:15	2:14 PM
		Break	0:25	2:22 PM
Giaretta Georgio		New MMF -- How far can we go?	0:10	2:50 PM
Ed Cady	A	Information on 10 Gig Short Haul Copper	0:20	2:59 PM
Dan Dove	A	Why we need a 10Gigabit Copper Link	0:15	3:15 PM
Jonathan Thatcher		**Motion Madness & Closing**	2:00	3:35 PM
		Adjourn	0:25	3:43 PM

Presentations:

1. Common PMD Interface "Hari"
   - Jonathan Thatcher - Picolight
   - Time Allocated = 30 minutes
   - Start 9:00AM
   - End 9:29AM

- **Presentation Highlights:** Mr. Thatcher stated that the history of the Hari Interface began prior to the 10 Gigabit Ethernet call for interest back in March of 1999 and that this included industry groups such as FC, NGIO, OIF in addition to many of the current 802 HSSG participants. The Hari interface came about because there will be multiple PHY solutions to cover the various 10 GE distance requirements (100m, 300m, 2km, 10km, 40km) and it is highly desirable for all of these PMD's to support a common PMD interface with the fewest pins and highest speed signals possible. There are a number of issues to deal with such as support for multiple protocols and encoding schemes, support for the various PMD variants, layout, timing and electrical considerations. Since the 8B/10B code is well understood and commonly used there's an incentive to use it. Hari does not attempt to stress current technology beyond its limits, for example keeping the data rate to 3.125 Mbps for CMOS cores, support in the range of 20 inches over FR4 to aid board designers who must physically separate the PMD optical transceivers from the components they attached to. An OSI layer stack, which highlights where Hari fits in was shown. The "Hari" interface is a 4x1bit interface. Jonathan showed a proposed block diagram of the HARI Generic 10 GE transceiver data flow to help HSSG members understand the various functions, such as PLL, SerDes, encode/decode, and the SKIP character used to insert/delete based on clock variations. There were some techniques in this pitch that are not fully agreed upon, such as how to correct for clock variations. There was a convenient transceiver functional comparison table presented, it details the transmit, receive, and management functional requirements for the various transceiver types identified to date within the HSSG, see page 14 of Jonathan's presentation.

2. Hari Coding Objectives
   - Rich Taborek – Independent
   - Time Allocated = 30 minutes
   - Start 9:33AM
   - End 9:58AM

- **Presentation Highlights:** Mr. Taborek's presentation on "Hari" dealt with the coding techniques. In particular the desire to keep Hari coding protocol independent, application independent, PMD signaling independent and most importantly keep the coding simple. The 8B/10B K28.5 comma character shall be used for word level link synchronization. The 8B/10B K27.7 **/S/** shall be used for channel (or in Hari terms, Lane) ordering, i.e. identification of Lane 0. The 8B/10B K28.0 **/R/** shall be used for the insert/remove code, this provides clock tolerance compensation, and the K30.7 character to signal error conditions. The Lane-to-Lane skew budget was discussed, for example the skew allocated to the PCB and SerDes. The maximum lane-to-lane skew is 6.4 ns running at 3.125 Gbaud. Deskew is only necessary during initialization. Mr. Taborek explained that the current "Hari" coding rules are very

simple, similar to the tried and true 1000Base-X PCS, cost effective and rather flexible to implement. A number of slides were devoted to helping the audience understand the Lane concept. These slides focused on the repeating Idle pattern, Start and End of packet delimiters, Lane 0 identification, packet data, error code-group, data skewing/deskewing, plus the insertion and removal of **/R/** columns to deal with clock tolerance compensation.

- Question/Answer:
  - Mark – how is data deskewed if it gets out of line at transceiver's receiver. A transceiver doesn't need to perform deskew, if PMD does deskew then it will do this after the receiver.
  - Mike – alignment independence – what does it mean? The Hari encoding (8B/10B) is alignment independent.
  - Greg - There's a mix of what a PMD does, sometimes it has aligned data and some times it does not. Yes, Hari has to cover all these cases, meaning perform the deskew function all the time.

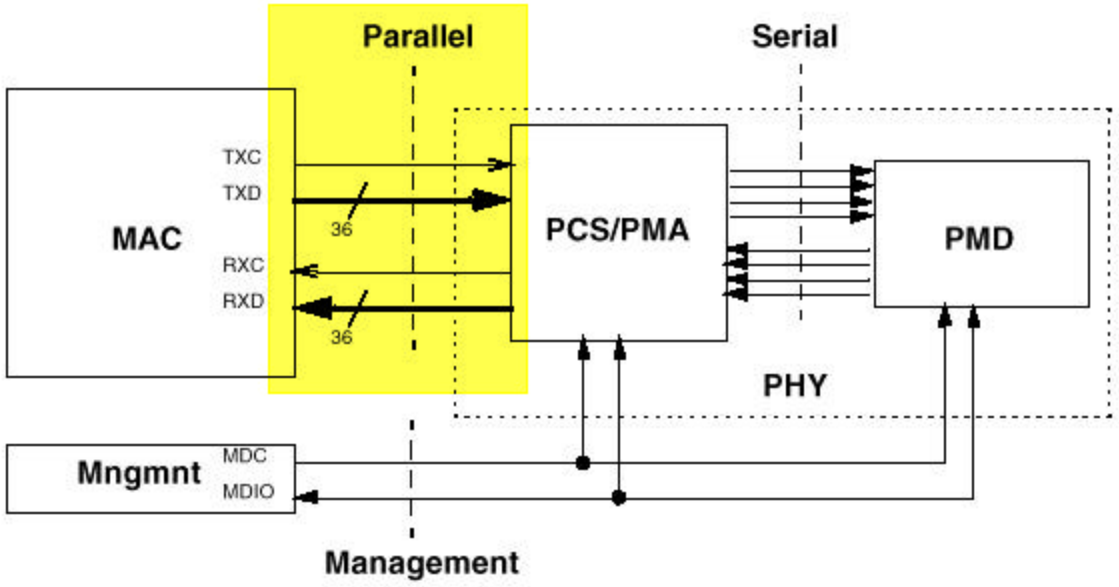
3. 10 Gig MII Update

- Howard Frazier - Cisco Systems (Speaker)
- Time Allocated = 45 minutes
- Start 10:47AM
- End 11:38AM

- **Presentation Highlights:** Mr. Frazier's presentation focused on the requirements and attributes of two interfaces, the Parallel interface which connects the Media Access Controller (MAC) with the Physical Layer (PHY) consisting of the PCS and PMA sub-layers, and the Serial interface which connects the PCS/PMA with the optical PMD transceivers. Please reference Mr. Frazier's Interface diagram on page 6 of 27 for a visual of where these two interfaces are located. The overall goal for providing these interfaces is to allow multiple physical and transceiver variants. By doing a complete job of defining these interface specifications, multiple independent groups can go off and develop different portions of the 10 GE specification in parallel. Scalability is key, by focusing on this point we can incorporate newer (faster) technology in the future, scaling down the 32/4 (Date/Control Lines) to 16/2, or 8/1. In the past, PMD optical transceivers did not include silicon for advanced functions, this is being reconsidered now. The full duplex Parallel interface is wide, currently 4 bytes wide (32 bits) plus 4 control lines. More specifically the first channel, Lane 0 contains data lines 'D<0:7>' plus control line 'C0' which is associated with this channel. This MAC-to-PHY interface is probably in the order of a few inches now. Data is clocked on both the rising and falling edges of the clock. The Serial interface is used to get physical separation of the transceivers and the PHY/MAC technology. The media specific encoding may/may not be placed in the transceivers. Embedded delimiters rather than discrete signals are used across the parallel interface because this scheme scales well. In this case each LANE has a control line which is used to indicate when these special characters are embedded in the data lines. The start of a packet is signaled only on Lane 0, however the end of the packet can be signaled on any Lane. For the parallel interface there are several standard electrical specifications being considered, such as SSTL_2. The Serial interface is comprised of four 2.5 Gbps

full duplex data signals (Lanes) with management provided by the current MDIO/MDC interface, new management bits and registers will be required. This serial interface byte stripes the data across these four Lanes. The 8B/10B NRZ encoding is recommended again because of 802.3's familiarity with this encoding scheme, ease of implementation, etc. This implies that the baud rate will be 3.125 GBaud. Clock tolerance compensation requires that a minimum IPG of 12 bytes be transmitted and the received IPG must be 4 bytes or more. Oscillators can be +/- 100 ppm. Since the SOP (i.e. KR) bytes appear as KKKKRRRRKKKKRRRR on a serial transmission system, the LANE synchronization is accomplished by aligning the 1st K of a KKKK sequence to LANE 0. Chances are that this parallel interface will be embedded in a combo MAC/PCS/PMA device to limit the number of I/O required. By placing some silicon in the transceivers, the transceiver vendors can adapt just about any of the PMD variants to the combo MAC/PCS/PMA device.

- Questions/Answers:
  - Brad – Will the management interface use preamble suppression? Yes
  - Ben – Looks like you're using a variable IPG, yes this simplifies packet parsing.
  - Paul – Is Hari applicable across LAN & WAN PHYs? Yes it can be, depends on the amount of function one puts in the transceiver.
  - Shimon – If we start on LANE 0, over subscription can occur. The over-riding objective was to make packet processing easier.
  - Someone? – Can Hari support slower speeds? Unknown.
- Why pick 12 for IPG? Was picked for 1.488 packet rate.



4. Hari the Universal Electrical Interface

- Rich Dugan – Agilent Technologies (Speaker)
- Ali Ghiasi – Sun Microsystems
- Time Allocated = 30 minutes
- Start 10:00 AM

- End 10:21 AM

- **Presentation Highlights:** Mr. Dugan explained that the motivation for Hari is to provide a flexible interconnect from ASIC to PMD or from ASIC to ASIC. On each side of the Hari interface there exists a unique jitter domain, on one side the system jitter and on the other the PMD jitter. Jitter on each side is reset to a local reference oscillator, so one can think of Hari as providing jitter and noise isolation. A BER goal of 10EE-13 is desired for Hari links. Hari has a loss budget of 9.1 dB supporting potentially 20" of PBC distances. The compliance point (measurements) will be at the receiver. Mr. Dugan described the measurement methodology to be used for testing compliance to this electrical interface. Hari interconnections are AC coupled at the receiver inputs, more specifically low swing differential AC coupling. This universal Hari electrical interface can be used for generic back-plane interconnections. Mr. Dugan presented the proposed Hari Interconnect specification, examples of Hari interconnections, a jitter proposal, receiver mask compliance, and skew budget.
- Questions/Answers:
  - Atikem commented that more consideration is required on PBC parameters.
  - Bob Grow – ask if a "full specification was required in the document, answer yes.
  - Dan Dove – loss budget, what frequency are losses determined? Answer is half the Baud rate.

5. TIA FO-2.2.1 Task Group on Modal Dependence of BW Status Update

- Michael J. Hackert – Corning (Speaker)
- Time Allocated = 10 minutes
- Start 11:40 AM
- End 11:50 AM

- **Presentation Highlights:** Mr. Hackert updated the HSSG members with the latest TIA FO-2.2.1 task group's activities on modal dependence of bandwidth. FO-2.2.1's objective is to deliver improved system performance using MMF. They have conducted a validation experiment and are analyzing the data, initial results look promising and correlate with expected results. The experiment attempts to confirm that short-wave lasers which comply to a new launch condition and MMF (both 62.5 & 50 micron) meeting new BW requirements using restricted launch condition will result in an improved level of system performance. A half dozen manufactures for fiber and transceivers participated in the experiment. A recommendation is expected to go forward in January 2000 to the TIA group. They are also looking at 50-micron fiber performance, this way they will have recommendations for increased performance on both 62.5 and 50 MMF.
- Questions/Answers:
  - Impact of MM connectors – offset introduced? W/C 5-7 micron offset, beyond 5 micron of offset we see significant impact. If you go through multiple connectors, each with significant offset, what happens – our work isn't done, but can say it is not like just adding up the individual connector penalties.

6. Optical Internetworking Forum Report

- Tom Palkert - AMCC (Speaker)
- Scott Lowrey - Network Elements
- Time Allocated = 15 minutes
- Start 1:12 PM
- End 1:23 PM

- **Presentation Highlights:** Mr. Palkert's presentation, a liaison report, focused on one of three working groups within the OIF, the PLL working group. The other two working groups deal with architecture and OAM&P issues. The OIF mission is to "foster the development and deployment of interoperable products and services for data switching and routing using optical networking technologies". Mr. Palkert presented a few topics of interest to this HSSG that the PLL group is focusing on. They are, the development of specifications for SerDes/Framer electrical interface for OC-192, a standard system physical interface between the physical and link layer devices and a 10 Gb/s interface based on SONET/SDH standards with emphasis on Packet-Over-Sonet (POS). An interesting point was made that 75 % of OC-192 needs could be supported with a very short reach (100 to 500 meters) solution. For this the OIF is focused on parallel fiber (10X1.25Gbps). The HSSG should keep a close eye on these OIF activities. The OIF is currently pursuing a 16x622Mbps low voltage differential signal SerDes to Framer interface.

7. Update of Fiber Survey

- Bruce Tolley – 3Com (Speaker)
- Time Allocated = 30 minutes
- Start 1:22 PM
- End 1:28 PM

- **Presentation Highlights:** Mr. Tolley reported that he has only received six fiber survey responses. The objective of this study was to get granular data on installed fiber links and factor that data into the various proposals we have before us to make some decisions on supporting the installed base. Bruce made an additional plea to the group to get their fiber surveys filled out and returned to him as soon as possible
- Questions/Answers:
  - Ed – What does survey include? Answer, it's on the WEB – go read it, fill it out, and return it.

8. Link Aggregation 'vs' 10 GE

- Steve Haddock – Extreme Networks (Speaker)
- Time Allocated = 10 minutes
- Start 1:30 PM
- End 1:42 PM

- **Presentation Highlights:** Mr. Haddock discussed 10 GE economic considerations with respect to Link Aggregation. Steve began the discussion by stating that link aggregation and 10 GE are different solutions to different objectives. The decision to implement Link Aggregation or higher speed transmission links satisfy very different objectives. Take Link Aggregation for example, this is a solution which provides linear increases in bandwidth using the previously standardized Ethernet speeds, for example multiple 100 Mbps links while IEEE 802.3 was in the process of standardizing the next speed, e.g. 1 GE. The simple fact that technology costs drop as

technology matures and volumes increase tells us that implementation cost associated with 10 GE will drop below the cost of ten single GE links. Mr. Haddock also points out that when the cost per Mbps of 100 'vs' 1000 became roughly equal there was in Steve's terms, a "sweet spot" that showed approximately 4 links were ideally aggregated. Otherwise the solution became ridiculous to do more and more redundant links; somewhere between 4 & 8 links is the usual answer. Link Aggregation of ten 100 Mbps links was never intended to be a 1 GE solution, it was meant to aggregate multiple 100 Mbps links, nominally 4 links, this is a migration path to higher speeds and a means of provisioning parallel links for redundancy. The form-factor considerations are a critical point for getting higher density BW on a given board.

9. Economic Feasibility 10 GE

- Jens Fiedler – Infineon
- Paul Bottorff – Nortel Networks (Speaker)
- Ed Cornejo – Lucent
- Time Allocated = 10 minutes
- Start 1:43 PM
- End 4:17 PM

Presentation Highlights: Mr. Bottorff presented a cost comparison of optics based on SONET technology. The analysis (an extrapolation) shows the cost of 10 GE reaches 3x the cost of 1 GE in the year 2,003. The curve is based on declining prices for 1 GigE and moves from equal cost in 2001 (1 year before standard) to the 1/3 target in 2003 (1 year after the standard). Mr. Bottorff also stated that there will be improvements in packaging that will also reduce costs. An interesting point was made about the relative volumes of WAN 'vs' LAN PHY shipments, " WAN PHY's will out number the LAN PHYs in the early years".

- Questions/Answers:
  - Paul – I don't understand the Y axis label – should be 10 GE cost to 1 GE cost, an error.
  - Bruce – We need to clean up the relative cost comparison chart so that we don't confuse the marketplace.

10. Feasibility of 3.125 Gb/s

- Mike Jenkins - LSI Logic Corporation (Speaker)
- Time Allocated = 15 minutes
- Start 1:53 PM
- End 2:02 PM

- **Presentation Highlights:** Mr. Jenkins reported that LSI Logic's CMOS technology has clearly demonstrated technical feasibility of 3.125 Gbps transmission and he strongly recommended 'word striping' as opposed to the current byte striping proposal that requires higher clocking rates. Mr. Jenkins presented results from a demo performed with G11 GigaBlaze technology. The demo consisted of board trace distances needed in real life 10 GE implementations, and it demonstrated an error rate of 10EE-12 is achievable. Mr. Jenkins did point out that these results are only compatible with the "word striping" approach on the PCS/PMA to PMD interface and that the higher clocking rates for the "byte striping" approach would require more complex logic plus training sequences.

- Questions/Answers:
  - Has the Word Striping Proposal been proposed yet, answer wait ten minutes.

11. Word Striping on Multiple Serial Lanes

- Mark B. Ritter - IBM (Ritter)
- Albert X. Widmer - IBM
- Mike Jenkins - LSI Logic
- Time Allocated = 20 minutes
- Start 2:02 PM
- End 2:33 PM

- **Presentation Highlights:** Mr. Ritter began by stating that 'Word Striping' simplifies deskewing on both the serial and media interfaces. This approach would change the insert/delete granularity to 1 word as compared to the current byte striping methodology. This word striping proposal requires that commas be placed in the same byte position from word to word, this gives synchronization in each and all Lanes. Synchronization is independent of the number of Lanes. Mr. Ritter explained that no special training sequences or protocol would be needed to deskew and that this proposal is useful to High Speed Ethernet as well as Fiber Channel technology. Lane-to-Lane skew seems to be eliminated with this proposal. The concept of insertion and deletion would now be done on a granularity of words as opposed to bytes; this is accomplished at the FIFO and would be programmable via MDIO/MDC interface. It is assumed that disparity recalculation at a word rate is not too complex. A set of hardware clocks can be used to eliminate skew, simple clocking and latching is used. This solves the long term DC shifts that will be exhibited in the current KKKKRRRRR proposal.
- Questions/Answers:
  - Bob – how do you handle data ending on an odd number? Answer fill in with control characters other than comma characters.
  - You don't have just 12 bytes in the IPG, isn't that a problem? Answer: There is a way to maintain an exactly 12 byte IPG with the word-based striping. However, since Howard Frazier's MII update shows start-of-frame alignment on Byte 0, this forces a variable IPG from 12 to 15 bytes for either byte or word based striping.
  - Ethernet is byte based, and you are word based. Is that a problem? Answer: Word striping can present data to the MAC/PLS interface with exactly the same orientation and granularity as byte striping, so the two schemes are equivalent as far as Ethernet is concerned.
  - Isn't word striping more complicated, requiring more gates? Answer: In circuits like these, the simplicity of having a hard-wired word-rate clock is highly desirable. In this way, there is no comparison of data across lanes to deskew- it comes automatically. In the byte case, the complexity is actually greater in the high-speed clock domains nearer the front of the deserializer, and that is not the best point to begin a design which should be high yield and low power.
  - Where do you do disparity checks? Answer: We do them where the words are deserialized and deskewed with a 4 byte wide checking circuit, and, with slightly less gates than the byte based scheme, we can check disparity and/or recalculate it for serial transmission. As mentioned, the KKKKRRRR sequences resulting from serialization of the present Hari coding sequence would yield DC shifts due to the

RRRR sequence having a greater area above (for +R) or below (for -R) the zero disparity line when looking at the trellis diagram.

12. 10 GE OC-192 Compatible Serial Framing Proposal

- Frederick Weniger - Vitesse (Speaker)
- Time Allocated = 15 minutes
- Start 3:00 PM
- End 3:17 PM

- **Presentation Highlights:** Mr. Weiniger went through the pluses and minuses of six serial LAN & WAN PHY options, discussing the trade-off of implementation decisions in CMOS. The final option, "10 GbE WAN Interface Proposal B" or SONET Lite was suggested. The pluses are low ASIC pin count, maximizes intra board distances, single fiber and source required, provides OC-192 compatible serial, multiple vendors, standard I/F's, no clock to ASIC, and maximizes use of CMOS, whereas the only negative identified was additional logic required. This proposal includes a CMOS SONET Framer. The table below summarizes Mr. Weniger's views of all six proposals.

	Pluses	**Minuses**
Vitesse's 1st 10GbE Proposal	- easy SerDes design - best fit with 8B/10B - one size fits all	- higher ASIC pin count - sync bus speed pushes CMOS limit - LAN & WAN needs diverge
10 GbE Parallel Optics	- CMOS compatible - low cost for short distances - VCSEL optics	- high signal skew - higher cost for long distances - single point of failure
10 GbE WDM	- low ASIC pin count - low fiber cost - VCSEL optics	- high signal skew - multi-vendor availability???
10 GbE Serial LAN	- low ASIC pin count - maximizes intra-board distances - single fiber & source required	- high serial rate, not CMOS - decode & re-encode required - market potential unknown
10 GbE WAN Interface Proposal A	- minimizes logic between - XGMII & serial - provides OC-192 compatible serial - single fiber & source required	- high pin count ASIC - two sync buses required - layout difficult
10 GbE WAN Interface Proposal B	- low ASIC pin count - maximizes intra-board distances - single fiber & source required - provides OC-192 compatible serial - multiple vendors, standard I/F's - no clock to ASIC - maximizes use of CMOS	- additional logic required

13. 10 GigE SerDes Interface

- Iain Verigin - PMC-Sierra (Speaker)
- Bjorn Liencres - Juniper
- Paul Bottorff - Nortel Technologies
- David Martin - Nortel Technologies
- Gary Nicholl - Cisco
- Mike Salzman - Lucent Technologies
- Tom Palkert - AMCC
- Bill Woodruff - Giga
- Fred Weniger - Vitesse

- Time Allocated = 20 minutes
- Start 3:18 PM
- End 3:28 PM

- **Presentation Highlights:** Mr. Verigin focused on leveraging an OIF developed electrical interface, and therefore the reuse of technology, e.g. optical modules that include SerDes developed for OC-192 speeds. This OIF work is taking place in the OIF Physical & Link Layer Working Group. This OIF effort should be given careful consideration by HSSG because there are no other standards bodies attempting to define a universal interface between Framers and SerDes technology and the HSSG will leverage SONET/SDH technology for the WAN PHY. This SerDes interface is positioned between the PHY and PMD, connecting an OC-192 Framer to and OIF compatible OC-192 SerDes that could be contained in the PMD transceiver. This electrical interface includes 36 differential pairs (16 each transmit & receive, 1 each transmit & receive clocks, 1 transmit source clock and 1 reference clock). This is a point to point unidirectional interface utilizing source-synchronous clocking. One disadvantage over the current Serial interface is the distance limitation, e.g. 20 inches 'vs' a few inches.
- Questions/Answers:
  - Comment - there is a distance disadvantage (few inches compared to 20 inches) as compared to he Hari proposal.
  - There was a concern that the speed of the differential signaling would be a problem, Iain thought it was do-able.

14. Serial LAN PMD Architecture Options

- Henning Lysdal - GiGA (Speaker)
- Time Allocated = 20 minutes
- Start 3:29 PM
- End 3:42 PM

- **Presentation Highlights:** Mr. Lysdal's presentation attempts to narrow the focus of a few serial LAN PMD options. The first option discussed was the 12.5 Gb/s line rate with the popular 8B/10B, this option is closest to the current 1000Base-X standard and implies that a silicon germanium (SiGe) SerDes and optics must be developed. Mr. Lysdal estimated a long time to develop prototypes for this option, in the 2Q00 time frame, and that this option is only applicable to the LAN PHY. The second option discussed was the 10.000 Gb/s data rate option with a new scrambler and existing SerDes technology acquired from the SONET/SDH technology space. Mr. Lysdal felt this would be easier to prototype over option 1. A decision to be made is the width of the SerDes (10 'vs' 16 bits), the 16 bit interface leverages existing SONET devices. The third option, "No CMOS in PMD" seems to be a non-option at this time because it restricts PCB trace lengths and includes the difficulty of developing a 12.5 Gb/s SerDes. The presentation concluded with a narrowing of scope to options one and two and a statement of the major differences between them.

15. Packet-Over-SONET (POS) A Technical Primer

- Gary Nicholl - Cisco Systems (Speaker)
- Time Allocated = 30 minutes
- Start 3:40 PM

- End 4:17 PM

- **Presentation Highlights:** Mr. Nicholl continued his POS education series with another informative pitch on various POS fundamentals. The synchronization slide points out that POS Switch / Router line cards will require a standby oscillator used to clock the transmit data when the receive path drops out from the SONET/SDH cloud, in that case the line card still wants to transmit OAM messages. The main point here is that the synchronization requirements for POS/EOS interfaces on switch/routers are much simpler than for traditional SONET ADMs. Each POS/EOS link in the network can be independently timed, and, unlike in a SONET network, there is no requirement to synchronize all POS/EOS links to a common Stratum 1 network clock. There is therefore no requirement to have an external network timing reference input on the switch/router and each line card/port on the switch/router can run off an independent and local PHY clock. If the POS/EOS interface is connected to a SONET ADM the local PHY clock can be derived from the received OC-N signal (sometimes called 'line timing'). In this case a local 20ppm standby oscillator is also required to take over in case the received OC-N signal should fail. If the POS/EOS interface is connected to a DWDM network then the PHY clock is not derived from the DWDM network, but is instead sourced from a local 20ppm oscillator (this is sometimes called 'internal timing' or 'source clocking'). A Stratum 1 clocks are accurate to better than 0.00001 ppm, the 20 ppm clock suggested above is similar in accuracy to a Stratum 4, which has an accuracy of 32 ppm. The jitter considerations are much more stringent for the DWDM/Optical Network environment than for the traditional SONET/SDH Network. Mr. Nicholl also stressed the importance of the SONET Framer interface, a 16 bit 622 Mbps LVDS as specified by the OIF99.102 standard. Two fiber options were highlighted, the short and intermediate reach (SR/IR) utilizing SMF supporting distances of less than 80km and the 12 strand parallel MMF option for very short reach (VSR) applications requiring distances less than 500 meters. The POS network model shown indicates that POS solutions connect to both SONET Networks via Add Drop Multiplexer (ADM) or to a DWDM Optical Network via a Transponder. This is true for rates up to OC-48. However at OC-192 it is a little different in that none of the current generation of ADMs support OC-192 tributary interfaces and therefore OC-192 POS/EOS interfaces have to connect to DWDM (typically via a transponder). Mr. Nicholl defined the transport and path overhead bytes used by POS, by inspection one notices that this is in slight conflict with the proposed overhead bytes as defined by the “Proposal for a 10 Gigabit Ethernet WAN PHY” from Nortel and AMCC. The differences are slight but worth noting here. The POS overhead usage includes the B2 and M1 bytes whereas the recently posted Nortel/AMCC document does not require these bytes. The B2 provides error monitoring for the previously transmitted/received STS-1 frame, similar to B1 except it is used to keep track of just the line overhead parity. The M1 byte is a counter used to propagate the BIP-8 (B2) "line overhead parity" error counts back to the source of the errors, OC-1 links use M0 (4 bits), OC-N (e.g. OC-192) links used M1 (8bits). Another observation worth noting is the lack of focus to date on the K1/K2 Line overhead bytes. These bytes are used for APS (K1, K2) - Automatic Protection Switching. Perhaps we can persuade Mr. Nicholl to include a detailed discussion of APS in his continued POS educational series at the up coming interim meeting in

Dallas, Texas? An APS discussion might include detailed discussions or a strawman for the APS support required of HSSG compliant WAN PHY based products:

- Questions/Answers:
  - Jonathan – why didn't you make any specific recommendations in your proposal? Since Gary was asked, he stated his opinion, which was to just comply with the SONET jitter specifications, Gary doesn't quit understand why we're considering a SONET Lite proposal.
  - Roy – Commented that fault tolerance (APS) is not required on 10GE interfaces.

16. Low Overhead Coding Proposal for 10 Gb/s Serial Links

- Rick Walker - Agilent Technologies
- Richard Dugan - Agilent Technologies (Speaker)
- Time Allocated = 20 minutes
- Start 4:18 PM
- End 4:40 PM

- **Presentation Highlights:** Mr. Dugan's stated goals are to provide a full 10 GE BW for LAN applications at distances of 10km – 40km, compliant with Hari and compatible with existing Sonet lasers. Mr. Dugan claims there is a barrier (technology limit) for designs above 10 Gbaud and that efficient serial coding is the key to high data rates when using mature technologies. Different technology should be applied for the four basic HSSG distance requirements, see table below. Systems in the future will grow with parallelism, with serial links in the 2-4 Gbps range. The more efficient code being proposed uses a limited number of control characters (K, R, S, T, E …) Richard described all the coding scheme possibilities, such as pure data frame and mixed data and control frames. This coding proposal is DC balanced uses a self-synchronizing scrambler, which can be parallized allowing implementers to shift in 64 bits at a time. Maximum run length is guaranteed to be 64 bits with a 3% overhead. This could be used in the 4-color WDM, parallel fiber, 0.5 meter chip-to-chip, card-to-card, etc.

Distance	Solution Approach
0 – 10 meters	10G Serial Copper
0 – 100 meters	Parallel Optics
5 meters – 10 km	WDM 4x3.125G
10km – 40km	10G Serial Fiber

17. Duobinary Coding for 10 GE

- Greg Copeland – IDT (Speaker)
- Bertan Tezcan – IDT
- Time Allocated = 20 minutes
- Start 4:41 PM
- End 4:54 PM

- **Presentation Highlights:** Mr. Copeland also presented another coding scheme called Duobinary and claimed ease of implementation. The basics were discussed and experimental results shown. The Duobinary coding is a minimum bandwidth signal with high tolerance to chromatic dispersion. An acceptable BER and very long

distances are obtained when this coding technique is used along with forward error correction, such as Reed-Solomon (255, 239) which is an ITU standard.

18. Jitter Considerations of MB810

- Changoo Lee - ETRI (Speaker)
- Dae Young Kim - Chungham Nat'l Univ
- Kyung Gyu Chun - ETRI
- Hae Won Jung - ETRI
- Hyeong Ho Lee - ETRI
- Time Allocate = 20 minutes, Start Time = 4:57PM, End Time = 5:13PM

- **Presentation Highlights:** Mr. Lee gave an update on their MB810 coding, this time focusing on simulations to determine jitter performance and found that MB810 has a good relative jitter performance over NRZ and 8B/10B. This time around they also implemented the MB810 successfully in an FPGA and stated that this means a low-cost high-speed custom chip can be built.

19. 10 GE Fiber Optic Links – Link

- David Dolfi - Agilent Laboratories (Speaker)
- Time Allocated = 15 minutes
- Start 9:43 AM
- End 9:55 AM

- **Presentation Highlights:** Mr. Dolfi's brief link model update focused on three items, they were mode partition noise (MPD), narrow line width, chirped laser sources, and optical cross talk in WDM systems. Mr. Dolfi also outline several other areas for further investigation. When modeling MPD the gaussian approximation is OK for some sources but not all, e.g. VCSELs, but not for DFB lasers with finite side mode suppression. A new MPN penalty expression was discussed, it can easily be added to the current spreadsheet. David made some progress on the narrow line width chirped sources but is not ready to add this to the spreadsheet yet, more investigation is needed. A numerical example was shown that has good agreement with the gigabit optical link designer (GOLD) simulation. The power penalty resulting from cross talk from adjacent channels is also a topic for further study. Modifications due to RIN may be coming as well. In summary there are a number of potential modifications underway for the fiber optic spread sheet link model.
- Questions/Answers:
- Jonathan - Has any work been done for DMD effects, the concern here is that in the past the DMD work was done for MM lasers. While DMD shouldn't be significantly different between a single mode DFB and a multi-mode FP edge emitter (since it's the spatial rather than the temporal mode structure of the laser which matters), there may be an issue with modal noise, due to the higher coherence (and corresponding higher speckle contrast) of the DFB.

20. Preliminary Serial PMD Proposal for HSSG

- Len Young - Corning
- Vipul Bhatt - Finisar
- Peter Pepeljugoski - IBM
- Schelto Van-Doorn - Infineon
- Ed Cornejo - Lucent Microelectronics (Speaker)
- Paul Kolesar - Lucent Network Products
- Zbigniew Felczak - Mitsubish Electronics
- Joel Paslaski - Ortel
- Russ Patterson - Picolight
- Jim Yokouchi - Sumitomo Electric
- Atikem Haile-Mariam - Tyco Electrics
- Mark Donhowe - W.L. Gore
- Time Allocated = 15 minutes
- Start 9:56 AM
- End 10:10 AM

- **Presentation Highlights:** Mr. Cornejo began this presentation by detailing eight Serial PMD evaluation criteria, for example working prototypes and multi vendor supply available by completion of Sponsor ballot. The key objectives for the serial solutions is low cost, another key feature is industry support. To this point Mr. Cornejo identified eight 10 G transceiver vendors. Time to market is very important too and they feel they will be ready for year 2000 with product supporting ranges of 65 meters (100 m is better!) to 40km, with FP, VCSELs, and DFB sources. This group prefers connectorized modules however due to EMI concerns a pigtail may be required at 10 GE. For field replacement they want to support hot pluggable modules. The integration of SerDes is under consideration but the pin count is a concern. In the 40km range there are two windows under consideration, 1300/1550 nm. They showed a preliminary transmit and receive power budget analysis for SMF & MMF source types that included line rate, wavelength, response time, spectral width, side mode suppression ration, launch power, and extinction ratio. They are now focusing on Hari considerations. They intend to leverage new developments in the SR(2km) and VSR(<500m) OC-192 applications.
- Questions/Answers:
  - We can not allow 20 different PMD proposals to go forward in the standard, so over time we'll narrow down the list of options. A question was asked about the 65 meter range, why not 100 meters, the group will address this over time to meet the distance goal of 100 meters.

21. Serial 12.5 Gbaud, 10 km SMF Serial 12.5 Gbaud, 10 km SMF Link with Clock and Data Recovery with CDR IC

- John Crow - IBM (Speaker)
- Dan Kuchta - IBM
- Mounir Meghelli - IBM
- Petar Pepeljugoski - IBM
- Israel Ury - Ortel
- Time Allocated = 20 minutes
- Start 9:11 AM
- End 9:28 AM

- **Presentation Highlights:** Mr. Crow's presentation focused on a low cost (due to SiGe/CMOS) serial 10km PMD transceiver that uses transceivers from multiple sources and included experimental results from a recent prototyping effort. The prototype was stressed, for example IBM ran the transceiver a 13Gbaud and beyond the 10km requirement, to 14km. In this experiment an IBM integrated circuit including a SiGe BiCMOS CDR and Ortel's DFB laser source and PD receiver. The prototype ran fine at 13Gbps and a distance of 14km. The Ortel DFB laser was used with 5 different bias conditions to enhance the deterministic jitter in the system. The experiment attempted to use transmitter and receiver characteristics that match the current tentative specification. Mr. Crow's experiment did not focus on power budgets but did focus on jitter considerations. These results are initial findings that will evolve over the coming months. Deterministic jitter results at the 4 test sites, TP1,2,3,4 show that beyond 30 ps jitter the BER gets down to the 10EE-9 range. The implications of this piece of work show that 12.5 Gbps signaling rates are feasible and current production optics can be used and IBM's SiGe BiCMOS can be used.
- Questions/Answers:
  - What is the approximate power consumption of the CDR. In the range of a few hundred mW.
  - What temperature range was used. Normal room temperature.
  - Was a directly modulated laser used. Yes.

22. Optical Components for 12.5 Gbaud Serial Links

- Al Benzoni - Ortel
- Thomas Schrans - Ortel
- Bryon Kasper - Ortel
- Charles Tsai - Ortel
- Joel Paslaski - Ortel
- Israel Ury - Ortel (Speaker)
- Time Allocated = 20 minutes
- Start 9:30 AM
- End
- **Presentation Highlights:** Mr. Ury began by explaining why serial links are important to HSSG, for example the serial PMD consortium has significant support, and that existing technology can be applied, only requires a single fiber, etc. A directly driven DFB laser would be used requiring about 40 mA drive current. Cost differences between DFB's and FP's is not too great. The DFB lasers were picked because they have no mode partition noise penalty, no dispersion penalty, and they are standard components operating in the 1300 nm window and extendable to the next window for greater distances. From a temperature point of view you don't see a laser frequency roll off until you get to 65 degree C. At room temp can put out 30 mW. The laser spectrum over temp shows that you can get 40 dB SMSR. PIN based receivers were picked for the broad range of link design goals, not to mention the maturity of this technology. Mr. Ury's conclusion is that DFB transmitters and PIN receivers are more than adequate for 12.5 Gbps rates.
- Questions/Answers:
  - What are the effects of lower temps, show be OK.

23. Design of 300 Meter Installed 62.5 um Fiber for Longwave 10GbE

- Edward S. Chang - NetWorth Technologies, Inc. (Speaker)
- Time Allocated = 20 minutes
- Start 10:15 AM
- End 10:40 AM

- **Presentation Highlights:** Mr. Chang's presentation on reaching a 300 meter link distance over the installed base of 62.5 um fiber centered around discussion of three link parameters, i.e. jitter budget, power budget, and bandwidth budget. Mr. Chang stated that the first two, jitter and power, are not critical because they are controlled or assigned by the system designers. The fiber BW budget however is the critical factor, installed fiber is not within our control. Ed showed the results of a TIA cable study and stated that the use of either Offset or Circle Mode Conditioning is required to improve BW to an acceptable level (e.g. 750 MHz-km) for 10 GE signaling. Some small percentage of fibers showed excessive DMD where no BW improvements could be made, in this case Mr. Chang suggested discarding those fibers.

24. 300 Meters on Installed MMF – Architecture, BERs and RINs, Link Simulations, Coding Gain

- Jaime Kardontchik - Micro Linear (Speaker)
- Stefan Wurster - Micro Linear
- Time Allocated = 1 hour
- Start 10:42 AM
- End 11:25 AM

- **Presentation Highlights:** Mr. Kardontchik compared 3 architectures that have been proposed for installed MMF in terms of ISI loss, noise, SNR and delay skew. Then he presented a detailed analysis and complete link simulations of the architecture using PAM-5 + 4-WDM at 1.25 Gbaud/sec. The main conclusion was that this architecture is an attractive alternative to reuse the installed base of multimode fiber and, in addition, it has the advantage that reuses the PCS of an existing 802 standard, 1000BASE-T, saving valuable 10 GbE standard development time. The 300-meter range provides best coverage for the installed MMF. This presentation analyzes several architectures that support 300 meters, all architectures use PAM-x with signaling rates ranging from 1.25 – 5 GB/s. The ISI loss is lowest for the 1.25GB/s PAM-5 + scrambling + 4-WDM option at 300 meters. Receiver input is a PIN Photo Diode. Mr. Kardontchik showed the small signal receiver front end model which was used to stress that a smaller feedback resister is needed to improve the BW. When we go from 1.25 GB to 3.125 GB we are paying an 8dB penalty due to the thermal noise because the noise is proportional to the square of the BW. There is a 3dB advantage in the SNR between the 1.25 and 3.125 Gbaud rates. The analysis shows that two of the three architectures will work, if we stay with the familiar 8B/10B + 4-WDM at 3.125Gbaud/s we can support up to 200 meters, however 300 meters can be achieved with the PAM-5 + 4-WDM @ 1.25 Gbaud/s architecture if used with coding gain described by Jaime. A complete system simulation was performed to validate the

theory. This simulation showed an eye opening even at 500 meters using PAM-5 @ 1.25Gbaud/s even thought this is not recommended as a specification.

25. VCSEL Based Solutions for 10 Gigabit Ethernet

- Mark Donhowe - W.L. Gore & Associates
- Richard Kriese - W.L. Gore & Associates (Speaker)
- Time Allocated = 10 minutes
- Start 1:00 PM
- End 1:20 PM

- **Presentation Highlights:** Mr. Kriese's presentation discussed both short and long wavelength 10 GE VCSEL technologies. VCSEL characteristics such as output power 'vs' current and response 'vs' frequency, eye diagrams at 1, 300, and 600 meters were shown. Mr. Kriese stated short wavelength VCSEL solutions for 10-by-1.25 Gbps, 4-by-3.125 Gbps, and 1-by-12.5 Gbps are all possible. The short wavelength four channel parallel solution has been demonstrated to 300 meters using higher BW GE fiber and the short wavelength serial solution was demonstrated to 500 meters also using high BW fiber from Corning and Lucent. Mr. Kriess concluded by saying both short and long wavelength VCSELs are feasible for 10 GE applications and the long wave solution may satisfy both the 2km and 10km link distance requirements.

26. Wide Wavelength Division Multiplexing (WWDM) Interface Specification Proposal For 10 Gb/s Ethernet Fibre Optic Link

- Del Hanson - Agilent Technologies (Speaker)
- Time Allocated = 20 minutes
- Start 1:20 PM
- End 1:45 PM

- **Presentation Highlights:** Mr. Hanson took the group through some clause 38 extensions for 10 GE WWDM. The new issues deal with multiple (4) wavelengths & DFB's specifically wavelength separation, tolerances and cross talk, and DFB SMSR. New clause 38 tables that specify 10 GE operating range, transmitter characteristics, receiver characteristics, worst case link power budget and penalties, and jitter were discussed including consideration for the new Hari jitter proposal. A re-timer function is needed to improve the eye opening from 0.35 UI at the end of the back-plane/board (20") run to 0.75 UI at the input to the Optics. These updated clause 38 tables, proposed interface specification are based on technology that exists today. Over the next six months or so further work is required to refine some parameters
- Questions/Answers:
  - Roy – clarify the Hari model. It is a common interface that we can use to quickly get all the components underway.
  - Hon – How did you allocate the WWDM Budget? It is on a wavelength by wavelength basis.

27. Multilevel Serial PMD Update

- Rich Taborek – Independent (Speaker)
- Time Allocated = 30 minutes
- Start 1:45 PM

- End 2:13 PM

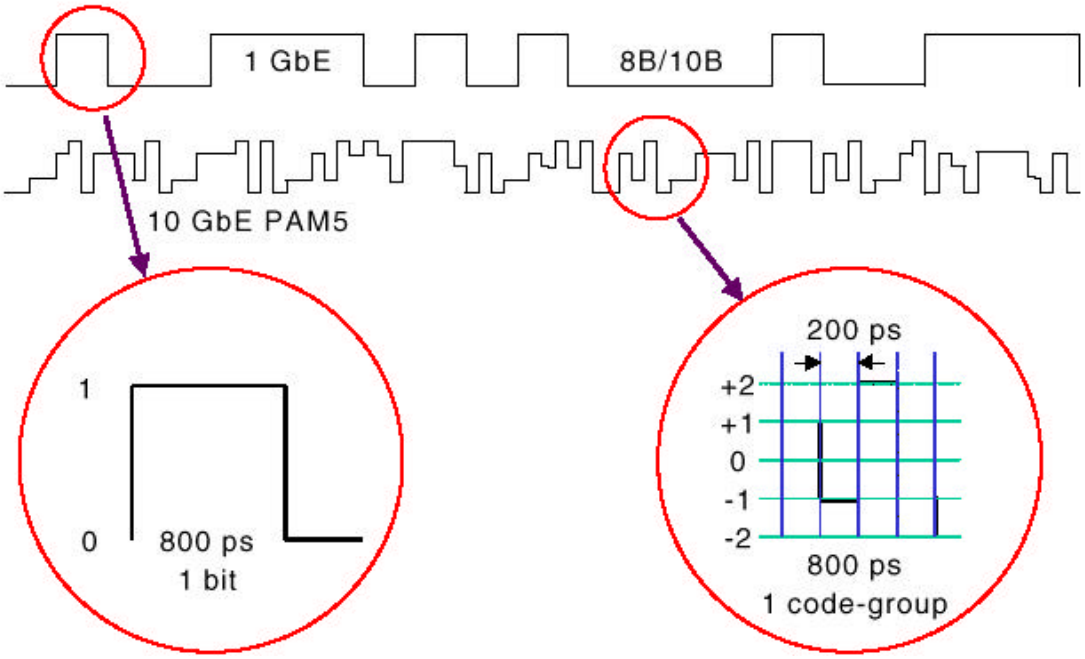
- **Presentation Highlights:** Mr. Taborek recently stated "*I have proposed what I believe to be the simplest multilevel modulation scheme for the 10 Gbps data transport. The tradeoffs are simple: Cut the line rate by 1/2 and use 5 levels. Of course this results in SNR penalty of 4.1 dB optical, but this penalty can be easily recovered by other tradeoffs in a multilevel optical system including intelligent closed-loop full-duplex link design, Forward Error Correcting FEC code, careful engineering to minimize laser noise (e.g. RIN, etc.). All of these techniques are well known and/or straightforward and used in most existing communications links*". The big cost saving from usage of MAS comes from the 50 % reduction in line rate. MAS will require CMOS in the transceivers, but this will have benefits such as increased link distances, supporting installed base of fiber up to 200 meters, and makes it easier to comply with EMI. This is the only PMD option that meets all HSSG distance requirements. Since we need 1 vs 4 lasers the reliability should be better. There is no intellectual property associated with this scheme. This is an encoded signal of five levels, called PAM5x4. The additional encoding that could be used is FEC coding gain, e.g. Reed-Solomon giving a 10X order of magnitude improvement in BER. The PAM5x4 coding structure includes a total of 625 codes. Circuit design challenges include waveform synthesis and capture, CDR for Hari and PAM5, plus FEC. Some architectural views were shown that specify where MAS is implemented, e.g. PMD coding & signaling sub-layers. One key point is that PAM and MAS are not new to Ethernet because PAM was used in 100BaseT2/T and multi-level coding used in 100Base-TX/T4. Although auto-negotiation is not required for the startup procedure it was picked here to perform a calibration of the MAS Transmit power and Receive levels. Reference the diagram below for a visual of the MAS signaling as compared to 1 GE.
- Mr. Taborek also recently stated that, "*The principal thrust behind multilevel optics is to cut the cost of an optical transport which has very high data rate requirements. The IEEE 802.3 HSSG has now heard of at lease 4 general options to do this:*

  1) Reduce to cost of serial binary signaled systems by several orders of magnitude (e.g. 1 bit/baud such as OC-192);

  2) Demultiplex the data by a factor of N for transport across N individual optical links (e.g. parallel optics);

  3) Demultiplex the data by a factor of N for transport across N wavelengths using N O/E sets and a single optical links (e.g. WWDM);

  4) Encode the data into multiple bits/baud or multiple subcarriers for transport across a single serial link (e.g. PAM, QAM, FSK, etc.)."



28. 10 Gigabit Ethernet WAN PHY Alternatives

- Norival Figueira - Nortel (Speaker)
- Time Allocated = 15 minutes
- Start 2:14 PM
- End ??? PM

- **Presentation Highlights:** Mr. Figueira began by stating three HSSG objectives tied to the 10 GE WAN PHY standardization. Four 10 GE WAN PHY alternatives/architectures were discussed very briefly, the 8B/10B, MB810, one polynomial scrambler, and two polynomial scrambler. There are some additional proposed objectives, like same OC-192 line frequency, same SONET/SDH frame format, minimum line, section, and path overheads, operates without an isochronous clock. Mr. Frigueria and Mr. Bottorff posted an excellent white paper (strawman) for a 10 GE WAN PHY to the HSSG web page. Mr. Frigueira wrapped up by suggesting the dual scrambler be used and would like to see the objectives above added to the HSSG objective's list.

29. New MMF, How Far Can We Go?

- Giorgio Giaretta - Lucent Technologies (Speaker)
- R.Michalzik - Lucent Technologies
- P.Kolesar - Lucent Technologies
- Time Allocated = 10 minutes
- Start 2:50 PM
- End 2:58 PM

- **Presentation Highlights:** Mr. Giaretta mentioned that the work in this presentation is going forward in FO-2.2. The LazrSPEED™ stressed system configuration offsets a limited modulation BW VCSEL by +/- 5um in the XYZ axis, includes a mode scrambler, fiber shakers, offset connectors, 300 meters of MMF, an attenuator, Pin

receiver and Bit Error Rate Tester. Support at 300 meters is easily maintained even under stressed conditions. A number of differential mode delay profiles were discussed, only the new MMF exhibited a flat and narrow DMD. Some longer distances were demonstrated under less stressful conditions, bottom line, the 300 meter link length objective over MMF s is easily achieved.

30. 10 G Short Haul CU Information

- Ed Cady – Berg Electronics (Speaker)
- Time Allocated = 20 minutes
- Start 2:59 PM
- End ???? PM

- **Presentation Highlights:** Mr. Cady explained the applications for this 10 GE copper type of solution include clustered workstations, clustered servers and switches in racks, etc…. There are a number of standards efforts going on in the industry where this CU technology may be applicable, such as Fiber Channel, ATM, Sonet, as well as some value added applications. The companies that have stepped forward and expressed interest in 10 GE CU are mostly component suppliers. The CU version of Hari enabled 3.125Gbps solution can support 10-20 meters over 100 ohm cabling. A series of eye diagrams were shown for various Madison cable, for example 26 AWG TurboTwist 5 meters, a very flexible cable in high volume production. An eight differential pair plug connector was shown, METRAL HB, see presentation for details. This connector has been presented in several standards committees for both back-plane and I/O applications, plus they intend to go into IEC as well.

31. Why We Need a 10 Gigabit Copper Link

- Daniel Dove - Hewlett Packard (Speaker)
- Time Allocated = 15 minutes
- Start
- End

- **Presentation Highlights:** Mr. Dove also discussed several applications for 10 GE copper and claimed these application will demand a low cost solution than fiber based solution. The applications Dan identified are Building Server Clusters (15 – 20m), Stacking Interconnect (0.5 – 6m), and Campus Server Cluster (15-20m). Aggregation of 1000Base-T links at 2-3 X the cost of 1000Base-CX. Since InfiniBand is developing a 4x serial specification based on Hari, this work could be leverage for 10 GE CU.
- Questions/Answers:
  - Howard – Explain the low cost solution for the Server clustering. Dan said that if a customer has a choice of a $1,000+ fiber NIC over a much less expensive CU NIC and the application doesn't require the long distances supported by the fiber solution that they would go for the CU solution and save money.

Motions:

- **Motion # 1**
  - Description: Approve word changes to PAR. Request 802.3 forward to SEC and NesCom
  - Motion Type: Procedural / Technical
  - Time: 3:31pm
  - Moved By: Tom Dineen
  - Seconded By: Edward Chang
  - Results: Yes = 137, No = 0, Abstains = 0

- **Motion # 2**
  - Description: Approve the York minutes.
  - Motion Type: Procedural
  - Time: 3:40PM
  - Moved By: Tom Dineen
  - Seconded By: Walt Thirion
  - Results: Passed by Acclimation

- **Motion # 3**
  - Description: Motion to Adjourn
  - Motion Type: Procedural / Technical
  - Time: 3:43PM
  - Moved By: Tom Dineen
  - Seconded By: ?
  - Results: Passed by Acclimation

PAR – Project Authorization Request:

Project is a supplement to an existing standard (not a new standard; not an update to an existing PAR)

Target Completion date: March 2,002

Purpose: The purpose of this project is to extend the 802.3 protocol to an operating speed of 10 Gb/s and to expand the Ethernet application space to include Wide Area Network links in order to provide a significant increase in bandwidth while maintaining maximum compatibility with the installed base of 802.3 interfaces, previous investment in research and development, and principles of network operation and management.

Scope: Define 802.3 Media Access Control (MAC) parameters and minimal augmentation of its operation, physical layer characteristics and management parameters for transfer of LLC and Ethernet format frames at 10 Gb/s using full duplex operation as defined in the 802.3 standard. In addition to the traditional LAN space, add parameters and mechanisms that enable deployment of Ethernet over the Wide Area Network operating at a data rate compatible with OC-192c and SDH VC-4-64c payload rate.

Similar Scope: There is no other project that uses the 802.3 MAC at speeds above 1000 Mb/s.

FIVE Criteria:

1. Broad Market Potential

Broad set(s) of applications
Multiple vendors, multiple users
Balanced cost, LAN vs. attached stations

- Rapid growth of network and internet traffic has placed high demand on the existing infrastructure motivating the development of higher performance links. Quantitative presentations have been made to the 802.3 HSSG indicating significant market opportunity.
- 10 Gb/s 802.3 solution extends Ethernet capabilities providing higher bandwidth for multimedia, distributed processing, imaging, medical, CAD/CAM, and pre-press applications by improving the performance of:
  - LAN Backbone and Server and Gateway Connectivity
  - Switch aggregation
  - the MAN, WAN, Regional Area Network (RAN), and Storage Area Network (SAN)
- 140 participants attended the 10 Gigabit call-for-interest, representing at least 55 companies, indicate that they plan to participate in the standardization of 10 Gb/s 802.3. 139 Indicated that this is the right time to start. Attendance and interest has increased steadily since that time.
- This level of commitment indicates that a standard will be supported by a large group of vendors. This in turn will ensure that there will be a wide variety of equipment supporting a multitude of applications.
- Prior experience scaling 802.3 across the range of 1 to 1000 Mb/ s indicates that the cost balance between adapters, switches, and the infrastructure remains roughly constant. 10 Gb/s Ethernet should continue this trend.

2. Compatibility with IEEE Standard 802.3

Conformance with CSMA/ CD MAC, PLS
Conformance with 802.2
Conformance with 802 FR

- The proposed standard will conform to the full-duplex operating mode of the 802.3 MAC, appropriately adapted for 10 Gb/ s operation. Half-duplex (CSMA/CD) operation will not be supported at 10 Gb/s.
- As was the case in previous 802.3 standards, new physical layers will be defined for 10 Gb/s operation.
- The proposed standard will conform to the 802.3 MAC Client Interface, which supports 802.2 LLC.
- The proposed standard will conform to the 802.1 Architecture, Management and Interworking.
- The proposed standard will conform with the 802 Functional Requirements Document (with the possible exception of Hamming distance).
- The proposed standard will define a set of systems management objects, which are compatible with OSI and SNMP system management standards.

3. Distinct Identity

Substantially different from other 802.3 specs/ solutions
Unique solution for problem (not two alternatives/ problem)
Easy for document reader to select relevant spec

- The proposed standard is an upgrade path for 802.3 users, based on the 802.3 MAC, running at 10 Gb/s.
- By adapting the existing 802.3 MAC protocol for use at 10 Gb/s, this proposed standard will maintain maximum compatibility with the installed base of over 600 million Ethernet nodes.
- The established benefits of the 802.3 MAC include:
  – Deterministic, highly efficient full-duplex operation mode
  – Well-characterized and understood operating behavior
  – Broad base of expertise in suppliers and customers
  – Straightforward bridging between networks at different data rates
- The Management Information Base (MIB) for 10 Gb/s 802.3 will be extended in a manner consistent with the 802.3 MIB for 10 / 100 / 1000 Mb/s operation. Therefore, network managers, installers, and administrators will see a consistent management model across all operating speeds.
- Two PHY families will address two distinct application spaces, the LAN and the WAN.
- The proposed standard will be a supplement to the existing 802.3 standard, formatted as a collection of new clauses, making it easy for the reader to select the relevant specification.

4. Technical Feasibility

Demonstrated feasibility; reports - - working models
Proven technology, reasonable testing
Confidence in reliability

- Technical presentations, given to 802.3, have demonstrated the feasibility of using the 802.3 MAC in useful network topologies at a rate of 10 Gb/s.
- The principle of scaling the 802.3 MAC to higher speeds has been well established by previous work within 802.3. The 10 Gb/s work will build on this experience.
- The principle of building bridging equipment which performs rate adaptation between 802.3 networks operating at different speeds has been amply demonstrated by the broad set of product offerings that bridge between 10, 100, and 1000 Mb/s.
- Vendors of optical components and systems are building reliable products, which operate at 10 Gb/s, and meet worldwide regulatory and operational requirements.
- Component vendors have presented research on the feasibility of physical layer signaling at a rate of 10 Gb/s on fiber optic media using a wide variety of innovative low cost technologies.
- 10 Gb/s Ethernet technology will be demonstrated during the course of the project, prior to the completion of the sponsor ballot.

5. Economic Feasibility

Cost factors known, reliable data
Reasonable cost for performance expected
Total Installation costs considered

- Cost factors are extrapolated from the OC-192 component supplier base and technology curves.
- A target cost increase of 3X of 1000BASE- X with a ten-fold increase in available bandwidth in the full duplex operating mode will result in an improvement in the cost- performance ratio by a factor of 3. This cost model has been validated during both the 100 and 1000 Mb/s Ethernet deployment.
- Customers will in some cases be able to re-use fiber that has been installed in accordance with ISO/ IEC 11801, and in other existing fiber facilities.
- Installation costs for new fiber runs based on established standards are well known and reasonable.
- Network design, installation and maintenance costs are minimized by preserving network architecture, management, software, and structured cabling.