Common PMD Interface
"Hari"

IEEE 802.3 HSSG

November, 1999

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Agenda

- **Introduction**
  - Background
  - Assumptions
  - Chief Issues
  - Guiding Decisions
- **Interface Description**
  - High Speed Data I/F
  - Management I/F
- **Transceiver Support**
  - Generic Block Diagram
  - Examples
  - Power Down Modes
- **Coding Proposal**
  - Functions/Features/Rules
  - Clock Tolerance Compensation
  - Skew Budget
  - Deskew Protocol
  - Examples Usage
- **Electrical Specs**
  - High Speed I/F
  - Management I/F
- **Timing Specs**
  - Jitter; Skew
- **Summary**

Hari History

1999

- **March 9-11: 10 Gigabit Ethernet Call for Interest**; IEEE 802 Creates High Speed Study Group
- **April - June:** Various Industry Group Leaders (FC; NGIO; OIF) **Express Interest in a Common 10 Gig PMD** to HSSG Chair
- **July 22**: **OIF Adopts Motion** to Utilize 10 Gig Ethernet PHY for Future Low Cost Interconnect
- **July 30: First Meeting of the "Hari" Group**
- **Oct 7: FC begins process for a 10 Gig Project**
- **Oct 26: Fifth and Final (?) Meeting**

10 G Ethernet PHY Requirements

IEEE 802.3 HSSG has adopted these PHY related objectives:

- Family of Physical Layer specifications supporting links of:
  - At least 100 m over installed MMF
  - At least 300 m over MMF
  - At least 2 km over SMF
  - At least 10 km over SMF
  - At least 40 km over SMF
- Support both LAN and WAN
  - LAN at 10.0000 Gb/s data rate
  - WAN at 9.58464 Gb/s data rate (SONET Friendly)
  - A common MAC layer that supports both

Assumptions

- **There will be multiple 10 Gig PHY/PMD solutions**
  - A single solution can't be ideal for all distance objectives
- **There will be a PLL in the transceiver**
  - High speed media interface too fast for GBIC/1x9 style I/F
  - The system I/F to the PMD can have relatively high jitter
- **Architects desire >20" of trace between devices**
  - Desire to physically separate optical transceiver from switch matrix
  - Mitigate fan-out issues; Allow for greater flexibility
- **Designers desire a common interface PMD I/F**
  - Can't afford Vendor / PHY / PMD solution permutations
  - Desire fewest pins / highest speed signals reasonable
- **Desire for common transceiver usage across platforms (Ethernet, Fibre Channel, SIO, OIF...)**

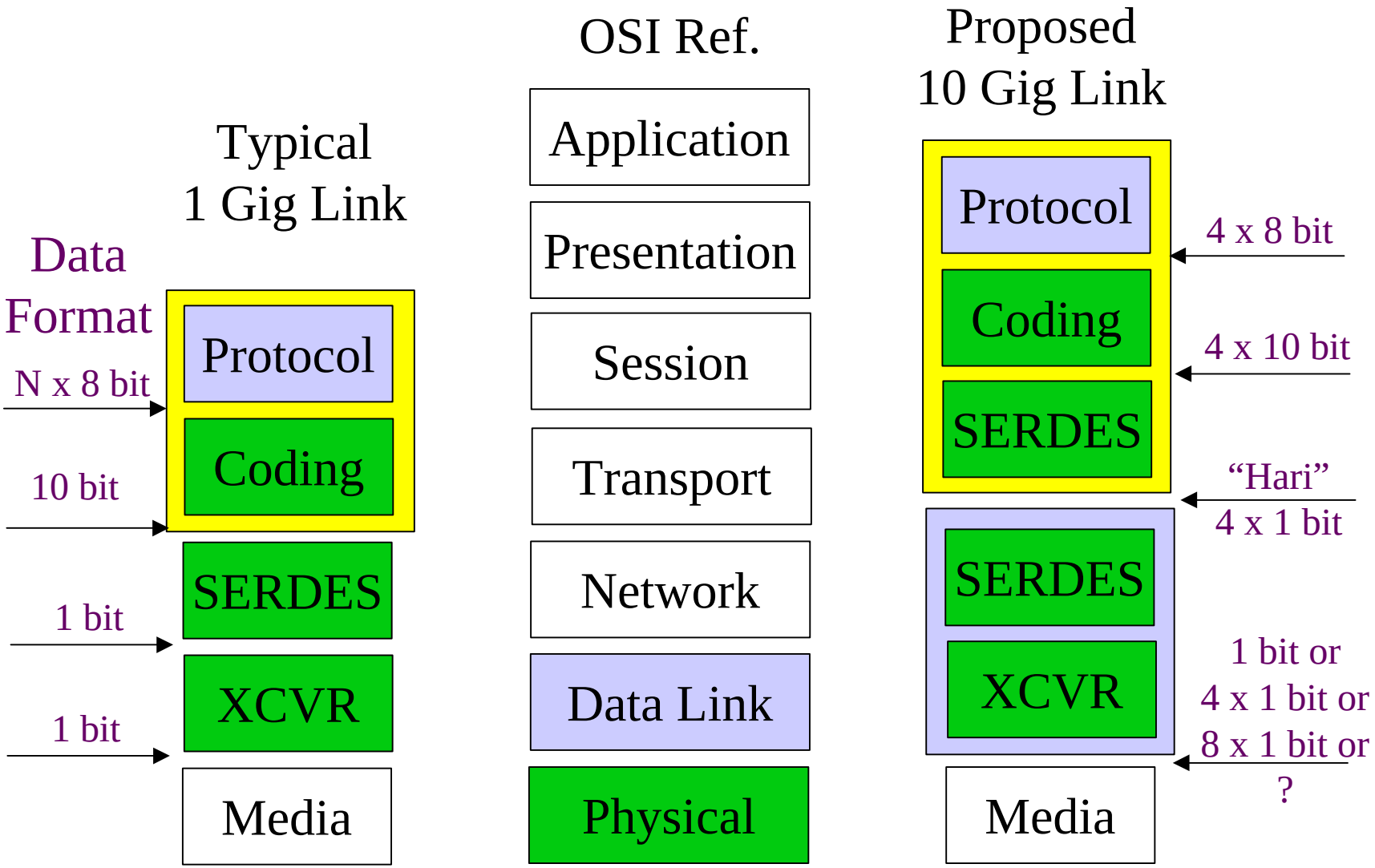
Chief Issues Addressed

- **Support multiple protocols and encoding schema**
- **Support multiple optical PMD's**
  - WDM
  - Serial
  - Parallel
  - Multilevel Amplitude
- **Layout, Timing, and Electrical Considerations**
  - Minimize Pin Count
  - Skew compensation (include media)
  - Electrical specifications
  - Data will be self clocking; jitter specifications required
  - Extension to wider interfaces
  - "Green" power down modes

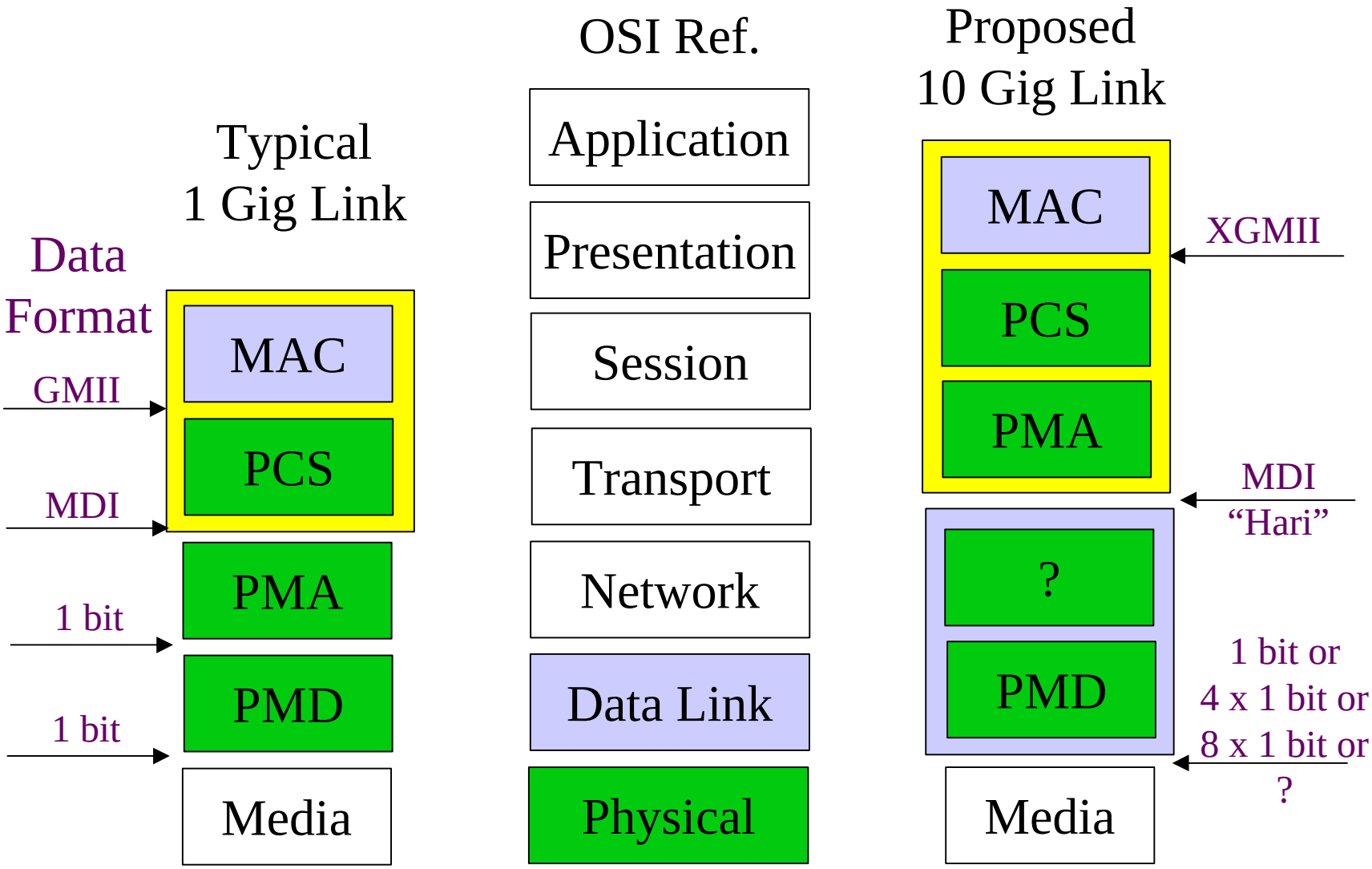
Guiding Decisions / Objectives

- **Utilize 8B/10B Code**
  - Well understood; commonly used; minimal circuit overhead
- **Relax Jitter requirements (the optics jitter budget is specified independent of Hari)**
- **Push "Protocol" Silicon to reasonable limit**
  - Future proof the architecture
  - 3.125 believed supportable as future "pure CMOS" core
- **Support distances of 18" to 24" over FR4**
  - Expect use of good design technique
- **Use techniques that avoid unnecessary IP**
- **Avoid excessive penalties for specific PHY types**
- **Use self clocking data only**

OSI Layer Stack Mapping



OSI Mapping For Ethernet

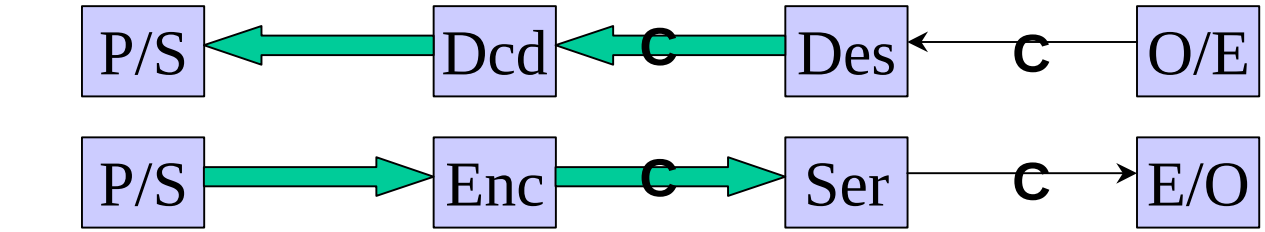


Expanded Block Diagrams (Key)

Transmit		Receive	
P/S	Protocol / Switch	Protocol / Switch	P/S
Sync	Synchronization Pattern	Deskew	Dsk
Enc	Encoder	Decoder	Dcd
Skip	Skip Insert / Delete	Skip Insert / Delete	Skip
Ser	Serializer	Deserializer (Bit/Byte Sync)	Des
E/O	Electrical to Optical	Optical to Electrical	E/O

Coded Interface

Example: 1 Gig Partitions



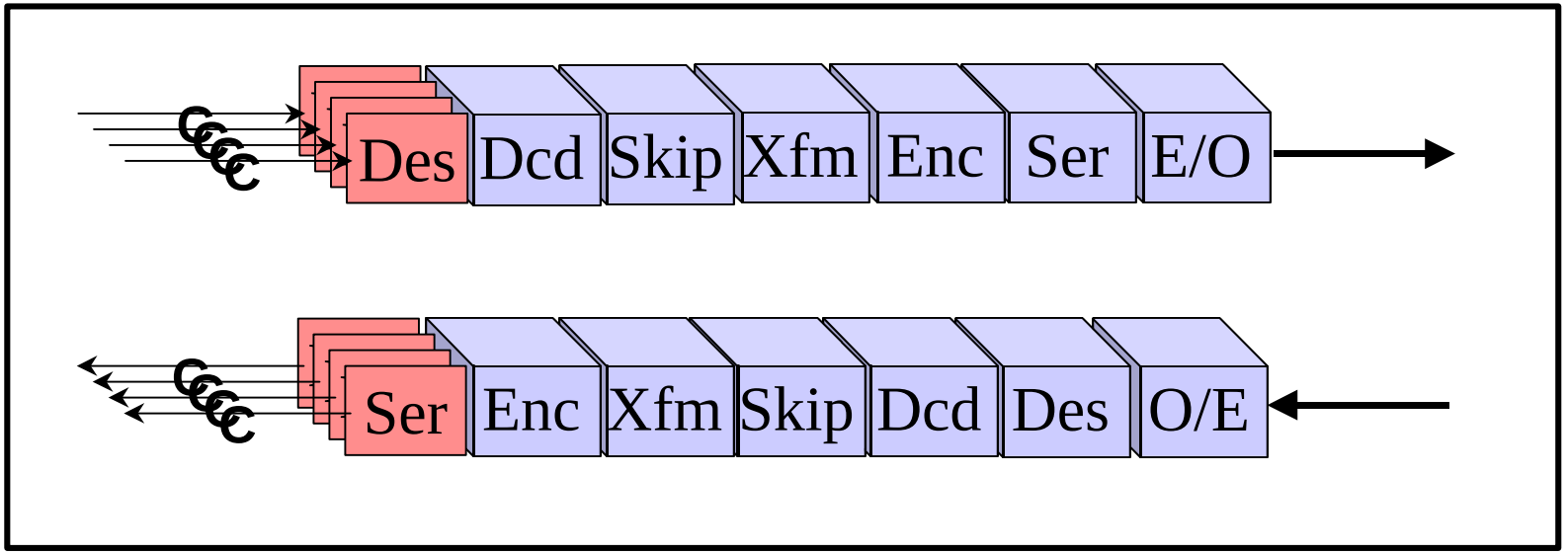
Protocol Layers:
"MAC" & "PCS";
"FC2" & "FC1"

20 "GLM"

10 "10B" 1d "1x9" "GBIC"

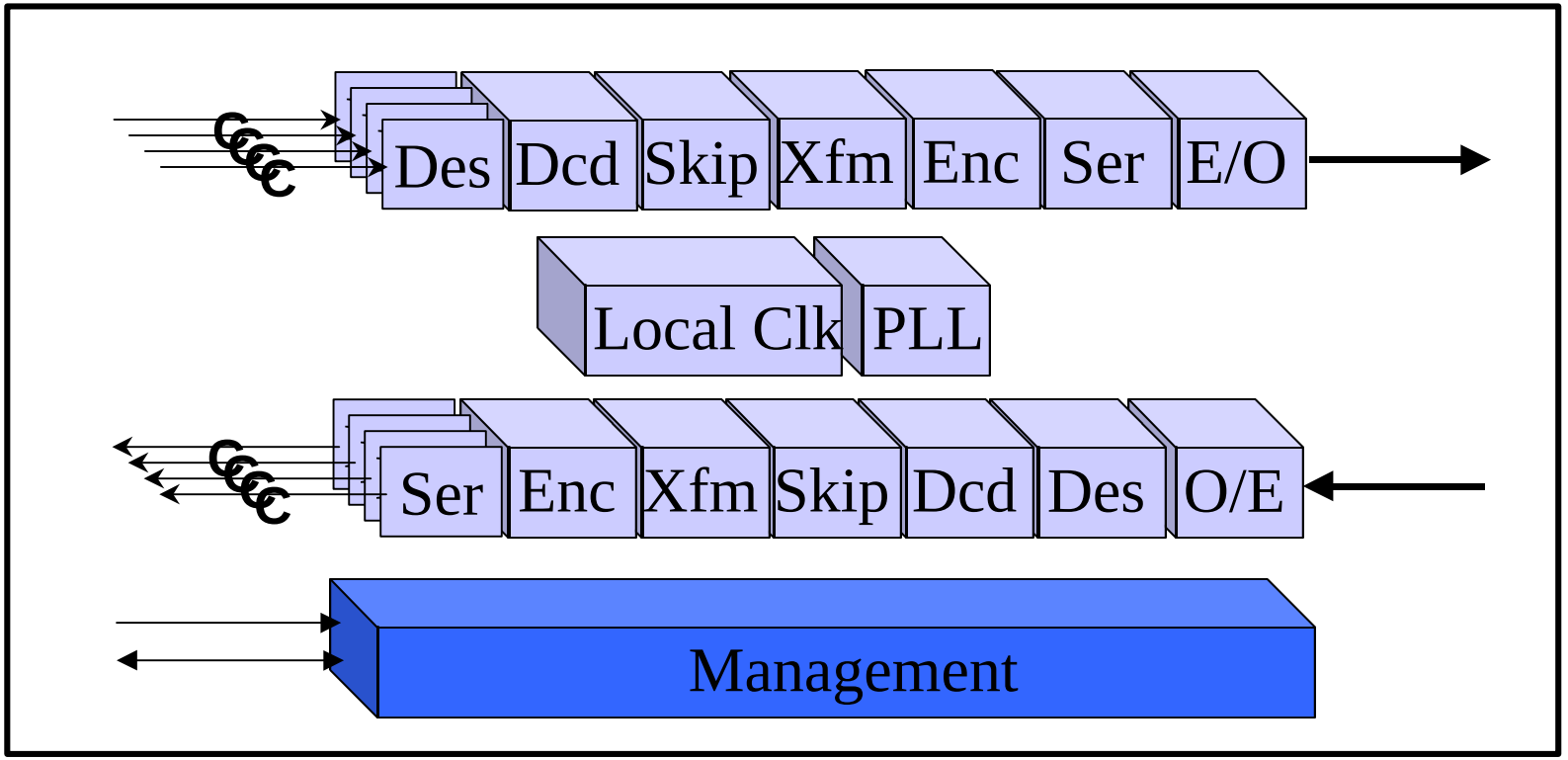
Protocol with "Integrated SERDES" 1d "1x9" "GBIC"

Generic 10 Gig XCVR Data Flow



- **Not all blocks required by all transceivers**
- **Order of functional blocks may vary**
- **Some blocks may be trivial or share functions**
  - **Deserializer and Serializer probably share PLL**
  - **Xfm might simply be a mux**
- **All Transceivers will require PLL & reclocking**
- **“Skip” Character Insert/Delete needed to correct for clock variations**

Generic Transceiver



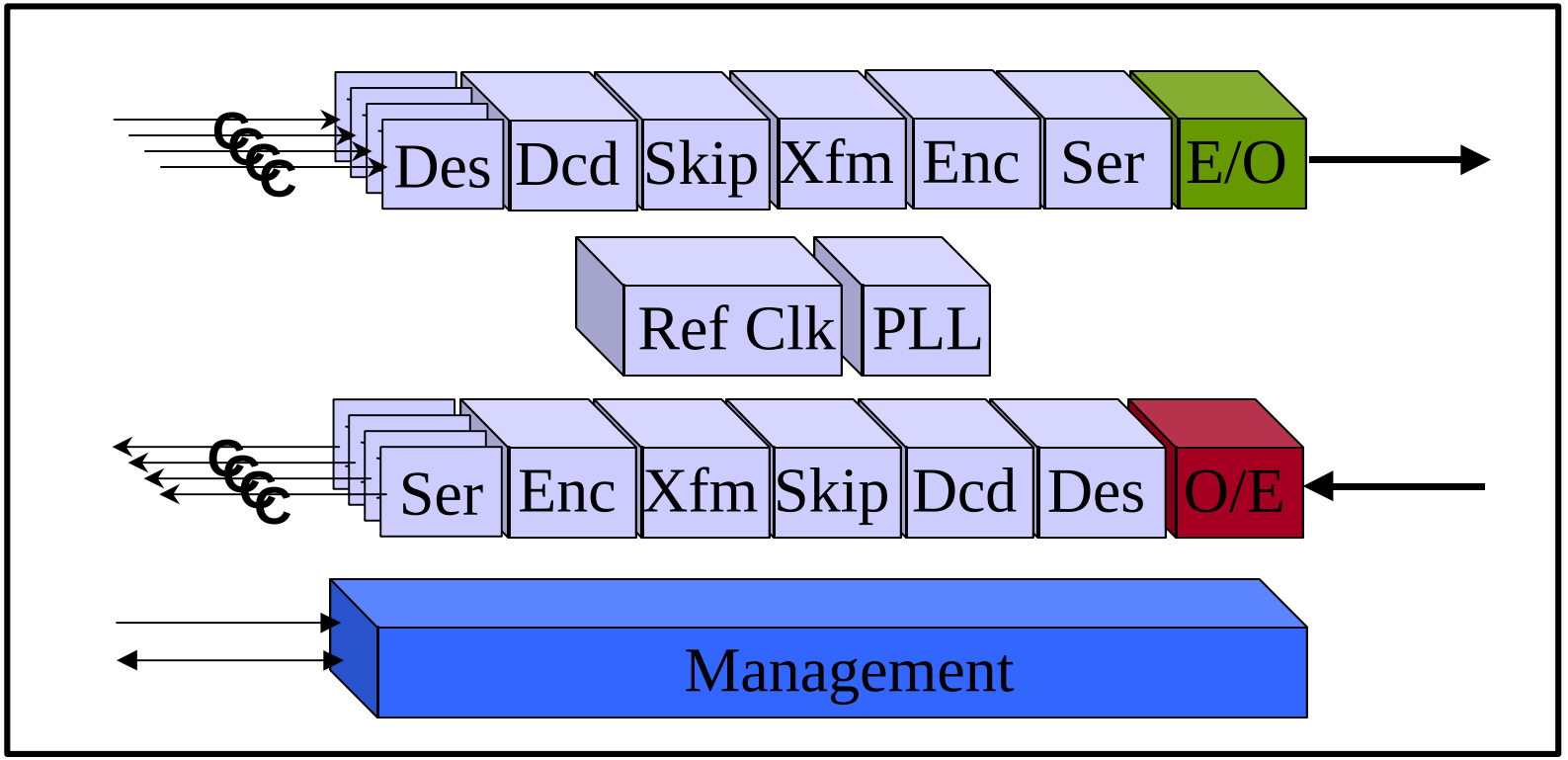
- **Reference Clock and PLL are assumed necessary since "Hari" Interface has no jitter budget allocated to transceiver**
- **Management I/F covers all low speed functions like signal detect, transmit disable, fault, etc.**

Transceiver Functional Comparison

Transceiver Type	Transmit							Receive							Common		
	Des	Dcd	Skip	Xfm	Enc	Ser	E/O	O/E	Des	Dcd	Skip	Xfm	Enc	Ser	Clk	PLL	Mgmt
12.5G Serial	✔			✔		✔	✔	✔	✔			✔		✔		✔	✔
4X WWDM	✔						✔	✔						✔		✔	✔
4X Parallel	✔						✔	✔						✔		✔	✔
Multilevel	✔	✔		✔	✔	✔	✔	✔	✔	✔		✔	✔	✔		✔	✔
10G Serial	✔	✔		✔	✔	✔	✔	✔	✔	✔		✔	✔	✔	✔	✔	✔
12.5G Serial	✔		✔	✔		✔	✔	✔	✔		✔	✔		✔	✔	✔	✔
4 x WWDM	✔		✔			✔	✔	✔	✔		✔			✔	✔	✔	✔
4 x Parallel	✔		✔			✔	✔	✔	✔		✔			✔	✔	✔	✔
Multilevel	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

- **Tx & Rx Ser & Des assumed if Skip is implemented (due to buffer)**
- **Implementations with clocks are reserved in case jitter on media can only be maintained with a local PMD clock.**

Power Down Domains



0: Management Always On; Everything else off

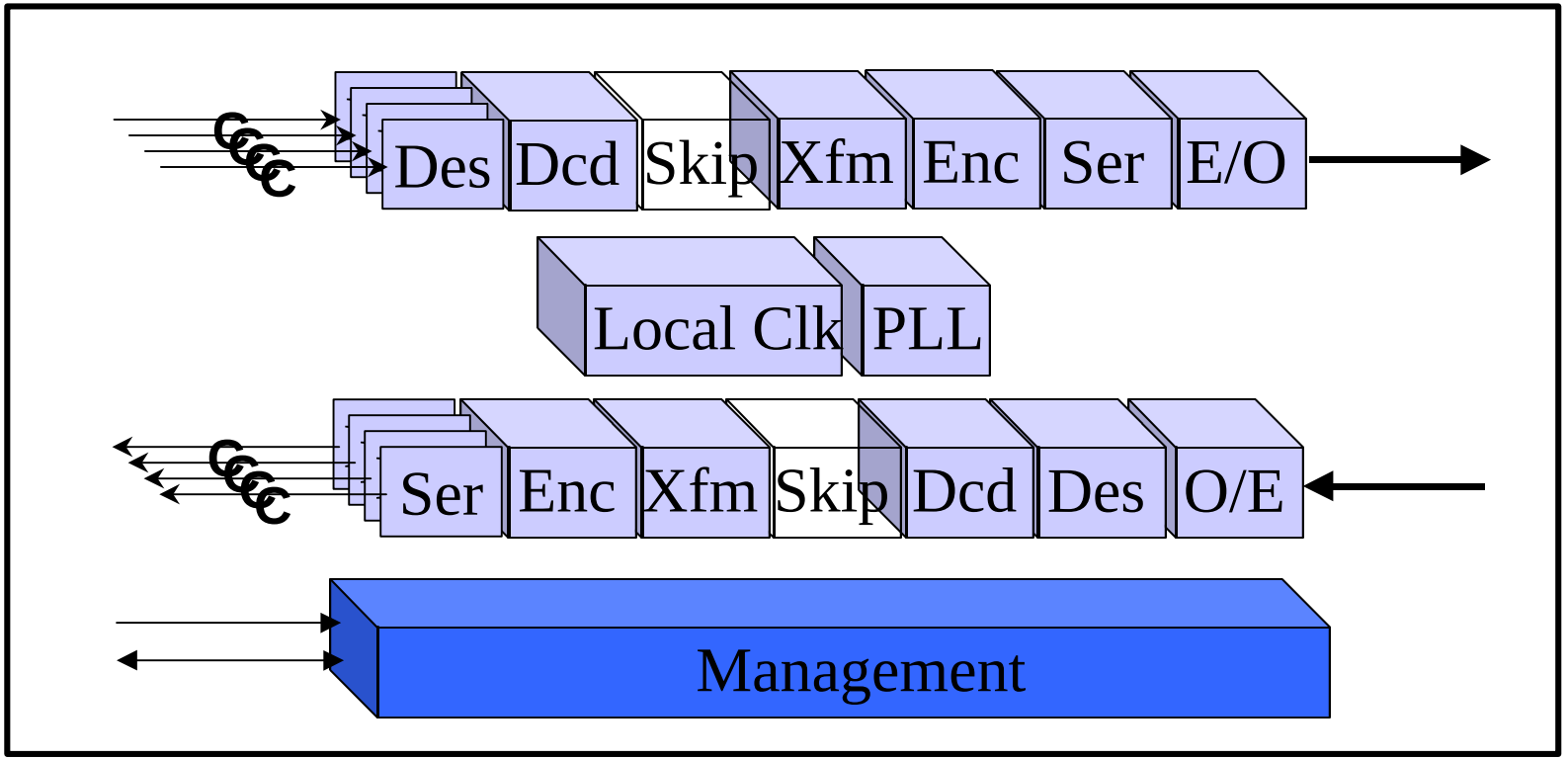
1: 0 + Preamp/Postamp/Signal Detect On -- watch for incoming light

2: All But Laser -- Support EWRAP (PLL running for Rx quick sync)

3: Reserved

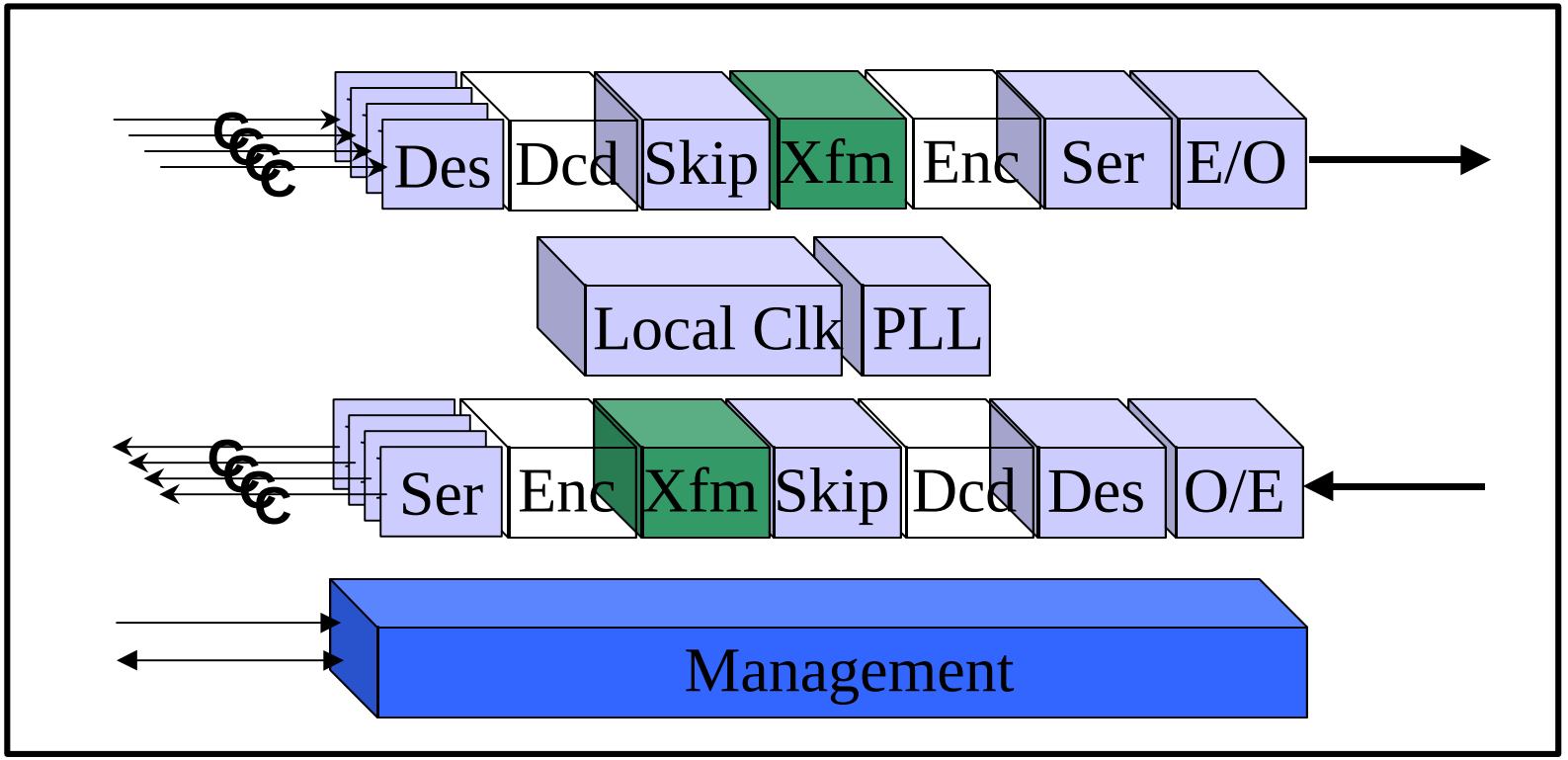
4: Everything On -- Full function

10.0 Gb/s Serial Transceiver



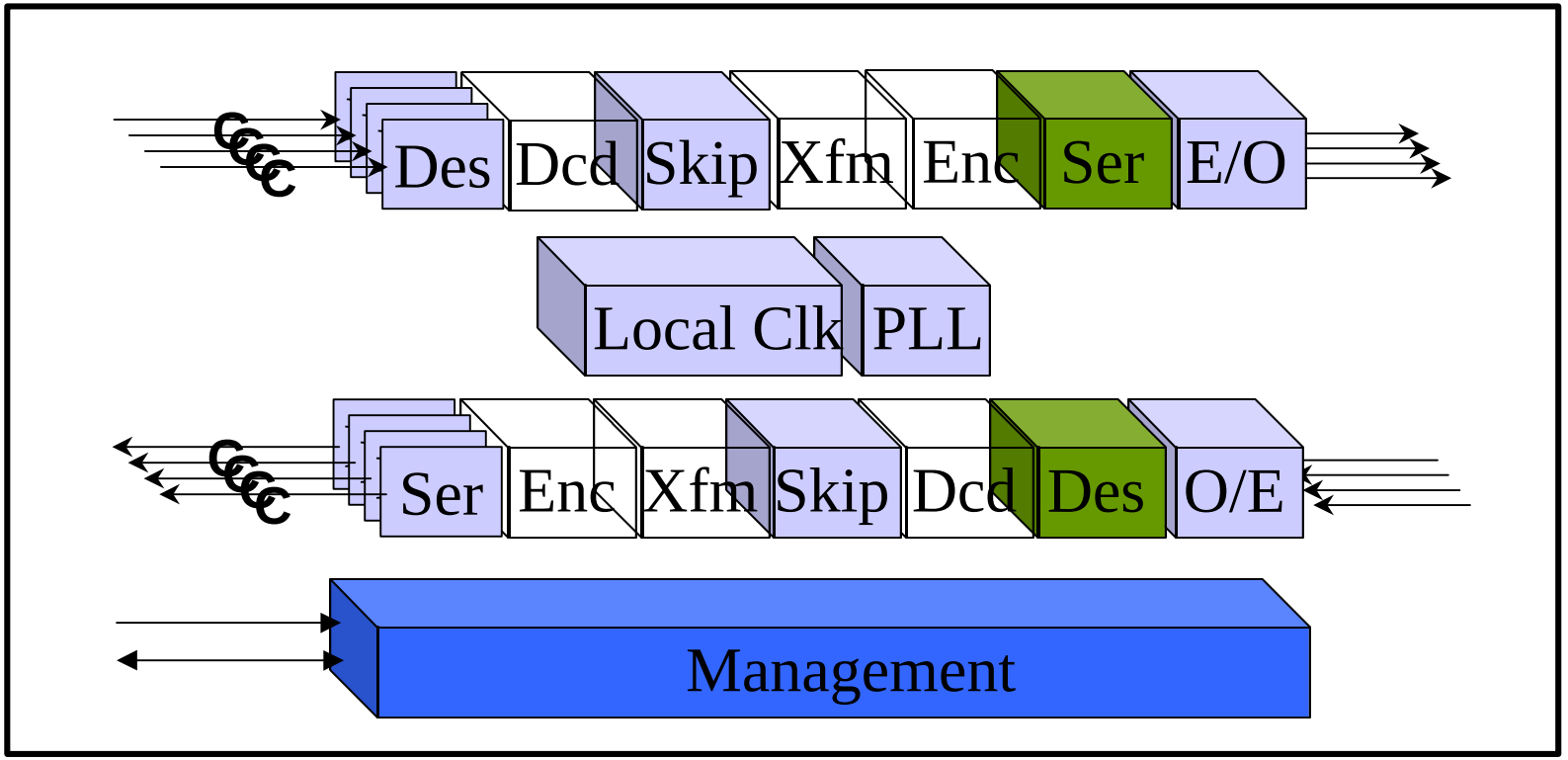
- **Assumed Use of Scrambled Code**
- **Transform complexity is determined by "protocol" requirements of the serialized stream (e.g. SONET)**

12.5 Gb/s Serial Transceiver



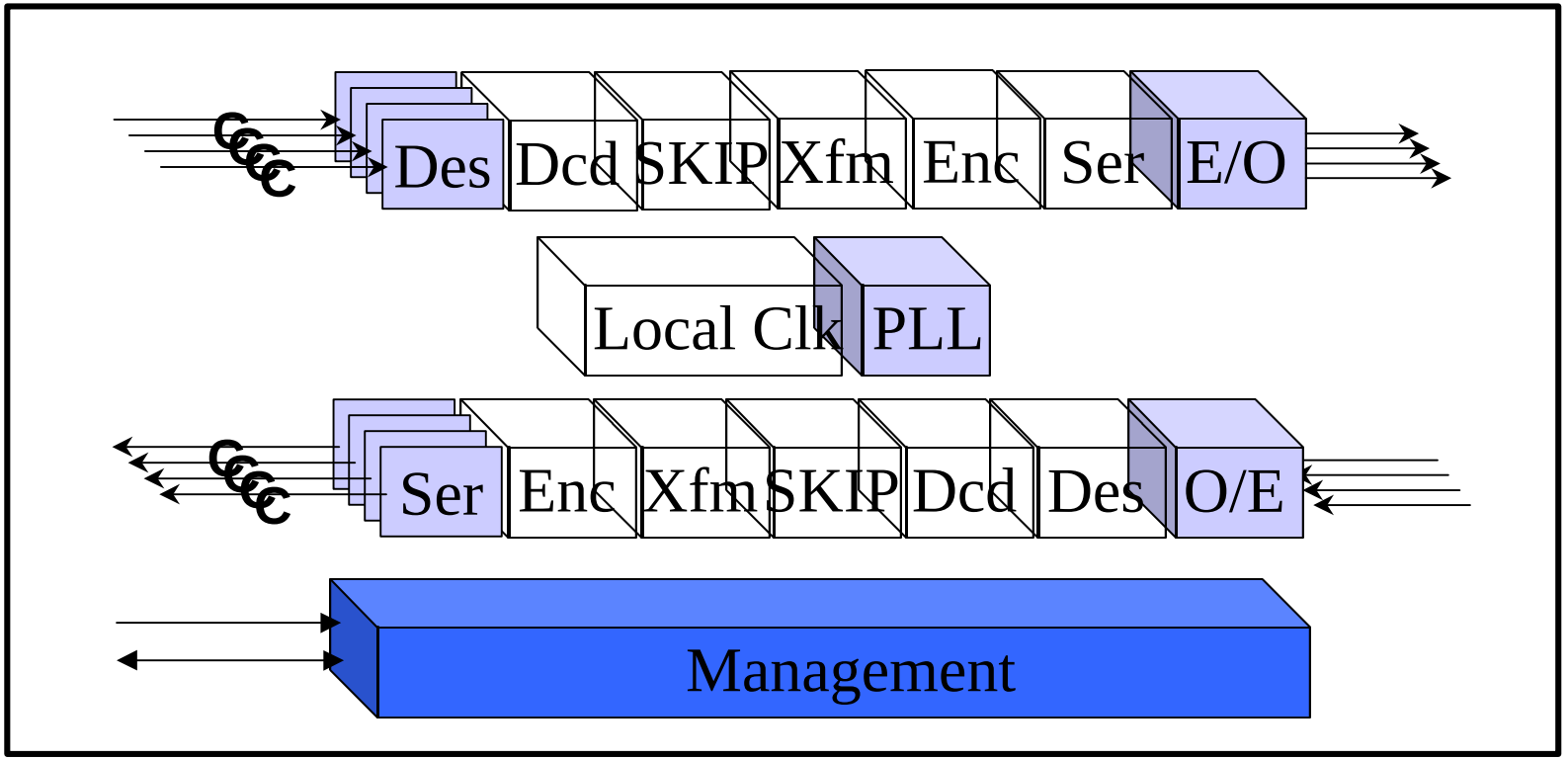
- **Assumed use of 8B/10B Code throughout**
- **No Encode / Decode Blocks Required**
- **Xfm: Transform could be a simple disparity correction**

4 x 3.125 WWDM and Parallel



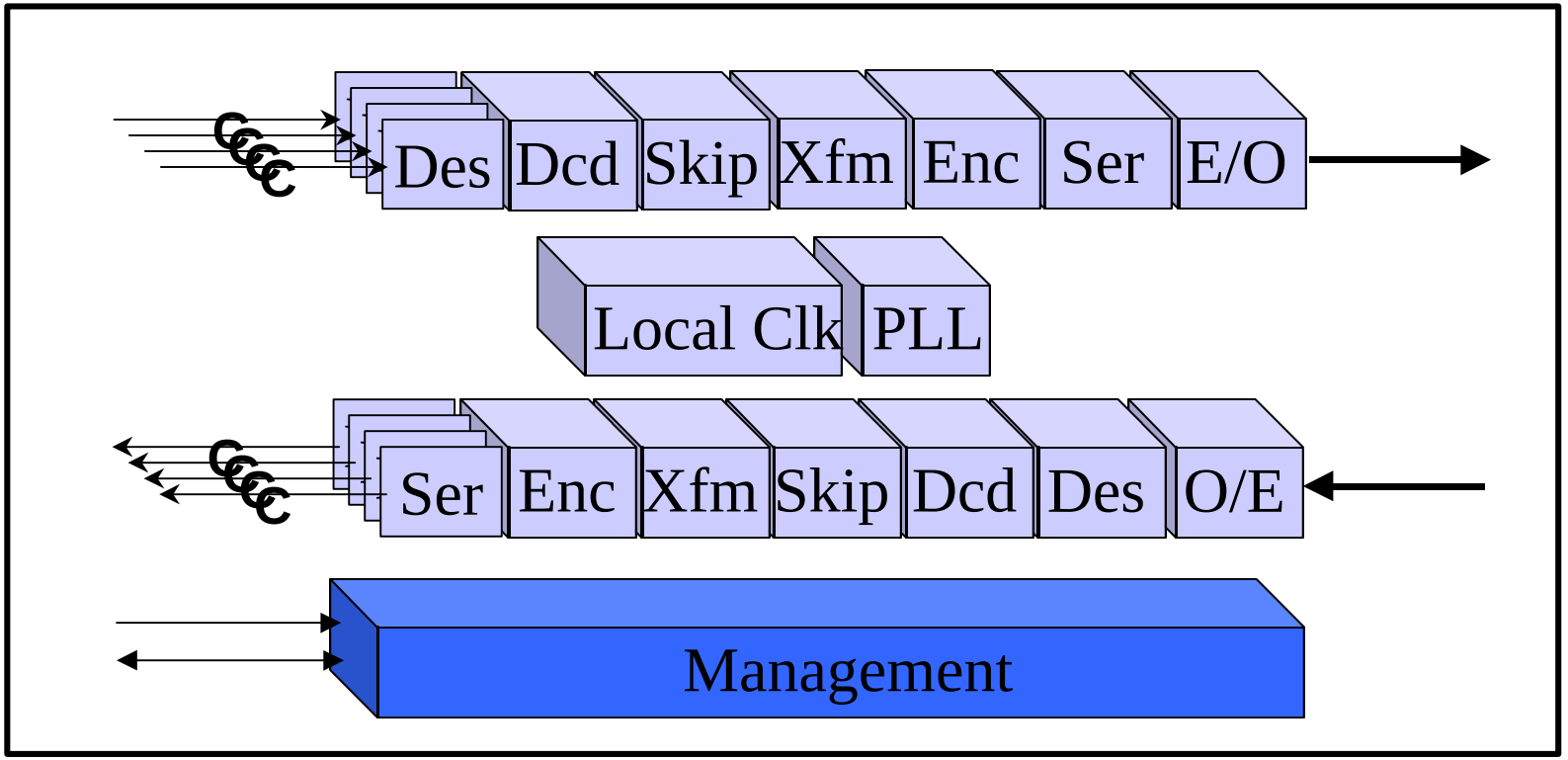
- **Assumed use of 8B/10B Code throughout**
- **No Encode / Decode or Transform Blocks Required**
- **SERDES assumed when SID buffer done in parallel**

Retimed 4 x 3.125 WWDM/Parallel



- **Most effective solution for WWDM and Parallel if local clock is not required and PHY can meet jitter requirements.**

Multilevel Transceiver (e.g. PAM)



- **Will use all functional blocks, with the exception that the Encode/Decode and Serializer functions will be substituted with magic analog sauce.**