10GE Link Design For Scrambled Encode

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Agenda

- Terminology
- Relationships
- Data Recovery
- Clock Recovery
- Jitter Tolerance
- Encode Complexity
- Performance

Terminology

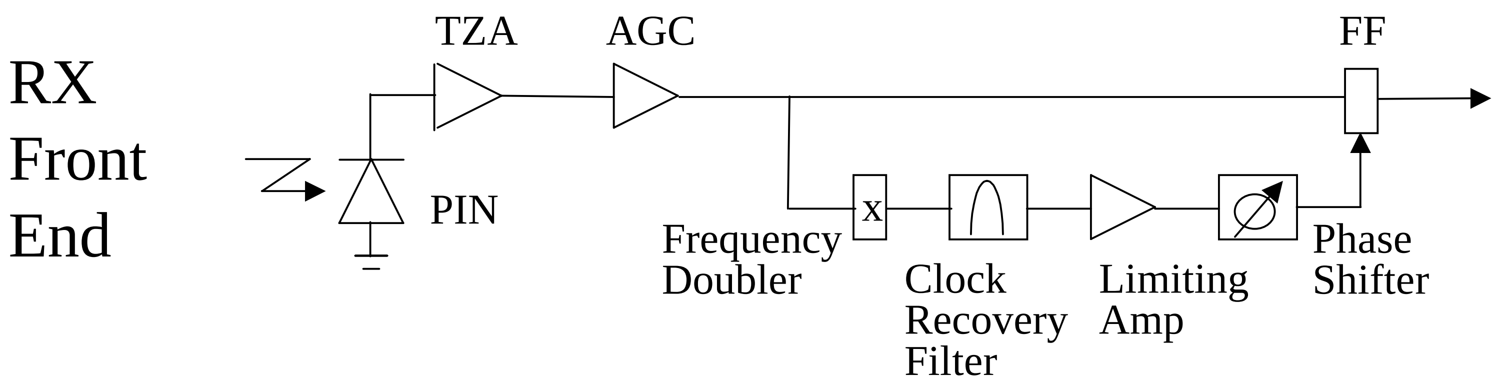
- **Digital Sum Variance (DSV)**
  - — the pk-pk difference between the min & max running sum of the data, over the sequence length
- **Baseline Wander**
  - — the variation, in the amplitude axis over time, of the data eye center
- **DC Balanced**
  - — whether or not the sum of the data, over the sequence length, is zero (where a data value of zero is counted as -1)
- **Run Length**
  - — the number of consecutive one’s or zero’s (CID) in the data stream
- **Transition Density**
  - — the number of data transitions over the sequence length

Relationships

- **Digital Sum Variance -> Data Recovery**
  - — a data pattern with a large DSV can potentially cause baseline wander at the RX data recovery block if the lower cutoff of the RX passband does not capture enough of the low frequency content in the data
- **Run Length -> Clock Recovery/Jitter Tolerance**
  - — the longer the run of continuous identical digits (CID) in a data pattern the higher the Q required for the clock recovery filter, for a higher Q (i.e. narrower bandwidth) clock recovery filter the lower the input jitter that can be tracked by the RX

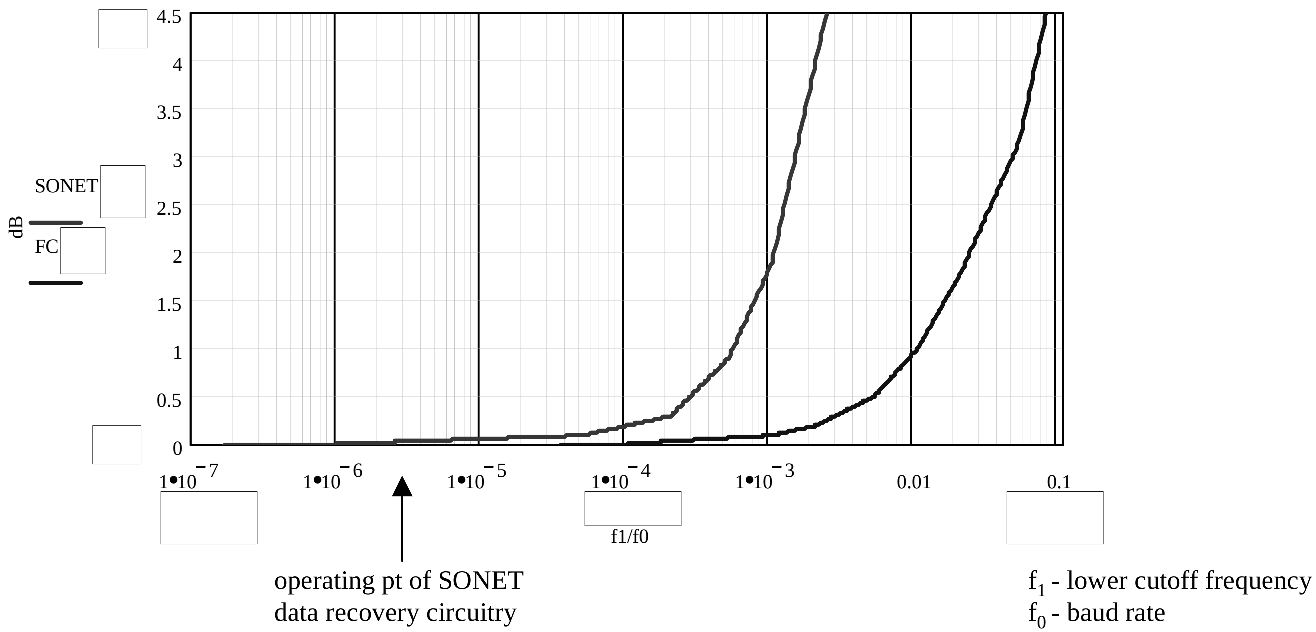
Data Recovery

- **Data passband filter...**



Data passband filter is comprised of the net effect of decoupling cap’s (between circuits with different DC bias points or different technologies) and the upper cutoff of the AGC (or passband filter if no AGC).

- **The lower cutoff frequency required to avoid baseline wander induced data errors for a SONET signal is in the 10s of kHz range**
- **Thus for 10G the capacitors selected need to be well behaved over ~6 orders of magnitude**
  - —not a cost issue, just a design choice
- **Note that if the RX front-end is integrated, with no AGC/decoupling cap's, then the required low frequency cutoff is achieved inherently (i.e. near-DC)**



The SONET curve is plotted for the 72 CID pattern, which has an average interval between occurrences of ~7500 yrs.

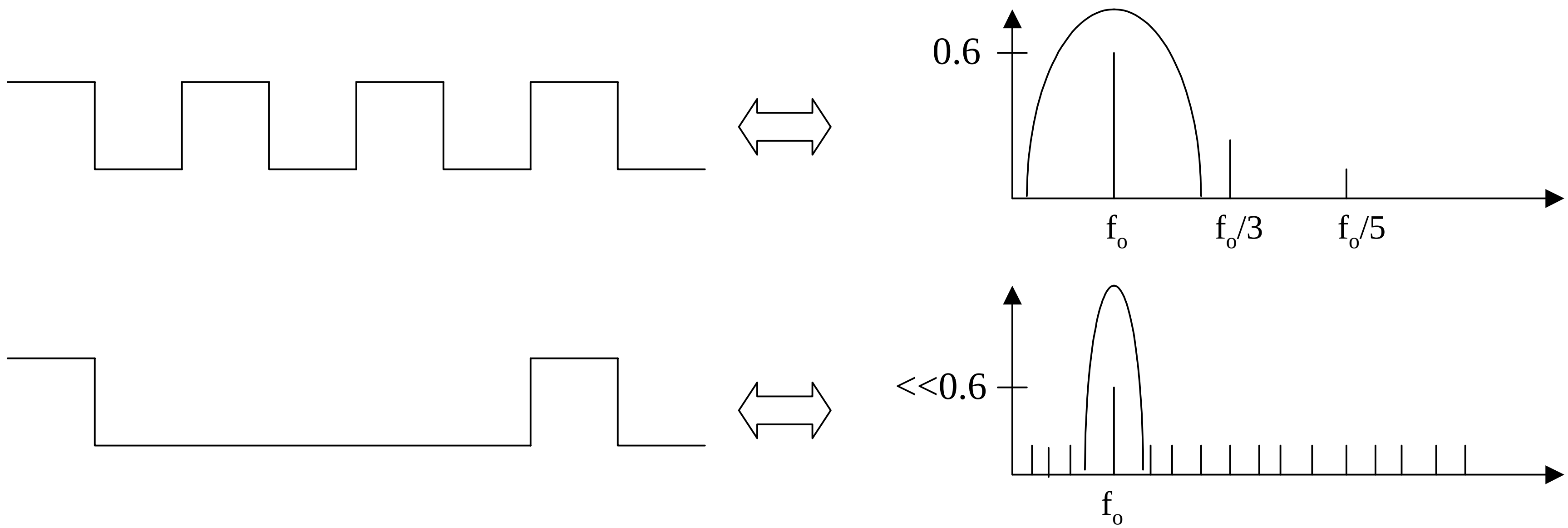
Baseline Wander Power Penalty

- **The upper cutoff frequency required for optimum signal/noise is at about half the NRZ data rate**
- **Thus for 10G the upper cutoff frequency of the AGC/decoupling cap's is ~5G**
  - —not a cost issue, just a design choice

Scrambled encode <u>not a cost issue</u> for data recovery

Clock Recovery

- **The longer the string of CID, the more signal energy is shifted to harmonics of the fundamental**
- **The clock recovery filter bandwidth must then be narrower to reject those harmonics and the partner limiting amp must be more sensitive to pick up the lower energy of the fundamental**

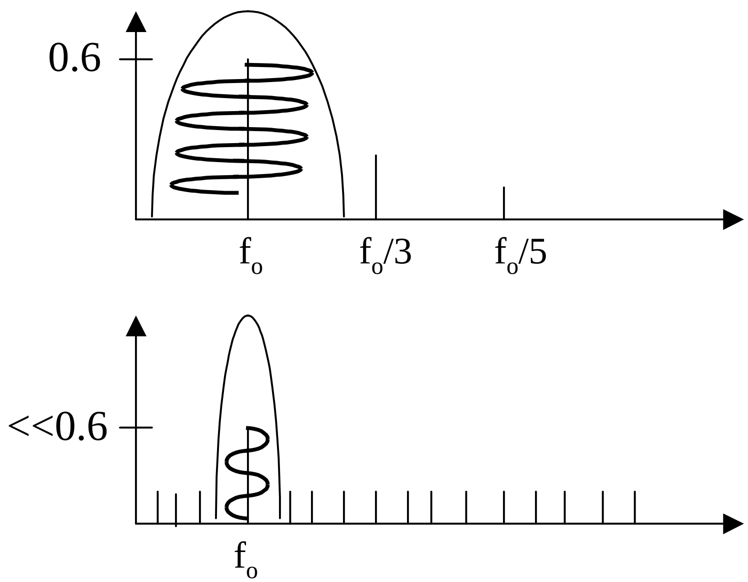


- **The filter $Q=f_{clk}/BW_{flt}$**
- **For 10G SONET a filter with a 3dB BW of 15-20MHz or Q of ~600 is used (2nd order Butterworth)**
- **A filter with a Q of this order is a commodity**
- **The partner limiting amp typically has a gain of ~20dB, again a commodity part**

Scrambled encode <u>not a cost issue</u> for clock recovery

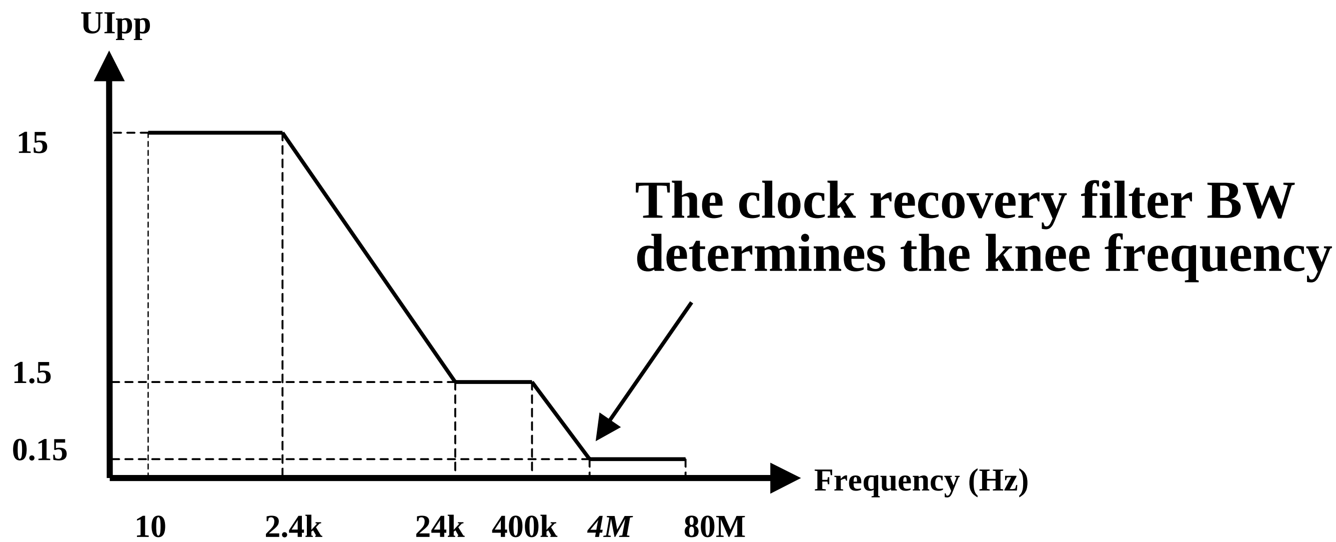
Jitter Tolerance

- **The clock recovery filter BW determines the RX input jitter tolerance high frequency knee**



The wider the clock recovery filter BW, the higher the knee frequency of the RX jitter tolerance

- **Input jitter tolerance (TP3)**



Source: GR-1377-CORE (12/98), G.825 (02/99)

- **The input jitter tolerance amplitude, in the knee region, from SONET OC-192 long reach can be relaxed for the 10GE shorter reach environment by reallocating some of the optical impairment jitter budget**

$$\frac{T_{open} - J_{bounded} - J_{trackable}}{\sigma_{RHS} + \sigma_{RHS}} = Q_{target}$$

$$\text{where,} \quad J_{bounded} = J_{pattern} + J_{propagation} + Rcvr_{impl}$$

- **Example:** T_{open}= 100ps

  $J_{pattern}$= 15ps

  $J_{propagation}$= 2ps*

  $Rcvr_{impl}$= 33ps

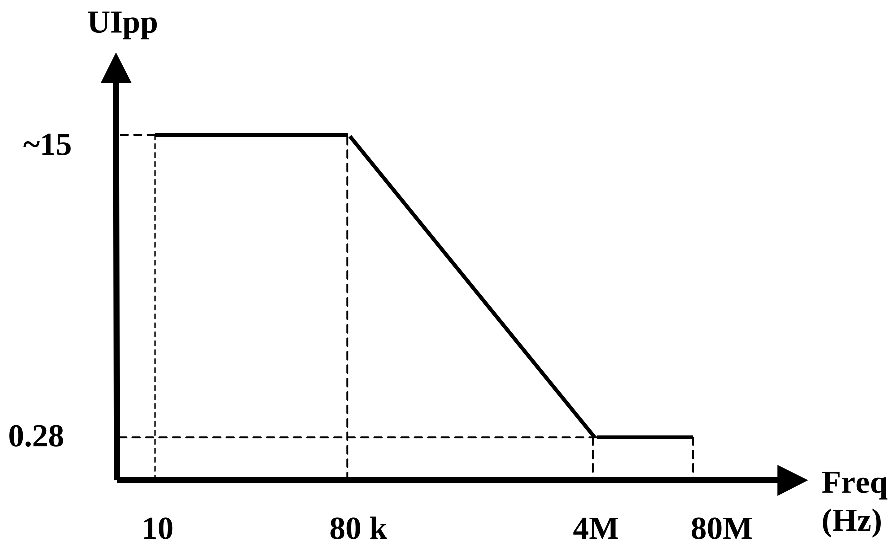
  σ_{RHS}=σ_{RHS}= 1ps

  Q_{target}= 10

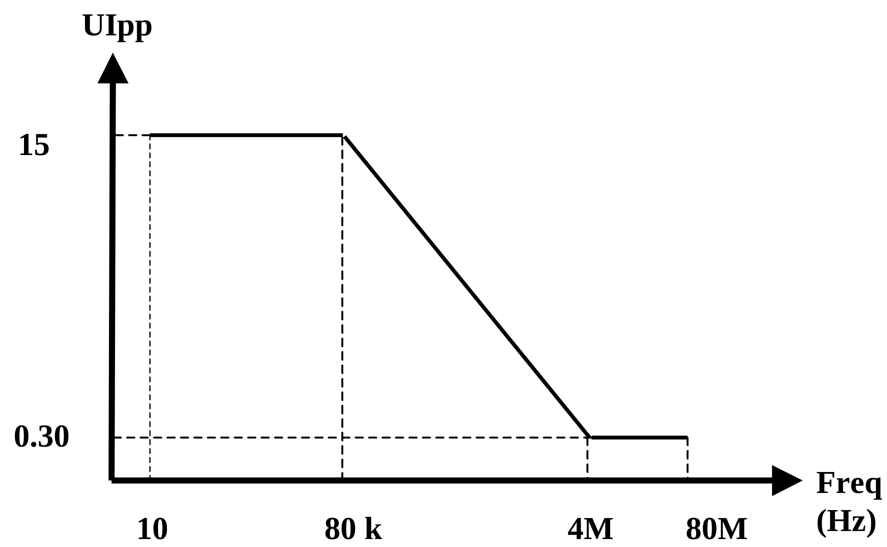
- **Yields… $J_{trackable}$= 30ps, twice the current mask value, thereby relaxing TX jitter generation/easing design**

* IR, 10km, cooled DFB 0.3nm, laser tolerance +/-3nm, fiber zero tolerance +/-5nm, fiber dispersion slope 0.07ps/nm/km/nm

- **Example 10GE jitter generation (TP2)**

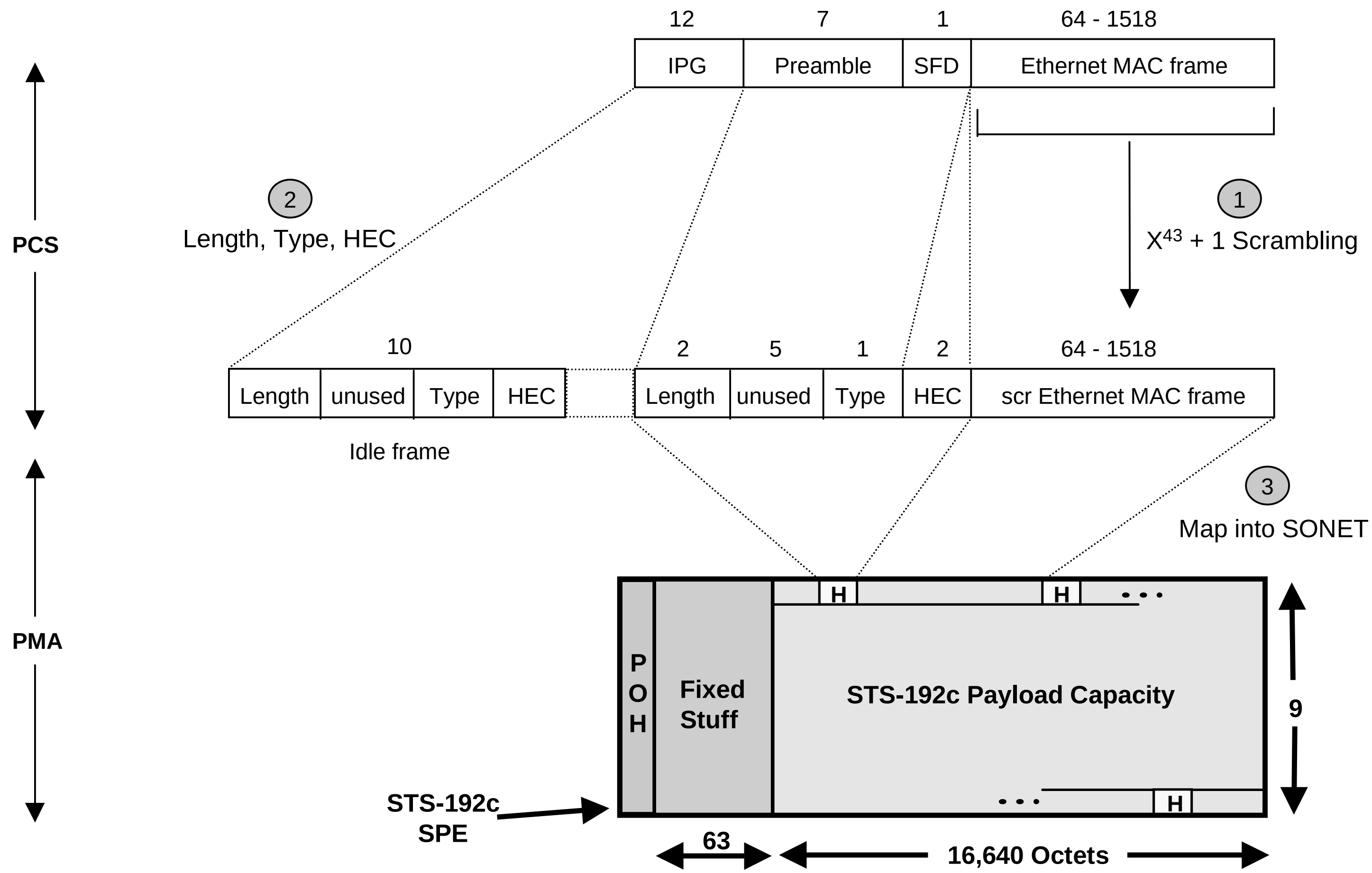


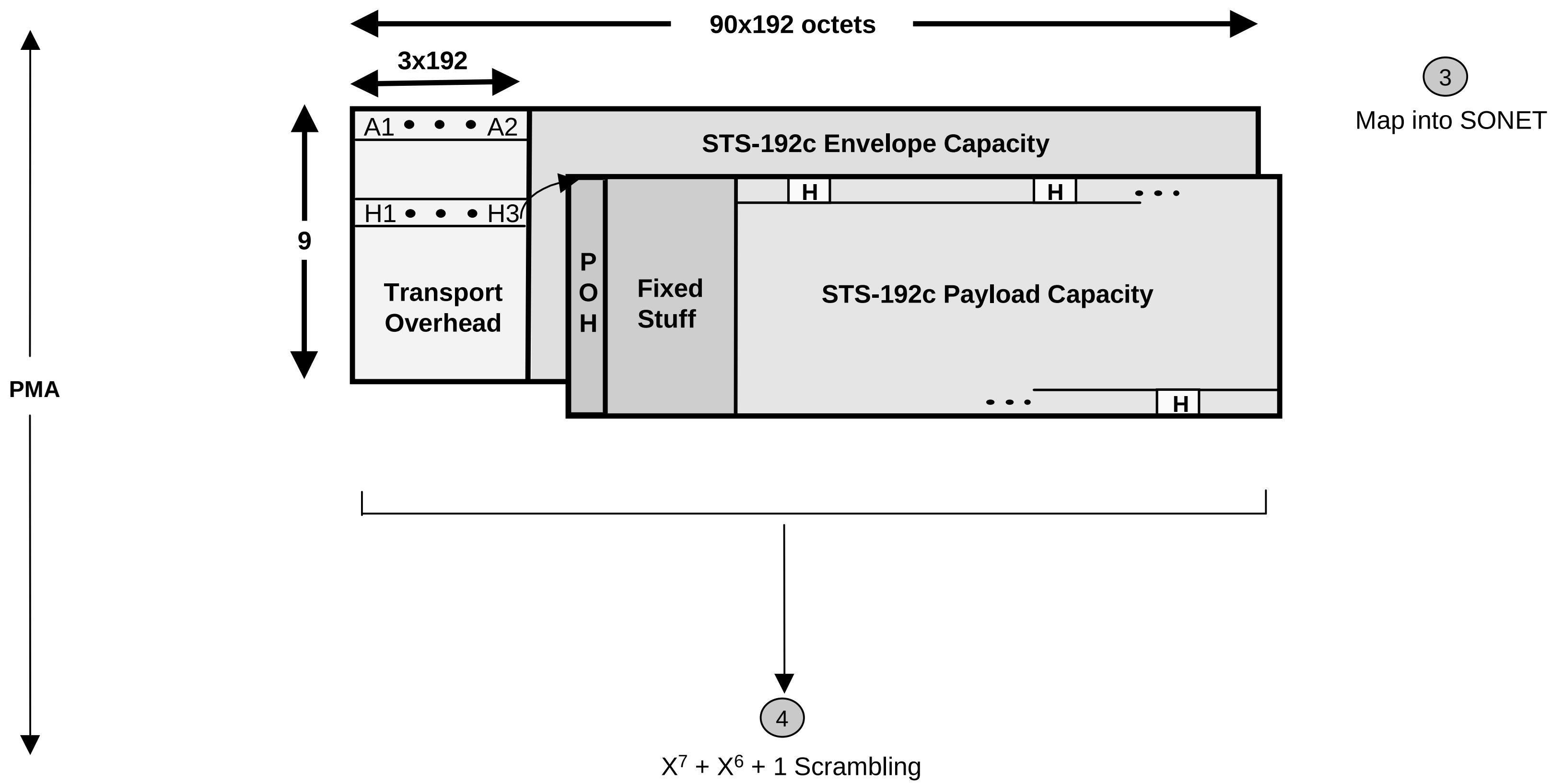
- **Example 10GE input jitter tolerance (TP3)**



Relaxed jitter tolerance possible with scrambled encode

Encode Complexity




90x192 octets
3x192
9
PMA
A1 • • • A2
H1 • • • H3
Transport Overhead
STS-192c Envelope Capacity
P O H
Fixed Stuff
H
H
STS-192c Payload Capacity
H
3
Map into SONET
4
X7 + X6 + 1 Scrambling

8B/10B PHY		**STS-192c PHY**		**Full SONET OH Processing**	
8B/10B encoder:	4080	x43 + 1 scrambler:	90		
		length generation:	150		
		HEC generation:	200		
		POH generation:	500	full POH generation:	700
		pointer generation:	0	full pointer generation:	700
		LOH generation:	300	full LOH generation:	1300
		SOH generation:	500	full SOH generation:	700
		x7 + x6 + 1 scrambler:	75		
8B/10B decoder:	2730	framer:	500		
		byte align:	300		
		x7 + x6 + 1 descrambler:	75		
		SOH extraction:	500	full SOH extraction:	800
		LOH extraction:	300	full LOH extraction:	1200
		pointer processing:	800	full pointer processing:	1700
		POH extraction:	500	full POH extraction:	1000
		HEC delineation:	1000		
		x43 + 1 descrambler:	90		
8B/10B Total	**6810**	STS-192c Total	**5880**	Full OH proc increment	**4700**

Note: Processing is at 155MHz, 64-bit wide.

Gate Count Comparison

Sublayer	OH Byte	STS-1#1	Notes	STS-1#2-192	Notes
SOH	A1	F6		F6	
	A2	28		28	
	J0	provision		00 (Z0)	
	B1	calculate		00	
	E1	00		00	
	F1	00		00	
	D1-3	00		00	
LOH	H1	62	NDF idle, 522 ptr offset	93	concatenation indicator
	H2	0A		FF	
	H3	00		00	
	B2	00	unused	00	unused
	K1	01	NR, CHID=1	00	
	K2	10	CHID=1	00	
	D4-12	00		00	
	S1	F0	"Don't Use"	00 (Z1)	
	M1	00	unused	00 (Z2)	
	E2	00		00	
POH for STS-192c	J1	provision			
	B3	calculate			
	C2	new code			
	G1	calculate	P-REI, P-RDI		
	F2	00			
	H4	00			
	Z3-5	00			

Summary

In the TX direction, all OH values are hardwired defaults except:

- J0: provisionable
- B1: calculated
- J1: provisionable
- B3: calculated
- G1: calculated

In the RX direction, all OH values ignored except:

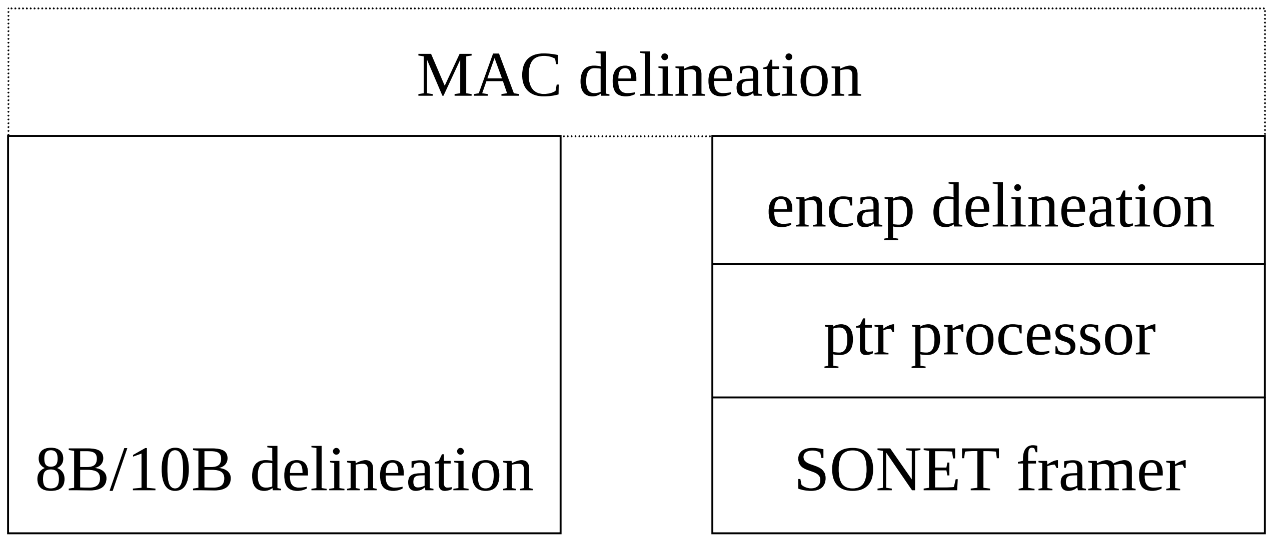
- A1-2: used by framer
- J0: compared against provisioned value
- B1: compared against calculated value
- H1-3: used by pointer processor
- J1: compared against provisioned value
- B3: compared against calculated value
- G1: extracted

Proposed Minimal SONET OH Usage

- **The gate count complexity for an 8B/10B or STS-192c PHY is very similar (actually slightly less for STS-192c)**

Scrambled encode <u>not a cost issue</u> for digital processing

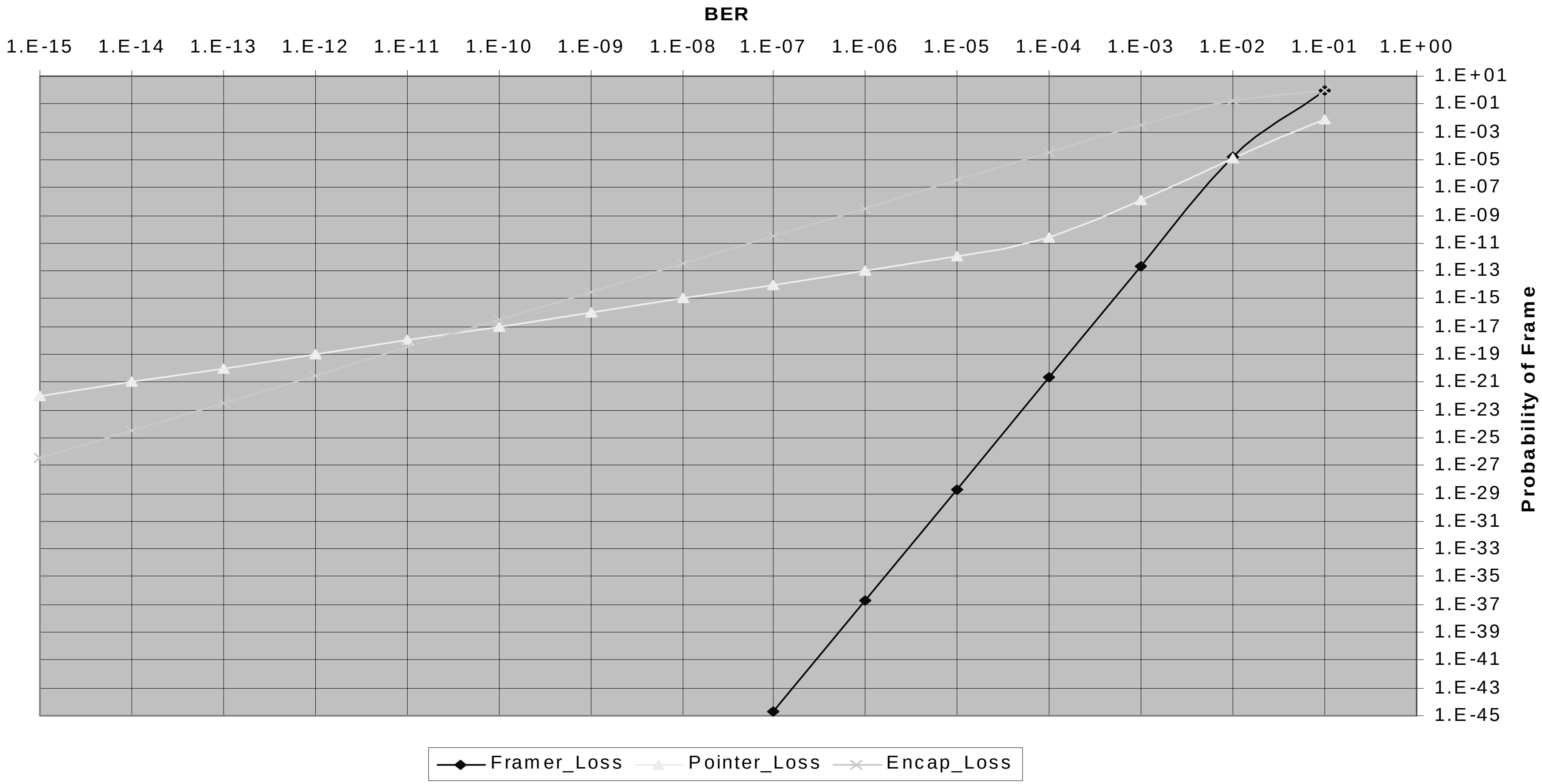
Performance



Compare 8B/10B vs SONET mapping delineation performance

(Recall no issue with error detection reduction, per Norival Figueira presentation Mtl-July'99)

SONET component frame loss

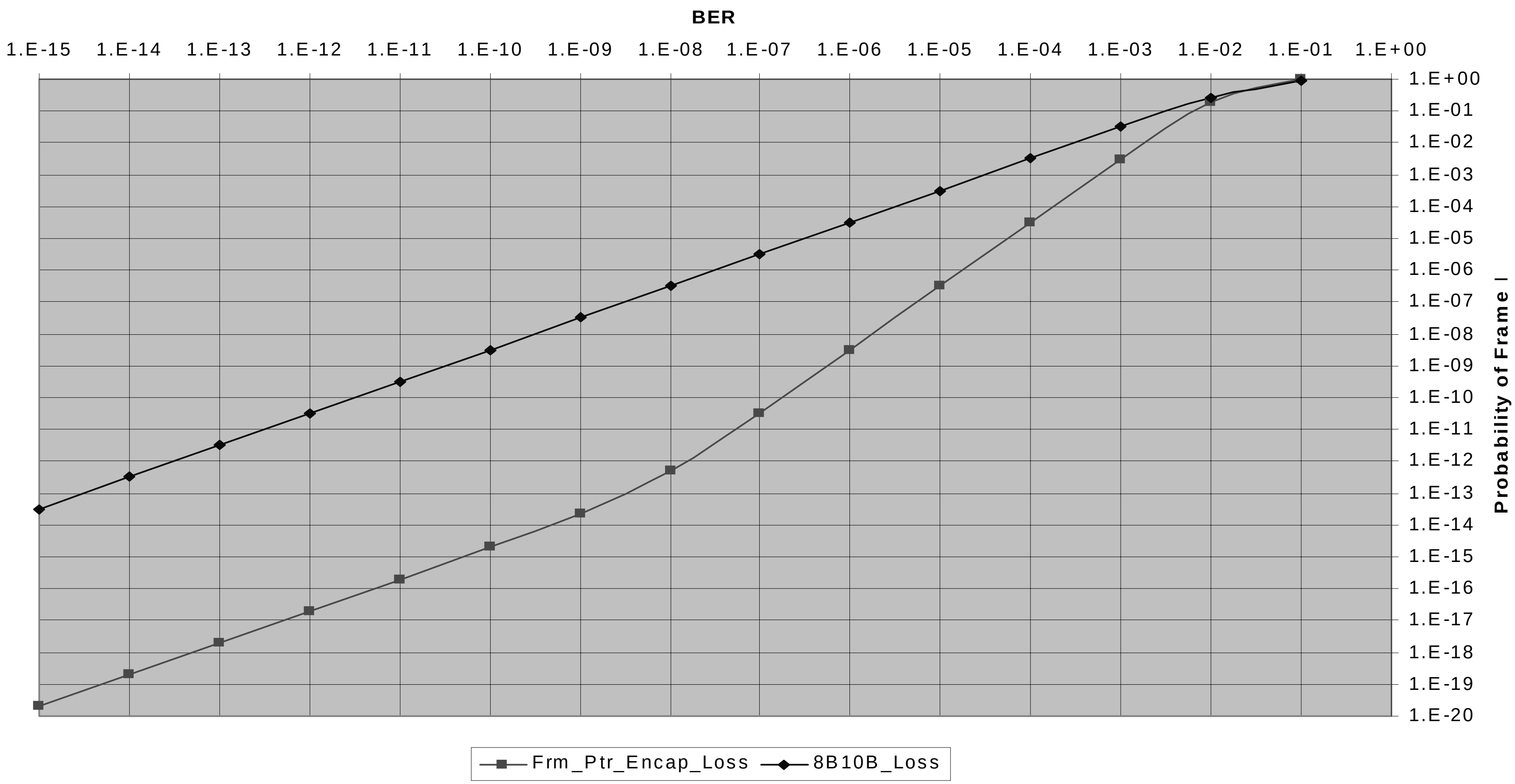


SONET Framer FL due to:
- > 1 error in frm pattern

SONET Ptr FL due to:
- ptr corrupt, data emulation

SONET Encap FL due to:
- > 1 error in header

SONET total vs 8B/10B frame loss



8B/10B layer FL due to:

- error in /S/, /T/, /R/ characters, data emulation

- **Compare performance of proposed SONET mapping (10G) vs 8B/10B (12.5G) at 1E-12 BER:**

SONET MTTFL=1/2.00E-17/10E09=58 days

8B/10B MTTFL=1/3.17E-11/12.5E09=2.5 sec

SONET mapping MTTFL better than 8B/10B by ~ 2E06 at 1E-12

Summary

- **Scrambled encode not a cost issue for:**
  - — data recovery
  - — clock recovery
  - — jitter tolerance
  - — digital processing (similar to 8B/10B)
- **The encode proposal has significant performance advantages:**
  - — robust delineation
  - — extended reach/relaxed link budget
- **Scrambling at 10G has been field proven since 1995**
  - — parts readily available now
- **Scrambling can operate over serial/parallel optics, MMF/SMF**