10BASE-T1: Power & Data II

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Introduction

This presentation explores a Data & Power architecture designed to fit applications that require a daisy-chained cable topology.

Consideration is given to both data aspects, as well as the desire to provide a modest amount of power to the devices. Being able to power devices over the communication cable allows for a small degree of power redundancy, as well as significant savings in standby power.

Simulations are provided that show the power delivery performance difference of multidrop and full-duplex, as well as a cost comparison of the needed coupling inductors.

DALI – Digital Addressable Lighting Interface

DALI covers OSI layers from Physical to Application and is extensively used in lighting controls. See ➠wendt_10SPE_01_0916.pdf

- 1200 bit/s, two wire communication
- Manchester endoded with voltage swing up to 16V±6.5V
- Nearly any cable can be used (mains cable, twisted pair, …)
- Free topology – possible due to the extremely low data rate

With 10BASE-T1 is is not expected that mains cabling can still be used, nor will it be possible/desired to use a completely free cabling topology.

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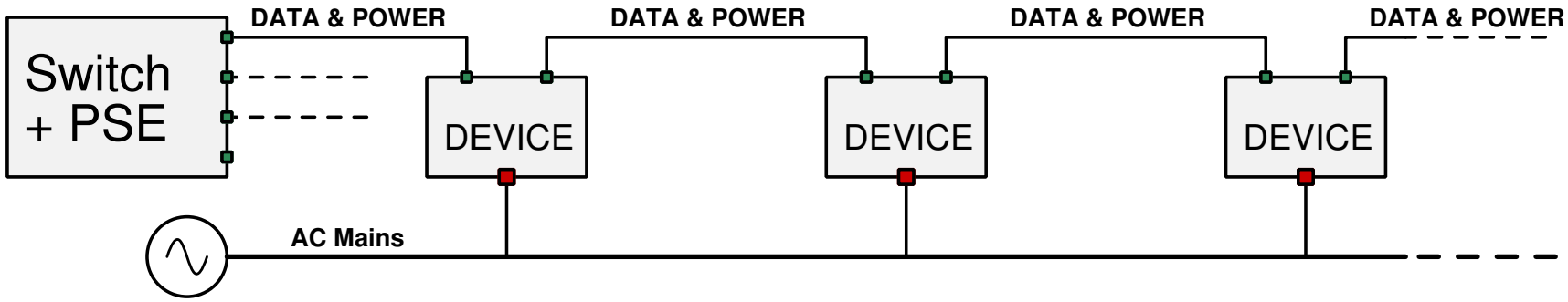
Architecture for Lighting



Devices (luminaires, sensors, …) are connected in passive linear topology. DALI carries a limited amount of power, and offers bus based data at very low data rate.

Requirements for 10BASE-T1:

1. **Redundancy:** Device fault doesn't interrupt data & power flow
2. **Power:** Mains failure doesn't interrupt data & power flow
3. **Topology:** Linear wiring possible (active or passive)

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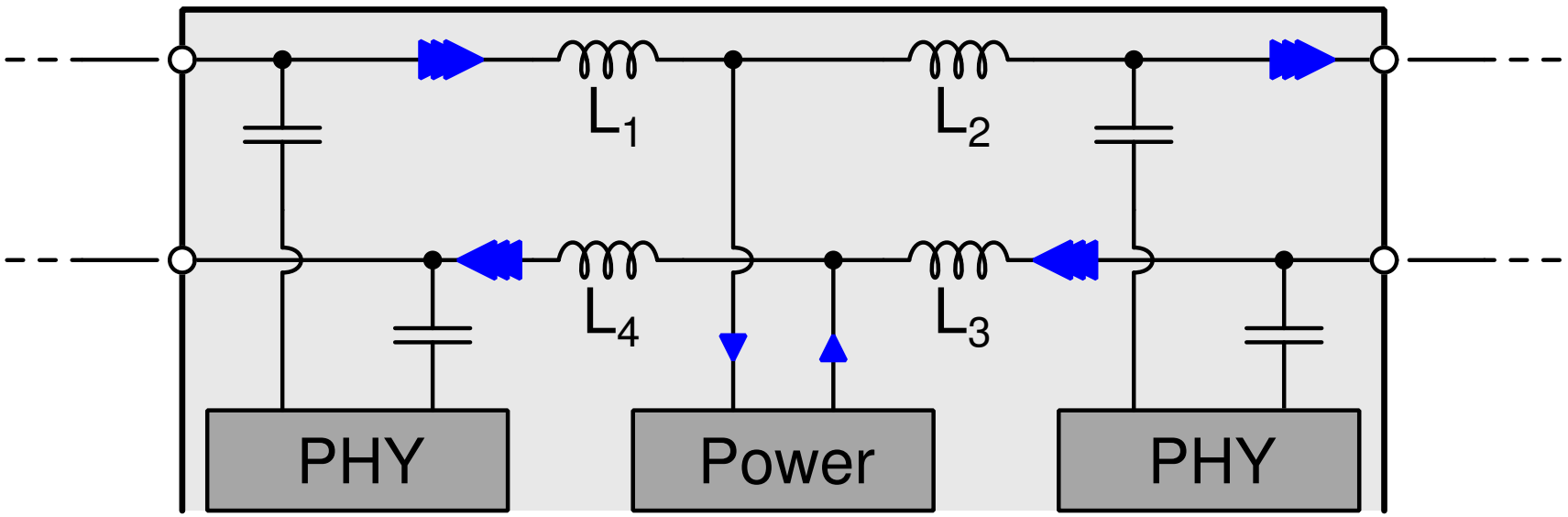
Full duplex 10SPE powering



The total current of all downstream devices flows through the device, encountering L_1, L_2, L_3 and L_4 in series. Power is tapped at the center of the inductors. These inductors must be rated for the maximum current that the PSE can source. This maximum PSE current becomes a specification point that cannot be altered later on.

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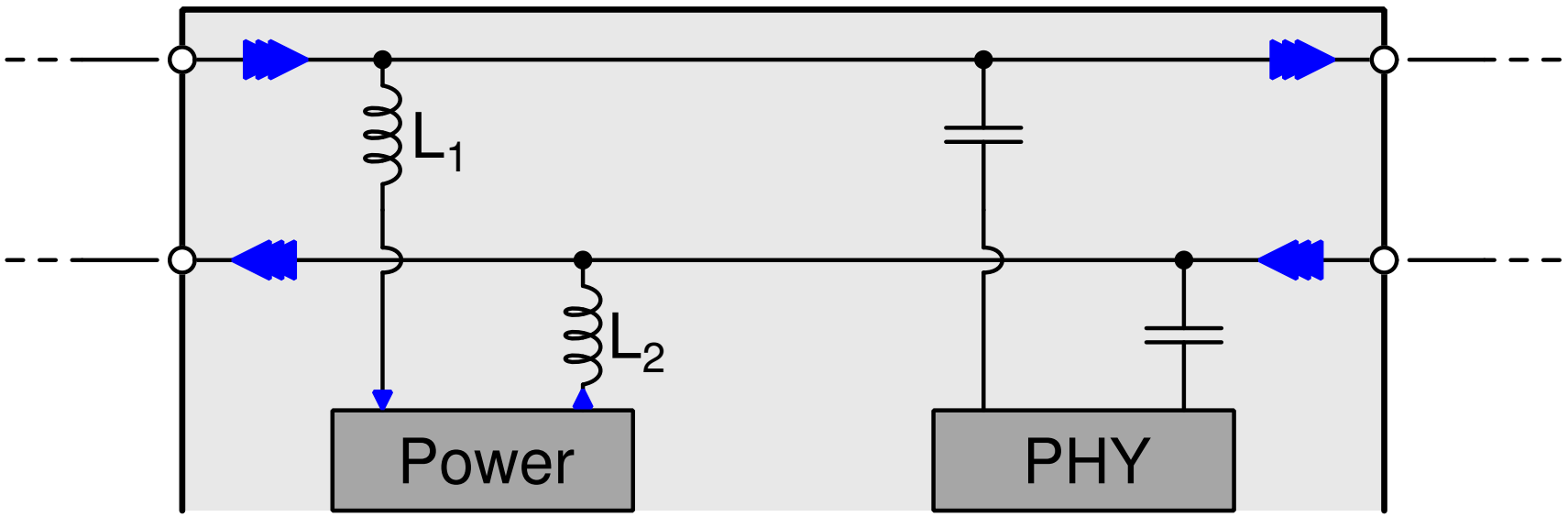
Multidrop 10SPE powering



The total current of all downstream devices flows through the device. No series components are required. Power is tapped through inductors L_1 and L_2, which only need to be sized according to the PD consumption. A large amount of pass-through current can be specified with minimal cost impact.

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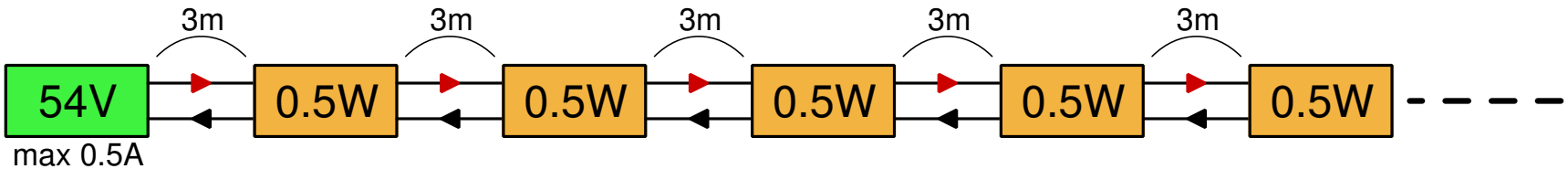
Benchmarking

Common assumptions to all simulations:

- V_{PSE} = 54V, maximum current 0.5A
- Between each node: 3 meter of AWG24 copper cable, single twisted pair at 20°C
- Each device consumes 500mW
- Lowest allowable PD voltage is 35V (stability)
- 220 µH inductors (L_1 – L_4)
- The relative cost compares the BOM cost of inductors L_1 – L_4 only!

The simulation keeps attaching a node in daisy chain with the last until either the last PD voltage is less than 35V, or the PSE current exceeds 0.5A.



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Benchmarking results

Name	DCR	Rel. cost	Nodes	Efficiency
Multidrop	5.40 Ω	1.00	48	88.7 %
Full Duplex (inductor 1)	0.75 Ω	6.90	28	70.7 %
Full Duplex (inductor 2)	0.40 Ω	14.7	36	71.7 %
Full Duplex (inductor 3)	0.19 Ω	33.9	43	77.6 %
Full Duplex (inductor 4)	0.15 Ω	62.0	44	80.0 %

Calculations show there is a severe cost and performance penalty for the full duplex linear powering method. The most cost effective full duplex solution is still more than 6x as expensive (inductor wise) compared to multidrop, and can support 28 versus 48 nodes at much lower efficiency. If lower DCR inductors are used (eg. inductor 3), performance is somewhat comparable, but the inductor cost is 33x higher than multidrop.

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Conclusions for Lighting

For the lighting application inline power is a requirement, as is support for linear wiring topology. The cost associated with the inductors for a full-duplex data scheme is prohibitive (by a wide margin) for the lighting application.

Without multidrop, an additional pair must be used to deliver power. This doubles the amount of copper in the cable and increases the risk for incorrect wiring.

It is understood that a multidrop PHY is a very different thing compared to full duplex PHY. Trade-offs will need to be made with regard to channel lengths, number of nodes, transmission power, bus capacitance, …

Proposed objectives

1. Investigate an optional multidrop mode for 10SPE. The MAC protocol to be chosen from MAC protocols already in 802.3.

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