S(H)DSL at a Glance

10 Mb/s Single Twisted Pair Ethernet Study Group

Nov 2016, Mario Traeber

Connected Home Division

Introduction

This presentation introduces SHDSL as a technology to support the CSD for 10SPE. The focus is mostly on feasibility of a Twisted Pair PHY ranging to 1km at 10Mbps full-duplex data transmission.

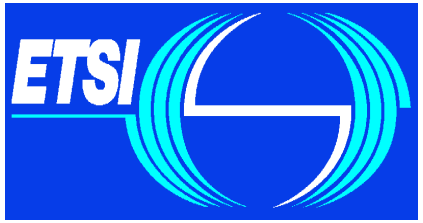
An introduction to the standards history, technology features and properties as well as performance characteristics will be presented.

The presentation concludes with a discussion on what would need to be explored further to apply the underlying technology principles to the objectives of 10SPE.

STANDARDS OVERVIEW

The history of SHDSL in various standards bodies and it’s relation into IEEE

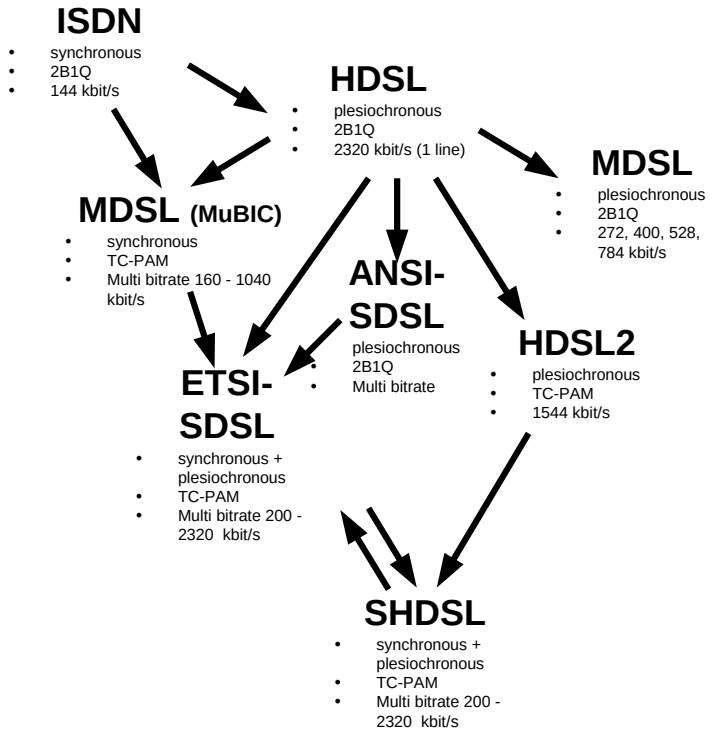
SDSL and SHDSL Standardization



Relationship between ISDN, HDSL, HDSL2, MDSL, SDSL and SHDSL

Standards

ISDN	(ETSI 1988)
HDSL	(ETSI 1996)
HDSL2	(ANSI 1999)
SDSL	(ETSI, 2000)
SHDSL	(ITU, 2000)



SDSL and SHDSL Standardization (2)

Major ETSI Decisions on SDSL

- Line code
- PSDs
- Network synchronization
- Data rates
- Frame structure
- EOC
- Electrical characteristics
- Activation
- Pre-activation
- ISDN transport
- Test loops
- Noise models

Major ITU-T Decisions on SHDSL

- Line code
- PSDs (North America)
- Network synchronization
- Data rates (North America)
- Frame structure
- EOC
- Electrical characteristics
- Activation
- Pre-activation

- Test loops (North America)
- Noise models (North America)
- ATM annex

SDSL and SHDSL Standardization

SDSL Data Rates

- Multi bit rate system
- Payload bit rates 192 kbit/s - 2312 kbit/s
- 8 kbit/s granularity

SHDSL Data Rates

- Multi bit rate system
- Payload bit rates 192 kbit/s - 2304 kbit/s
- North America: N• 64 kbit/s or N• 64 kbit/s + 8 kbit/s (payload)

SDSL and SHDSL Standardization

Start Up Procedure

- **Activation:**
  - Basic structure of HDSL2 activation sequence
- **Preactivation:**
  - g.hs

Management

- Clear eoc channel
- HDSL2 channel proocol

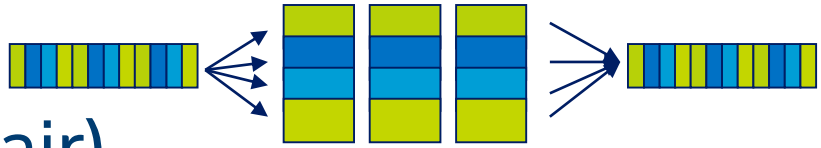
ITU-T G.991.2 Annex F&G (SHDSL.bis) Higher data rates

Standard Part of G.992.1	Data rates [kbps]	TC-PAM Levels (Bits / Symbol: Payload+OH)	B-Channels Z-Bits	Symbol Rates [kbaud]
Annex A+B (Standard SHDSL)	192..2312	16 (3+1)	3B + 0Z .... 36B + 1Z	66,7 ... 773,3
Annex F+G (SHDSL.bis)	192..3840	16 (3+1)	3B + 0Z .... 60B + 0Z	66,7 ... 1282,7
	768...5696	32 (4+1)	12B + 0Z .... 89B + 0Z	194 ... 1426

ITU-T G.991.2 Annex F&G (SHDSL.bis) Enhanced G.994.1 (G.hs) startup

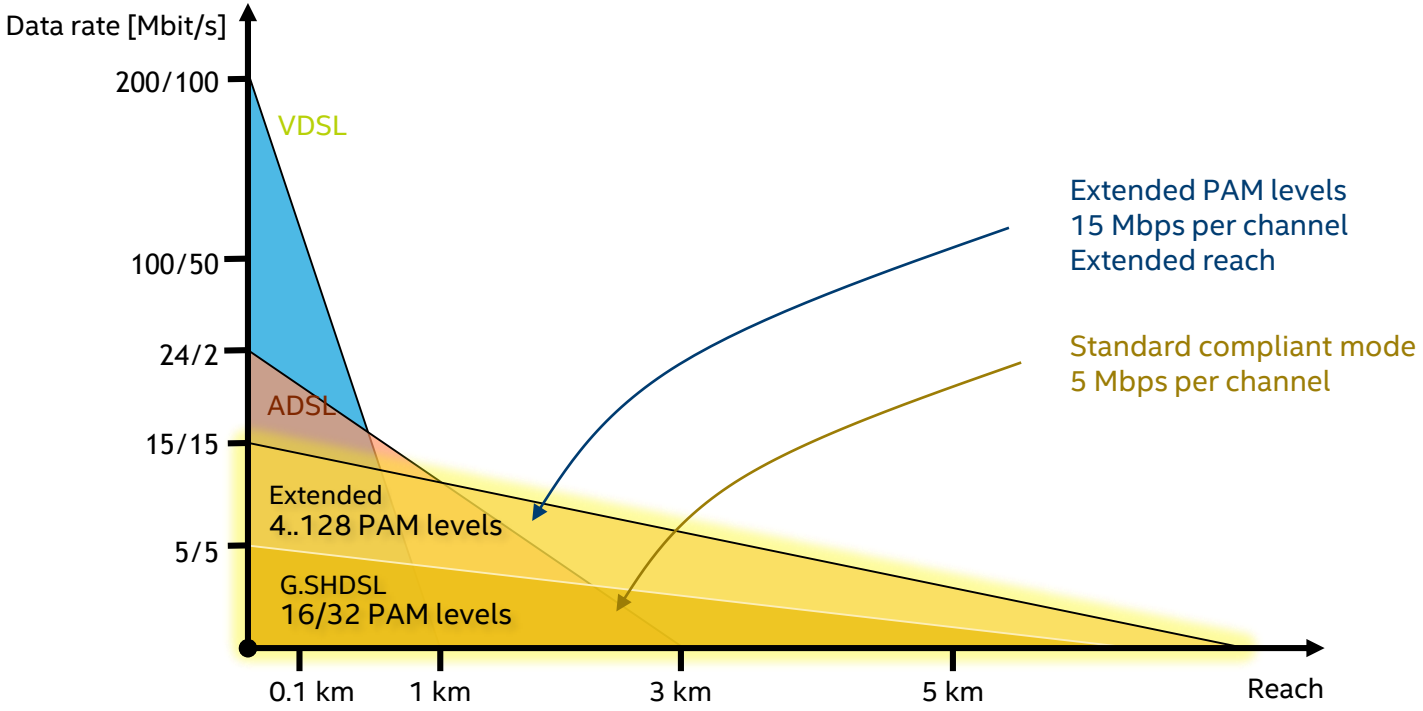
G.992.1 SHDSL (old) Standard	Caplist Version 1 -Bit mask for Baserates and Subrates -Enabling each single baserate and subrate -Bit mask applied to TCPAM-16 only
Extension for Annex F+G	Caplist Version 2: contains additionally -Ranges of Baserates per coding -3-tuple per coding TCPAM-16 and TCPAM-32 (min, max, step) Example: (40,70,10) means: 40x64kbps, 50x64kbps, 60x64kbps, 70x64kbps -Overlap of ranges is possible

ITU-T G.991.2 (SHDSL.bis) Multi-Channel bonding (M-Pair)

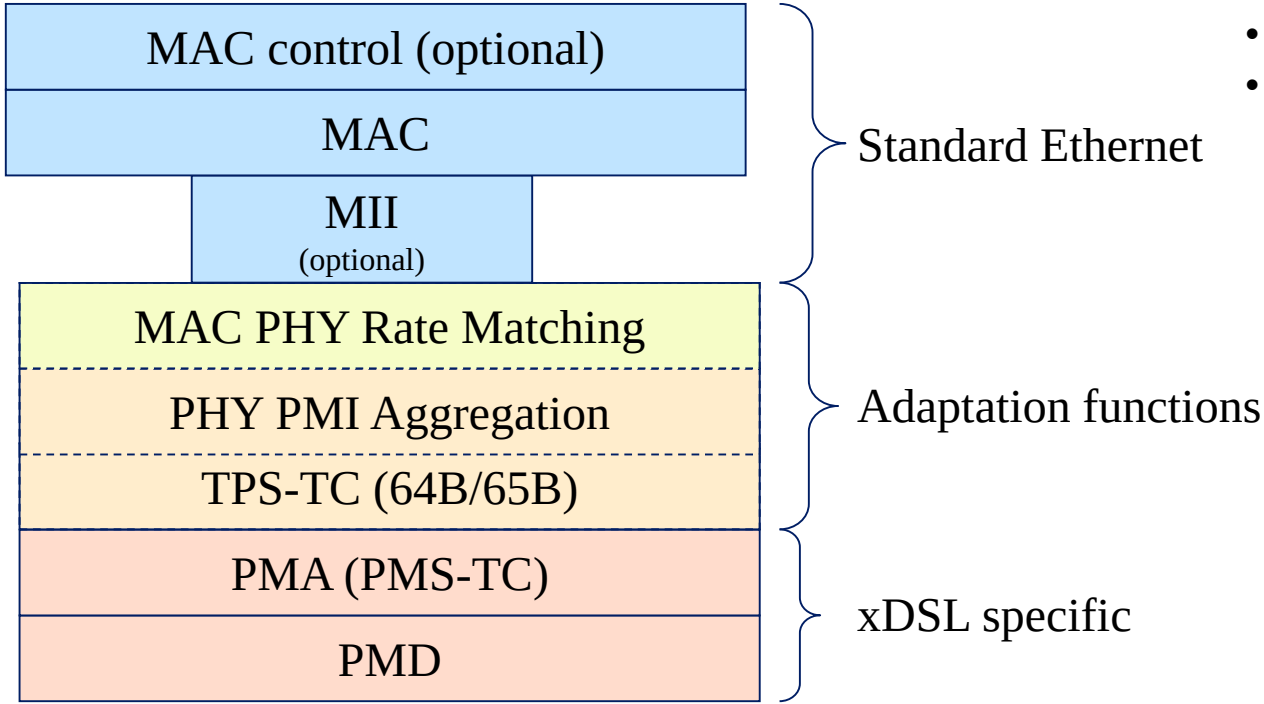


Standard Part of G.992.1	Line Bonding	Bonding Level	Interleaving	Interleaving Order of Subchannels
Annex A+B (Standard SHDSL)	4-wire	OSI-Layer 1	Byte Interleaving	Master / Slave
add-ons in Annex F+G (SHDSL.bis)	M-Pair (M=1,2..4)	OSI-Layer 1	Byte Interleaving	Interleaving acc. to negotiatioin in Activation Frame

xDSL rate/reach performance compared



ETHoverDSL @ IEEE 802.3ah (EFM=Ethernet First Mile)



New and edited chapters (SHDSL relevant)

- Clause 30
- Clause 45
- Clause 57
- Clause 61
- Clause 63

MAC PHY Rate matching

Rate Matching

Adapts the MAC/MII bit-rate (100Mbps) to the lower (aggregate) PHY bit-rate(s)

MAC is operated in half-duplex mode

- Note: It should still be able to transmit and receive simultaneously

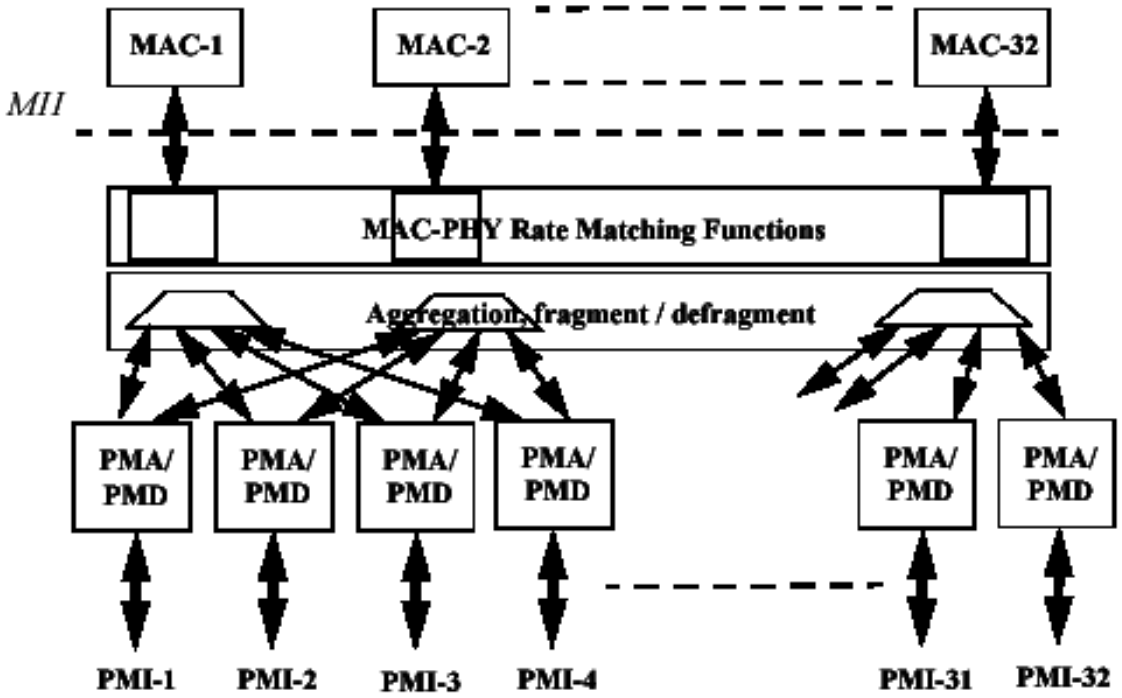
CRS function is used by the PHY to prevent MAC from sending another MAC frame

Preamble and SFD are removed

PHY needs to buffer one maximum length frame (i.e. 1522 Bytes) in both directions

PHY PMI Aggregation Function (PAF)

PAF



PHY PMI Aggregation Function (PAF)

PAF

Provides a flexible mapping of a MAC to different PHYs

Purpose is to increase the bandwidth and to provide redundancy

PAF will be negotiated using g.994.1 (2 Phases) *)

Implementation is PHY specific

- Combination of 10PASS-TS and 2BASE-TL theoretically possible

Restrictions

- Speed ratio between fastest and slowest link must be < 4
- Differential delay <15000 bit times
- Frame size between 64 and 512 Bytes with a 4 Byte granularity
- Up to 32 PHYs per MAC

Transmit sequence can be vendor specific

*) we'll have a dedicated session on EFM handshake and PAF

Encapsulation (64B/65B)

TPS-TC

Input is either a MAC frame or a PMI aggregation fragment

A 32bit(SHDSL)/16bit (VDSL) FCS will be calculated and added at the end of each frame/fragment (“TC-frame”)

This TC-frame is chopped into 64-Bytes packets

One Sync-Byte is added at the beginning to indicate the content of the following 64-Bytes packet resulting in a 65-Bytes “Codeword”

- Sync-Byte $0F_{16}$ indicates that all 64 following bytes are data from the very same data frame
- Sync-Byte $F0_{16}$ requires a look at the first payload bit D1
  - If Zero, wait for a frame start Byte
  - If not Zero it contains the position of the last Byte of the frame

IEEE EFM Physical layers for copper lines

PMD

10PASS-TS

- **10** Mbps, **PASS**band, **T**wisted Pair, **S**hort Reach
- Using VDSL2 technology
- Based on ANSI T1.424/trial use standard

2BASE-TL

- **2**Mbps, **BASE**-band, **T**wisted Pair, **L**ong Reach
- Based on SHDSL technology
- Using ITU-T G.991.2.bis standard
- Allowing 32-PAM coding for higher bit-rates

10PASS-TS Objectives

PMD

- To provide 100 Mb/s data rate at the MII.
- To provide ~10Mb/s encapsulated packet data rate at the α(β) interface.
- To provide full duplex operation.
- To provide for operating over non-loaded voice grade twisted pair cable at distances up to 750 m (2.5 kfeet).
- To provide a communication channel with a mean bit error rate, at the α(β) interface, of less than one part in 10^7 with 6 dB noise margin.
- To provide optional support for operation on multiple pairs
- All band-plans are allowed
- To have only one line code

2BASE-TL Objectives

PMD

- To provide 100 Mb/s data rate at the MII.
- To provide ~2Mb/s encapsulated packet data rate at the α(β) interface.
- To provide full duplex operation.
- To provide for operating over non-loaded voice grade twisted pair cable at distances up to 2,700 m (9 kfeet).
- To provide a communication channel with a mean bit error rate, at the α(β) interface, of less than one part in 10^7 with 5 dB noise margin.
- To provide optional support for operation on multiple pairs
- All data rates from 192 kbps up to 5696 kbps in a 64kbps granularity are supported
- Focus is on 512, 704, 1024, 2048, 3072 and 5696 kbps

*) Bonding on OSI-Layer 1, Byte interleaving

**) Bonding on OSI-Layer 2, Payload Interleaving

Standards Summary

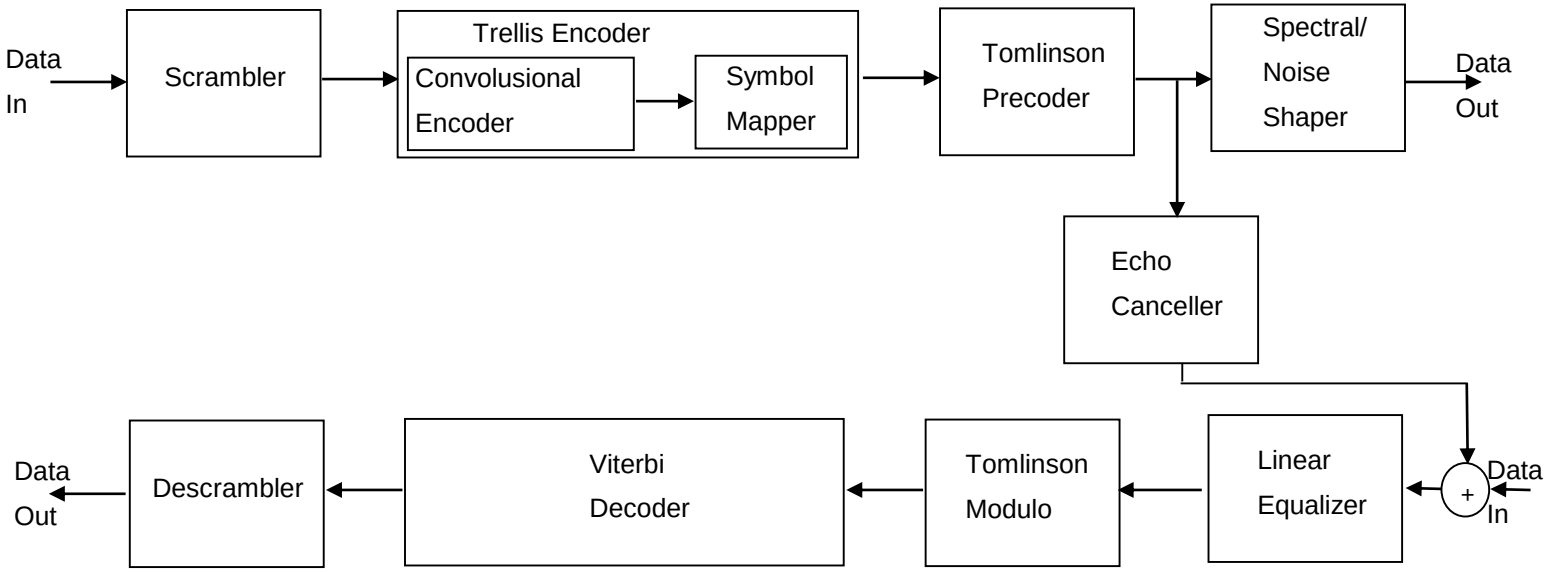
Comparison of Symmetrical Data Technologies

	SDSL	SHDSL	SHDSL.bis	EFM 2Base-TL
Data Rate	192kbps - 2.3Mbps	192kbps - 2.3Mbps or 384kbps – 4.624Mbps	192..5696 kbps per pair	
Pairs	1	1 or 2 *)	1-4 *)	1..32 **)
Line Code	2B1Q	TC PAM 16	TC PAM 16/32	TC PAM 16 / 32
EOC	Proprietary	20-bit HDLC-type		
Pre-activation	Proprietary	Standard Based	G.994.1 (g.hs)	
Rate Adaption	Yes	Yes		
Power Back-off	No	Yes		
Repeaters	No	Yes		
Timing	Synchronous	Synchronous + Plesiochronous		pref. Synchronous
Span Power	Yes	Yes		

PHYSICAL LAYER

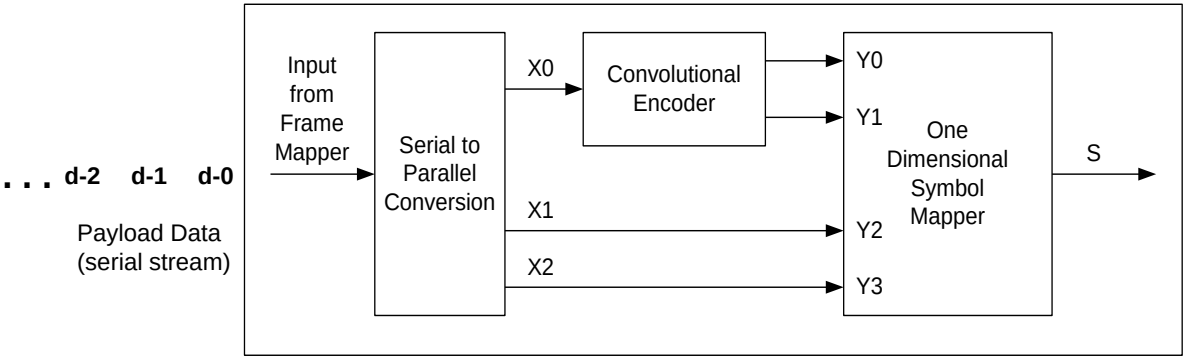
How is the SHDSL PHY defined?

Physical Layer Definition



PHY-TX: Trellis Encoder

Trellis Encoder
– Adds redundancy
– Output depends on state and input (512 states)
– Increases SNR
– 3/4 bits in – 16/32-level PAM pulse out



Level S:
x*1/16

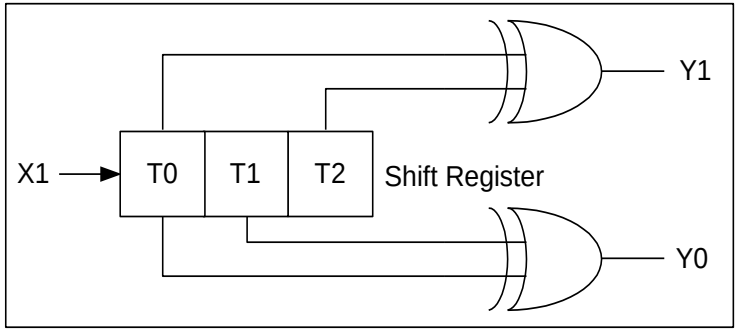
Mapper: Bit-to-level mapping

-15	-13	-11	-9	-7	-5	-3	-1	1	3	5	7	9	11	13	15	
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	Y3
0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	Y2
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	Y1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	Y0

Trellis Encoder Output

PHY-TX: Convolutional Encoder

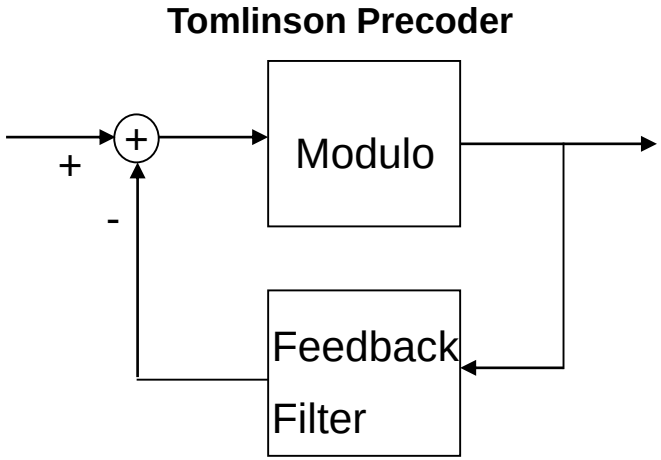
Principle of a convolutional encoder



Block Diagram of a simple convolutional encoder

A sequence of bits enters the encoder at the input X1. After one delay the actual bit proceeds from T0 to T1, the first memory stage. After each delay the bits are forwarded to the next stage. Y1 is the result of an XOR multiplication of T0 and T2 and Y0 respectively of T0 and T1.

PHY-TX: Tomlinson-Harashima Precoder



The idea of precoding is to move the cancellation of the post-cursor ISI to the transmitter where the past transmitted symbols are known exactly. So the post-cursor impulse response must be known precisely at the transmitter.

Tomlinson Precoder

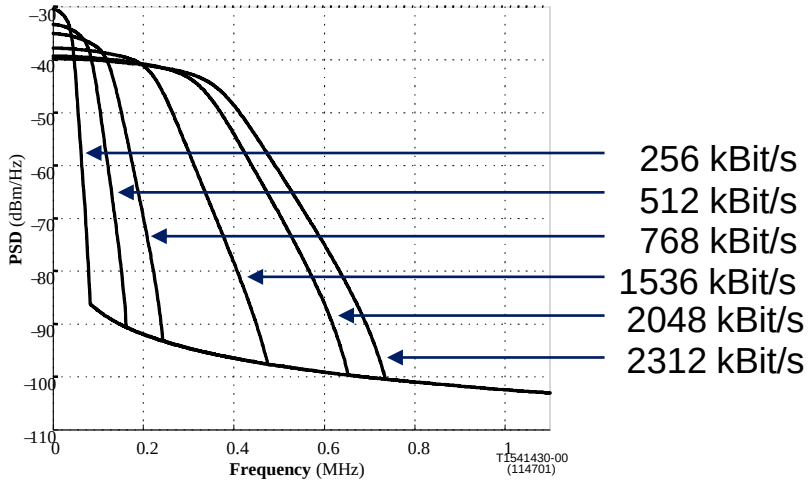
– Removes **I**nter-**S**ymbol **I**nterference (**D**ecision - **F**eedback **E**qualizer function)
– Modulo-n Filter
– Results in expanded symbol set

PHY-TX: Spectral Shaper

- Frequency domain
- PSD mask is independent of number of PAM-levels
- PSD mask only depends on symbol rate
- Total transmit power constant over the data rate

Spectral Shaper

- The PAM signal has infinite bandwidth and cannot be sent by a real transmitter.
- The shaper performs the filtering on the symbol sequence needed to produce a continuous-time signal for transmission over the channel.



S(H)DSL PSD Definition

- Frequency domain
- PSD mask is independent of number of PAM-levels
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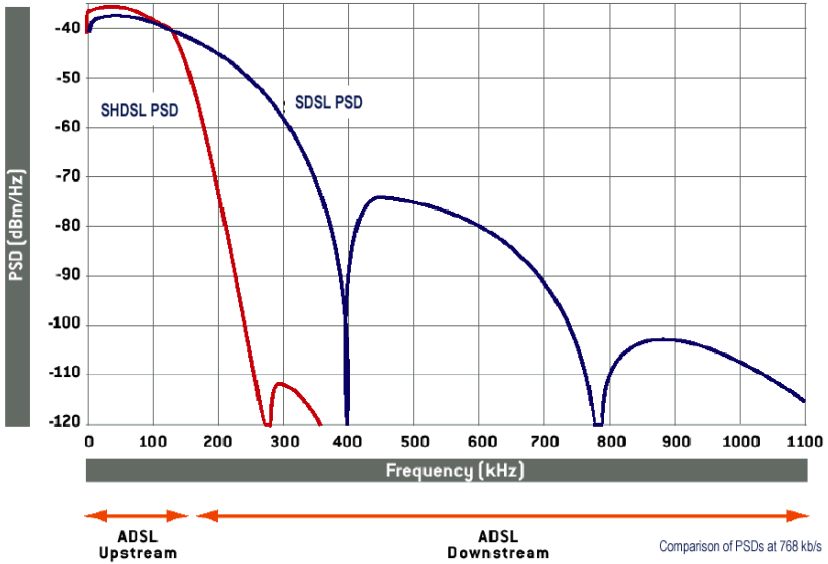
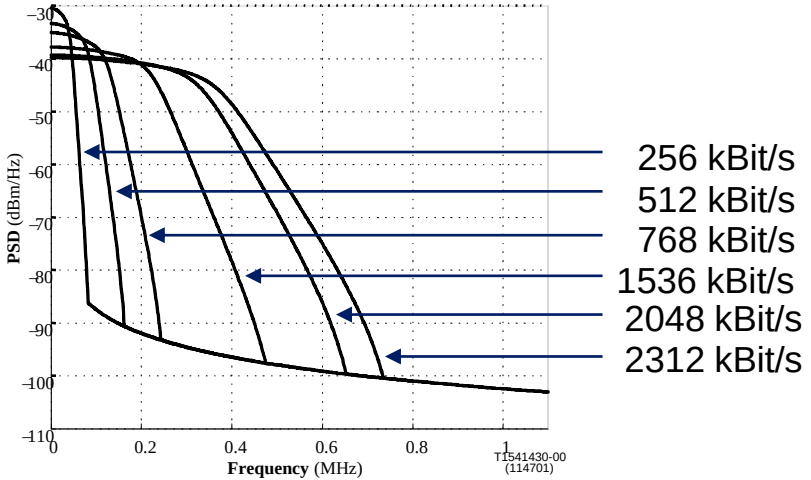
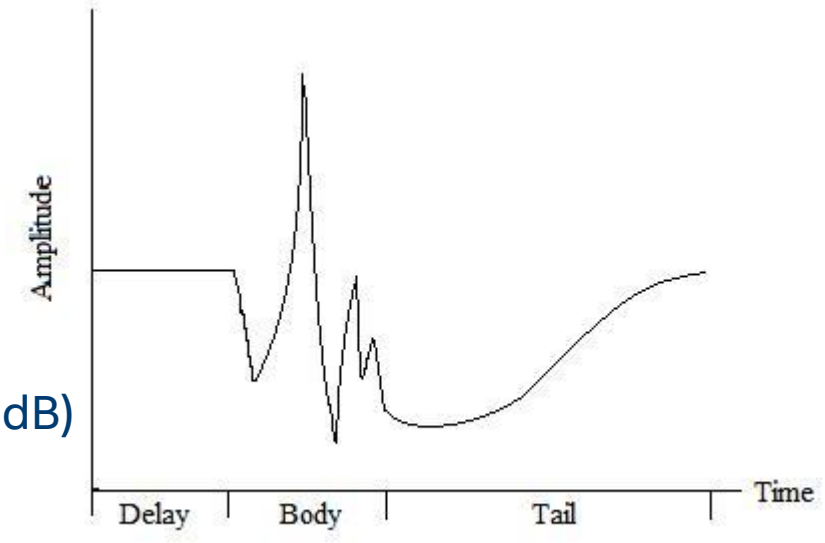




PHY-RX: Echo Cancellation



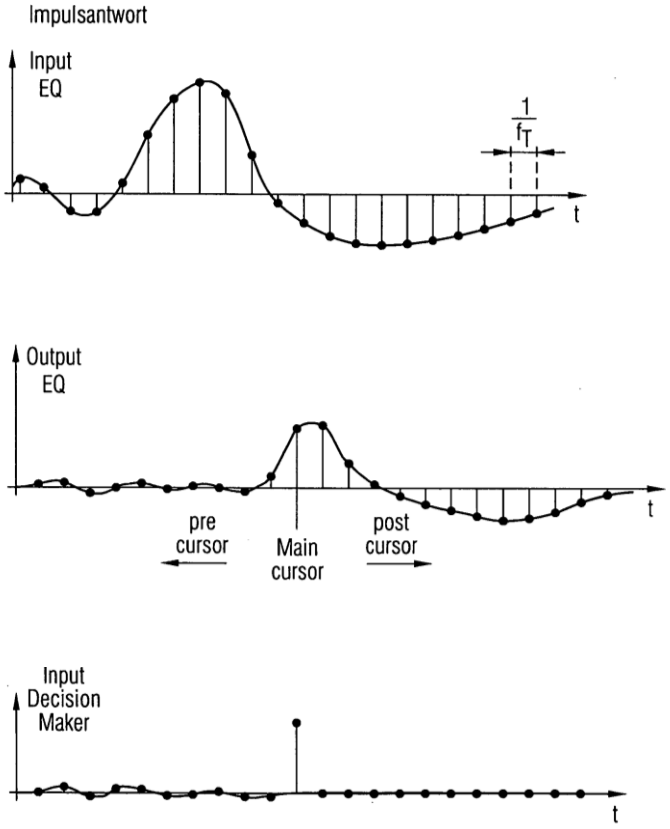
Typical Echo Impulse Response:

- Very long
- High dynamic range on long loops (60+dB)
- 200+ taps
- Effects of bridged taps visible and important
- Required due to full-duplex, spectrum overlapping baseband signaling
- Requires loop-timing

PHY-RX: Equalizer

Equalizer Function for an SHDSL Transceiver

- Training: DFEQ, converge, transform into THP
- Showtime: THP@TX + LEQ@RX
- Options: FSEQ, T-Spaced EQ
- Enhancements:
  - Noise-Whitening/Prediction
  - Viterbi-Equalizer

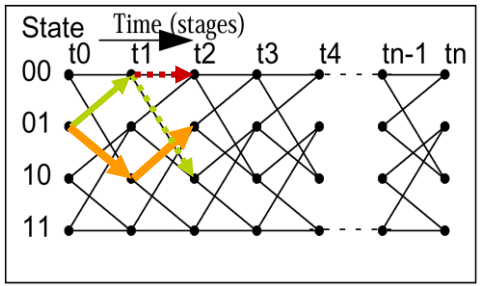


PHY-RX: Viterbi Decoder

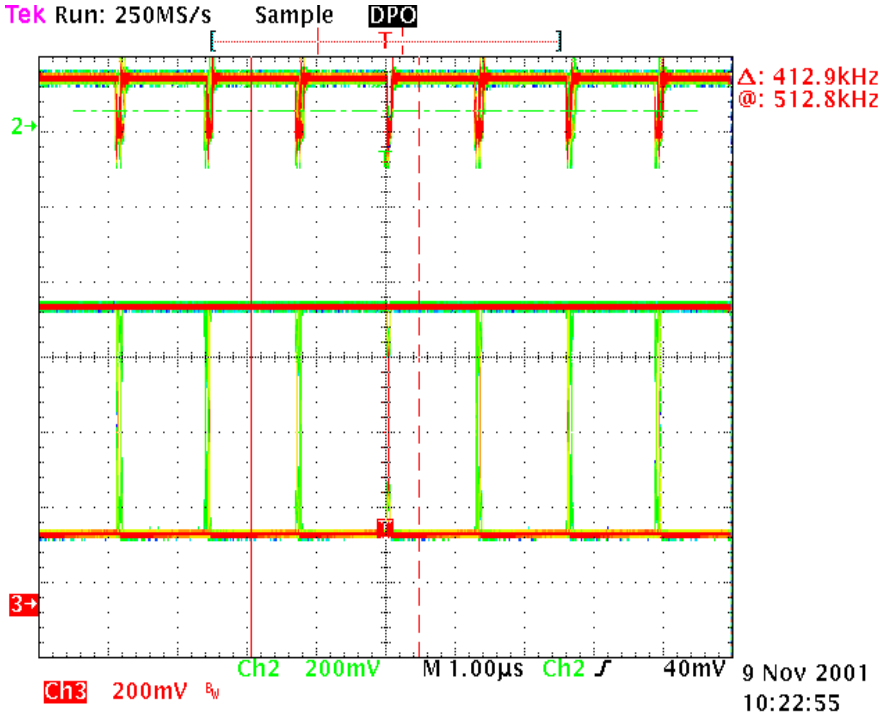
Viterbi Decoder

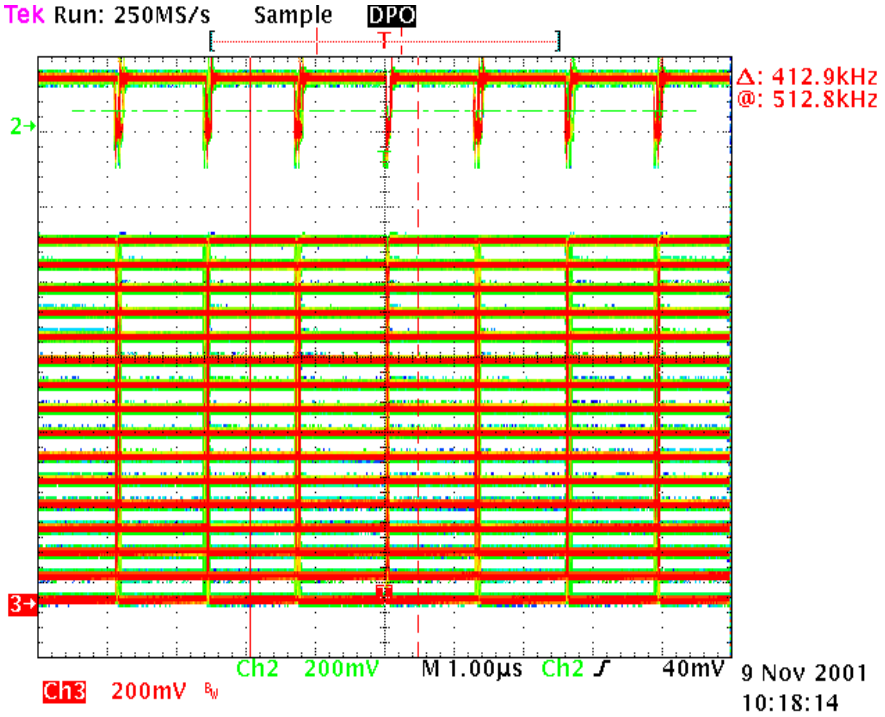
uses the Viterbi algorithm, it is used not only to decode convolutional codes but also to produce the maximum-likelihood estimate of the transmitted sequence through a channel with inter-symbol interference (ISI).

receives a sequence of bits and attempts to find a path in the trellis diagram with an output digit sequence that mostly agrees with the received sequence.



2/16-Level PAM at Receveiver @ baud rate

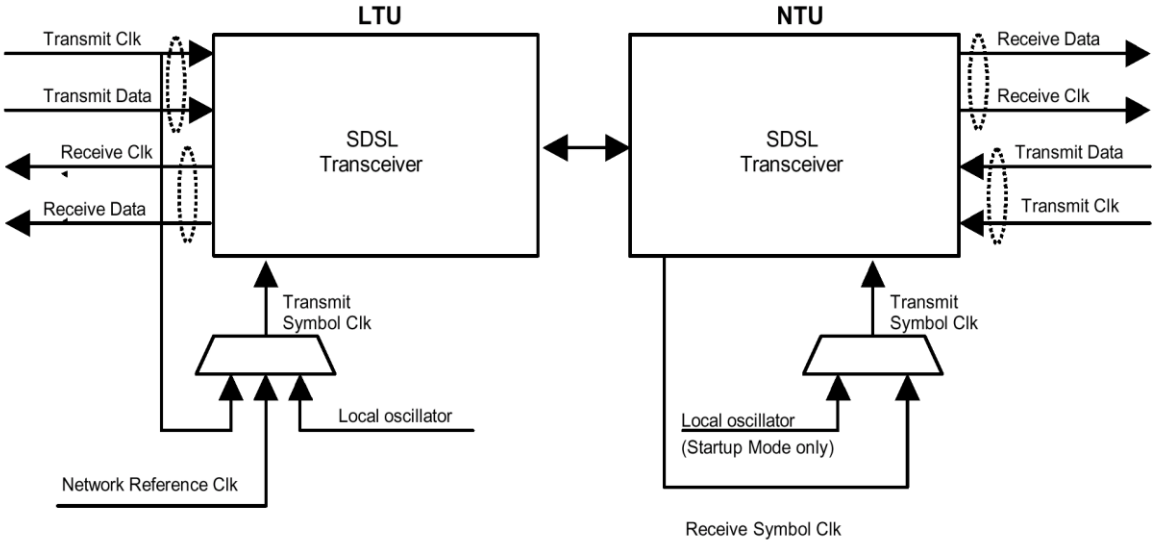




CLOCKING / LOOP TIMING

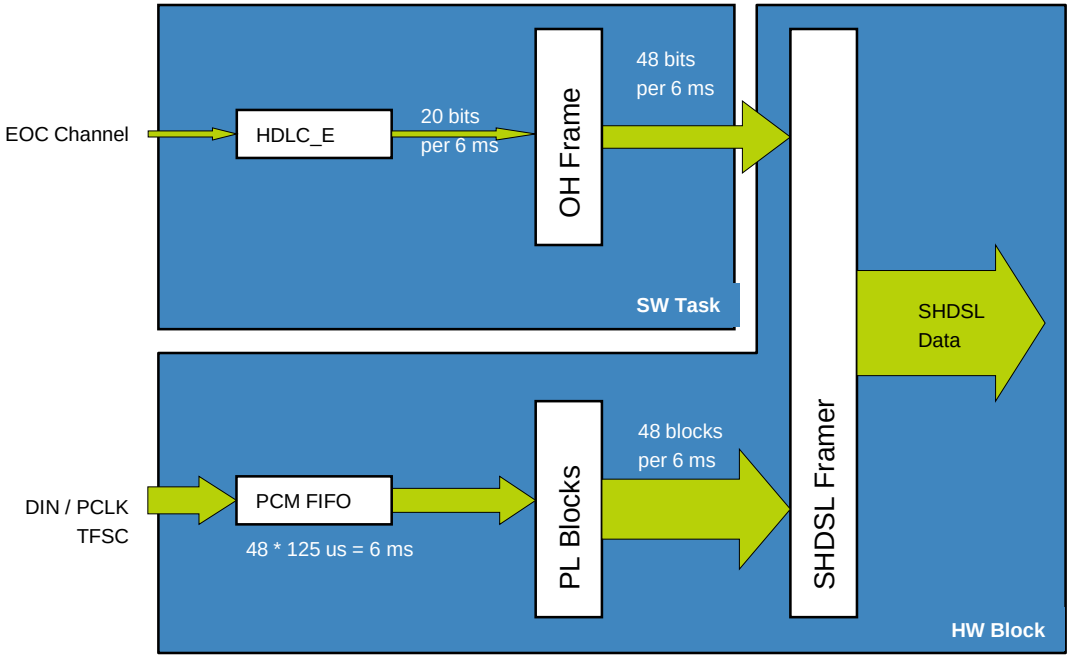
SHDSL Loop-Timing & Clocking Modes

Mode No.	LT symbol clock source	NT symbol clock source	Example application	Mode
1	Local oscillator	Received symbol clock	"Classic" HDSL	Plesiochronous
2	Network reference	Received symbol clock	"Classic" HDSL with embedded timing reference	Plesiochronous with timing reference
3a (see note)	Transmit data clock	Received symbol clock	Main application is synchronous transport in both directions	Synchronous
3b (see note)	Transmit data clock	Received symbol clock	Synchronous downstream transport and bit-stuffed upstream is also possible	Downstream: synchronous Upstream: plesiochronous
NOTE:	Both modes 3a and 3b are possible with the same clock sources depending on clock tolerances.			



FRAMING

Data Structure Block Diagram

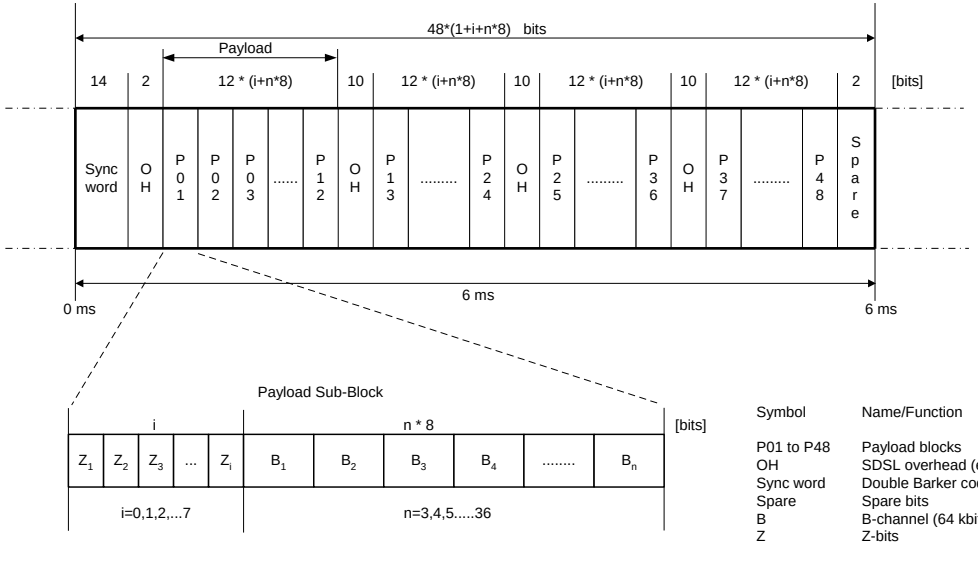


SDSL and SHDSL Frame Format (1)

Frame Structure

ETSI-SDSL frame structure consistent with ITU G.shdsl frame structure

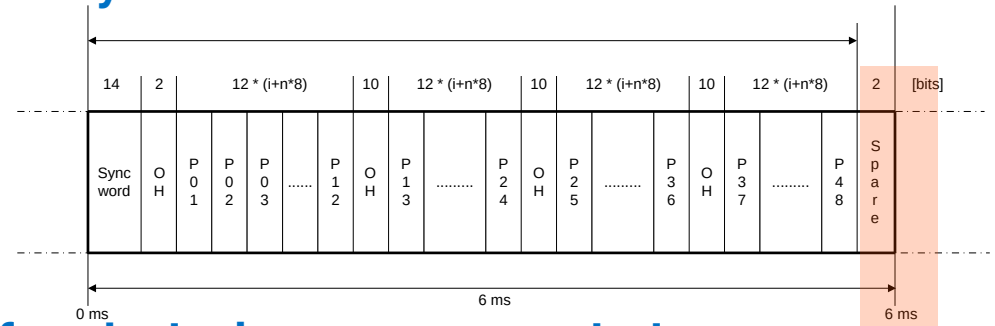
- 14 bit sync word
- 20 bit embedded eoc channel
- 6 bit crc
- 4 fixed indicator bits



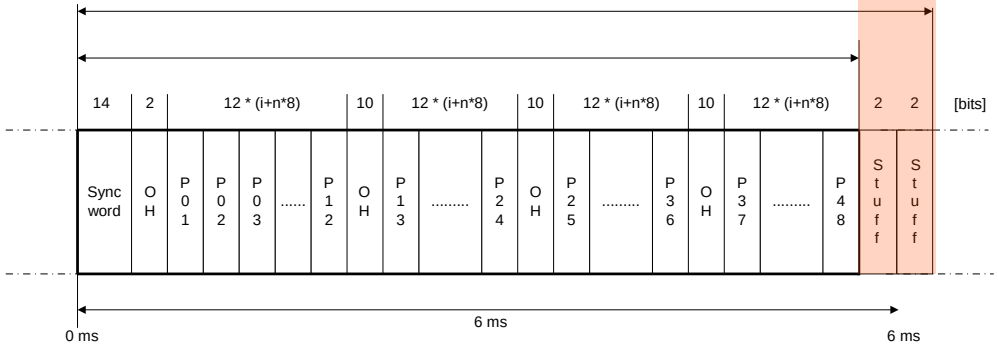
Symbol	Name/Function	
P01 to P48	Payload blocks	
OH	SDSL overhead (eoc, crc,...)	
Sync word	Double Barker code	
Spare	Spare bits	
B	B-channel (64 kbit/s),	n = 3,4,5...,36
Z	Z-bits	i = 0,1,2,.....,7
		i = 0: no Z-bits

SDSL and SHDSL Frame Format (2)

SDSL frame for synchronous transmission



SDSL frame for plesiochronous transmission



EOC Message Frame Structure (HDLC)

Performance FOM:

- SNR
- Loop Attenuation
- BER
- Sync-Status

Inventory

- Unit-ID
- Vendor

FLAG - 0x7E
FLAG - 0x7E
FLAG - 0x7E
FLAG (optional)
FLAG (optional)
Massage Segment: •Identification Field •Standard Information Field •Non-Standard Information Field
FCS (first octet)
FCS (second octet)
FLAG - 0x7E
FLAG - 0x7E
FLAG (optional)

LINK ACTIVATION / TRAINING

Activation / Link-Training

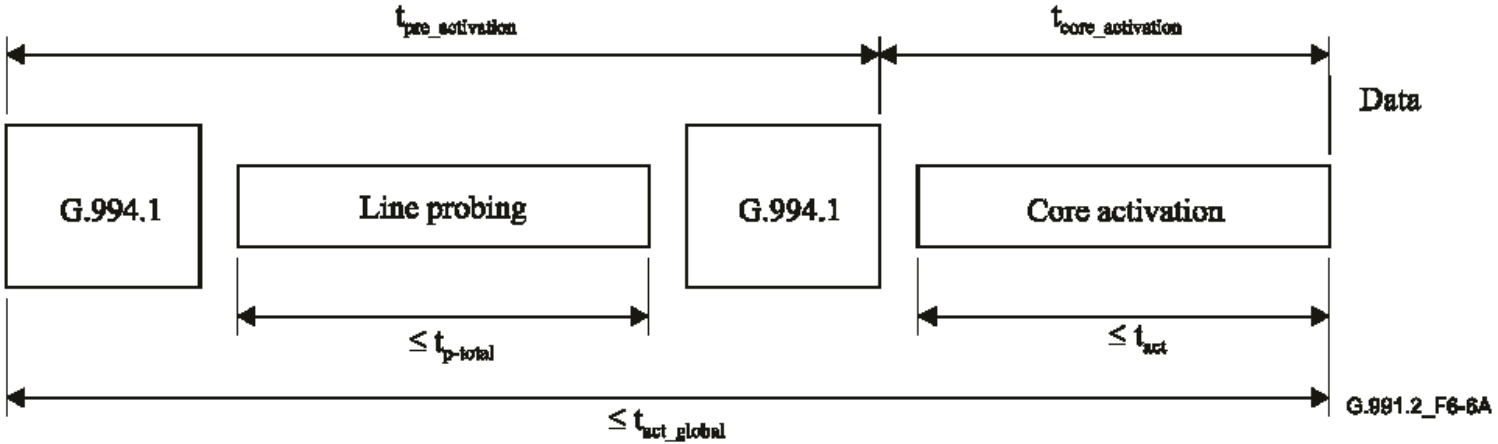
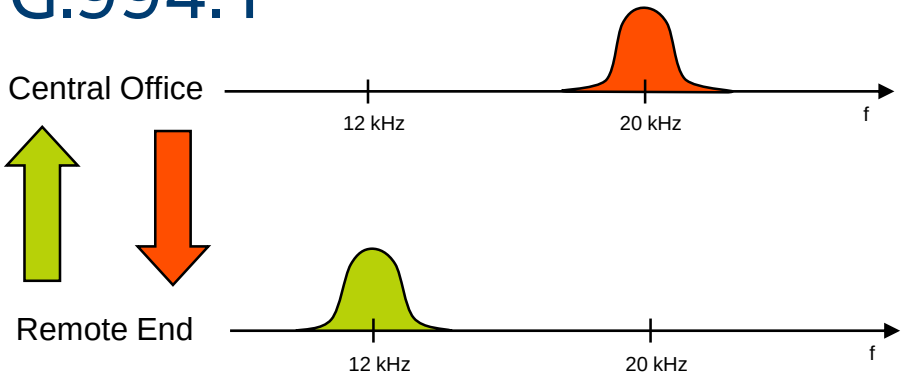


Figure 6-6a/G.991.2 – G.991.2 total activation sequence

G.944.1 Parameter Exchange

- Training Parameters
  - Max., Min. Brutto, Netto Data Rates
  - Max., Avg. Latency
  - Framing Parameters
  - Sync. Word
  - Clock, Timing Modes
  - Sym., Asym. PSD
- Stuff Bits
- Regenerators
- ATM, STM, HDLC/PTM …
- Vendor ID
- Line Probe
- Power Back Off (PBO)
- Non Standard Information …

G.994.1



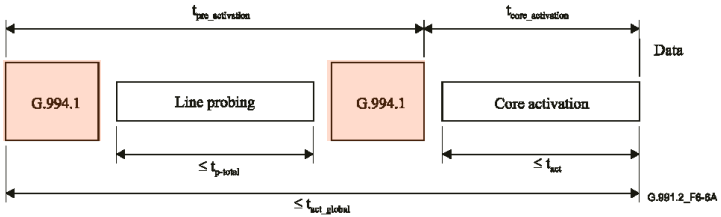
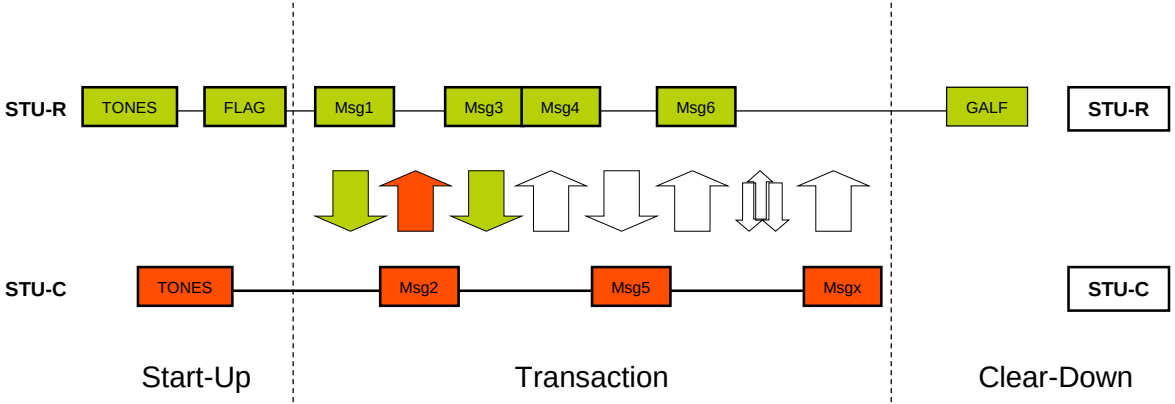


Figure 6-6a/G.991.2 – G.991.2 total activation sequence

Parameters:

- DPSK Modulation
- 800 Bits Per Second
- Frequency Division Multiplex
- Time Division Multiplex (Half Duplex)



Startup (G.991.2)
LineProbing

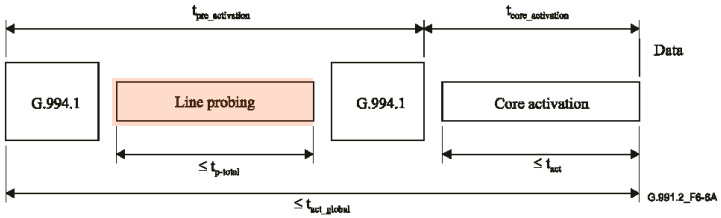


Figure 6-6a/G.991.2 – G.991.2 total activation sequence

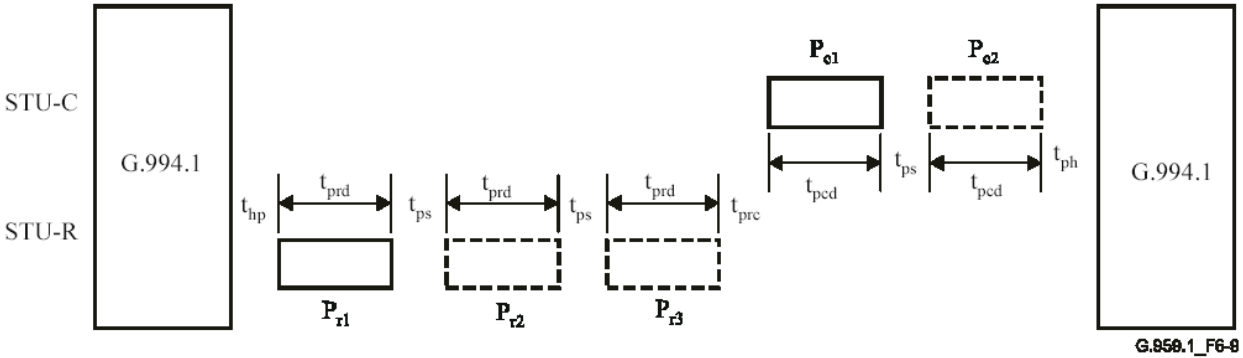


Figure 6-9/G.991.2 – Typical timing diagram for pre-activation sequence

- half duplex
- total duration ≤ $t_{p\text{-}total}$ =10s
- low number of probes (typ. 2..10)
- idle phases fix 200ms (±10ms)
- no full transceiver training (no hybrid, timing section, echo canceller etc. due to short probes
- Exact timing is listed in G.991.2, Chapter 6
- PMMS Probe timing depends on prior G.hs parameter exchange
- PMMS related restrictions apply

Startup (G.991.2)
Core Activation (Training)

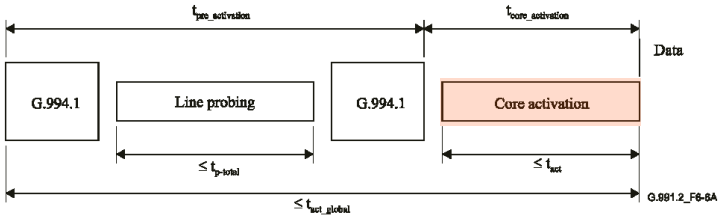
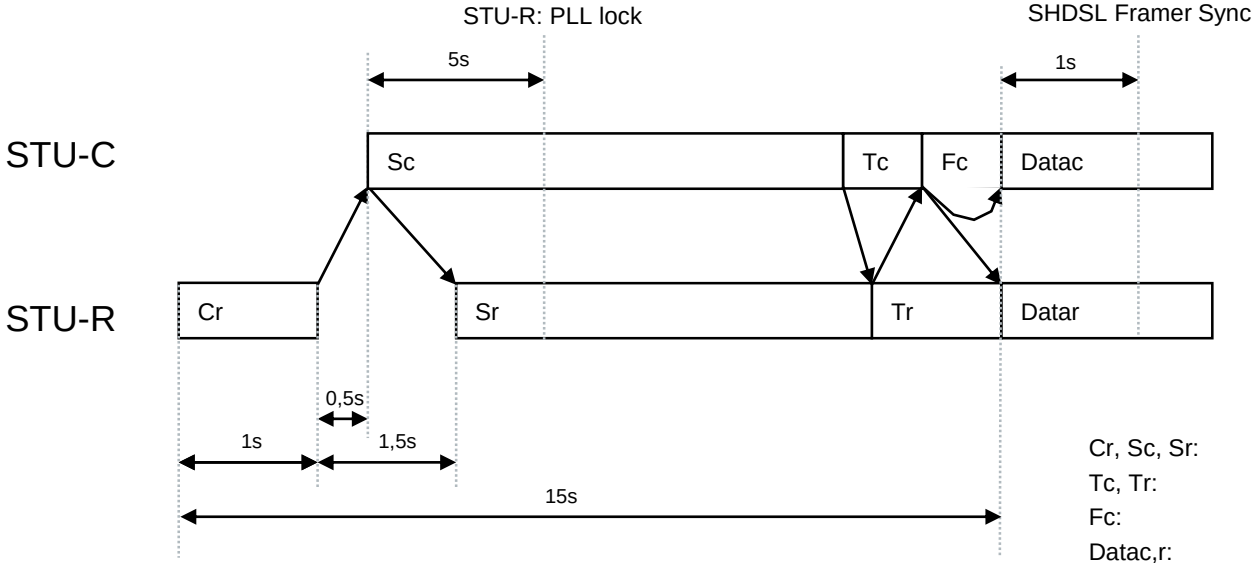
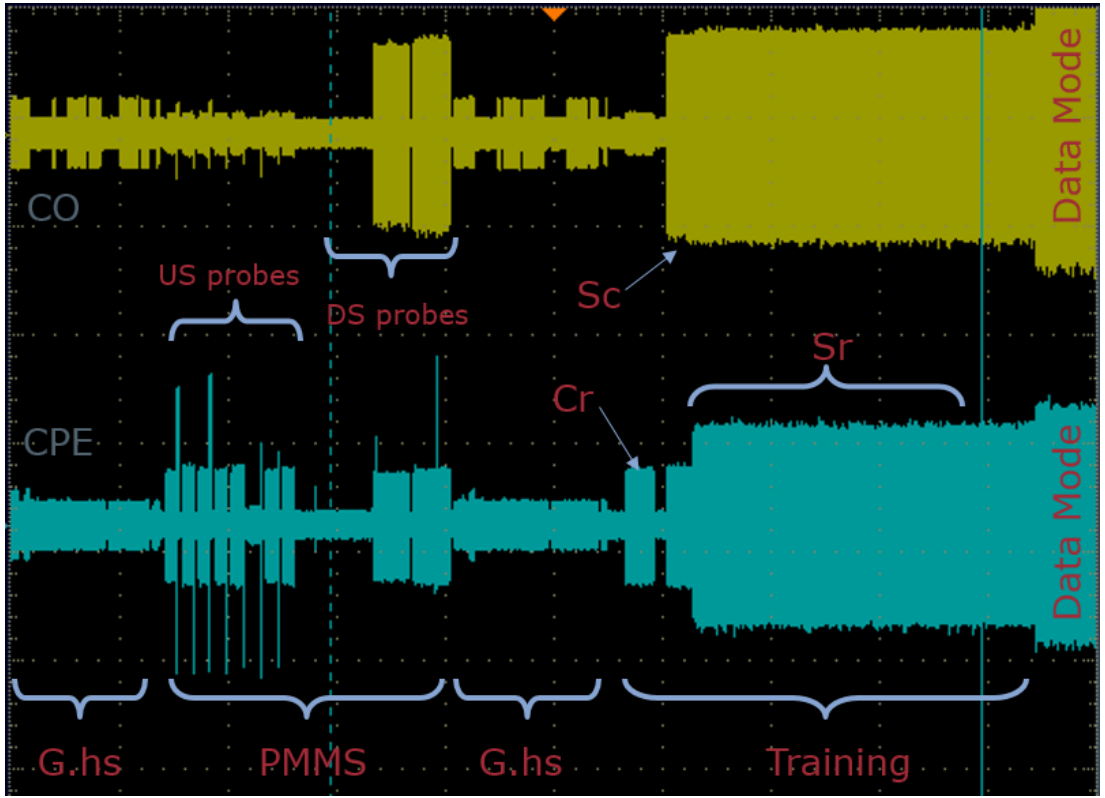


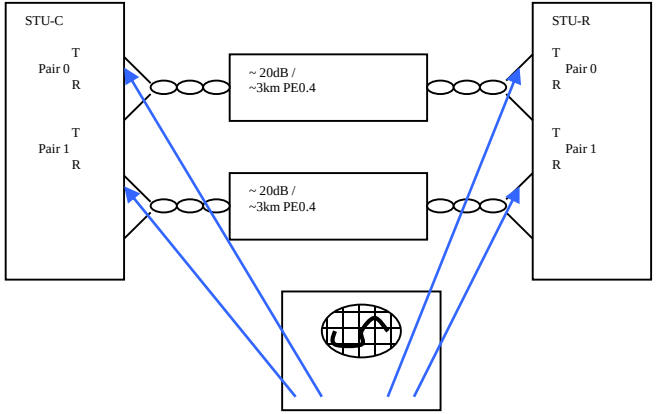
Figure 6-6a/G.991.2 – G.991.2 total activation sequence



Cr, Sc, Sr:	2-PAM (2 level scrambled ones) „Scrambled ones“
Tc, Tr:	2-PAM (2 level data) activation frames
Fc:	Activation frame with reversed sync word
Datac,r:	TC-PAM (multi level) data transmission
Framesync:	Transmission of payload data

Reference trace (2wire only)



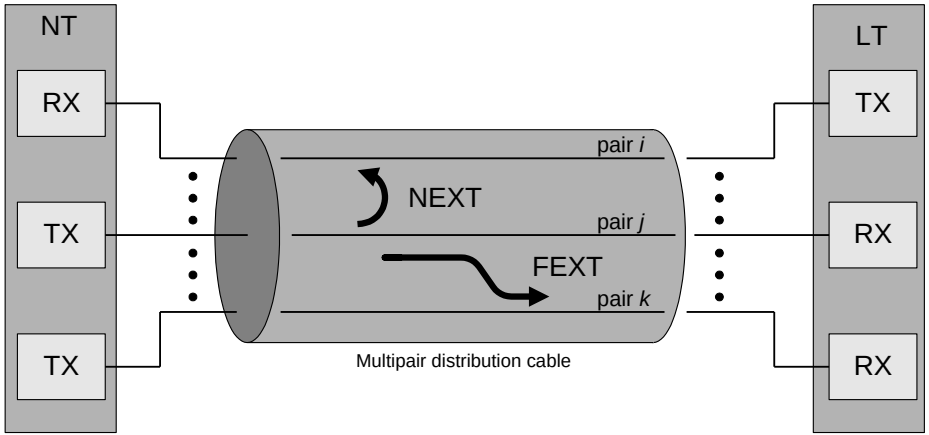


NOISE MODELS AND CHANNELS/CABLES

FSAN Noise Model

FSAN Noise Model

- FSAN = BT, France Telecom, KPN, DTAG, Telia, Telecom Italia, Swisscom, Korea Telecom
- Developed by operators
- New Noise model for SDSL and xDSL performance tests
- Combined noise of different scenarios in multipair cable



FSAN Noise Models

Model A
(High Penetration Scenario)

- 90 SDSL
- 90 ISDN/2B1Q
- 40 HDSL/2B1Q (2-pair)
- 90 ADSL over POTS
- 90 ADSL over ISDN

Model B
(Medium Penetration Scenario)

- 15 SDSL
- 10 ISDN/2B1Q
- 4 HDSL/2B1Q (2-pair)
- 10 ADSL-lite
- 5 ADSL over ISDN

FSAN Noise Models

Model C (Legacy Scenario)

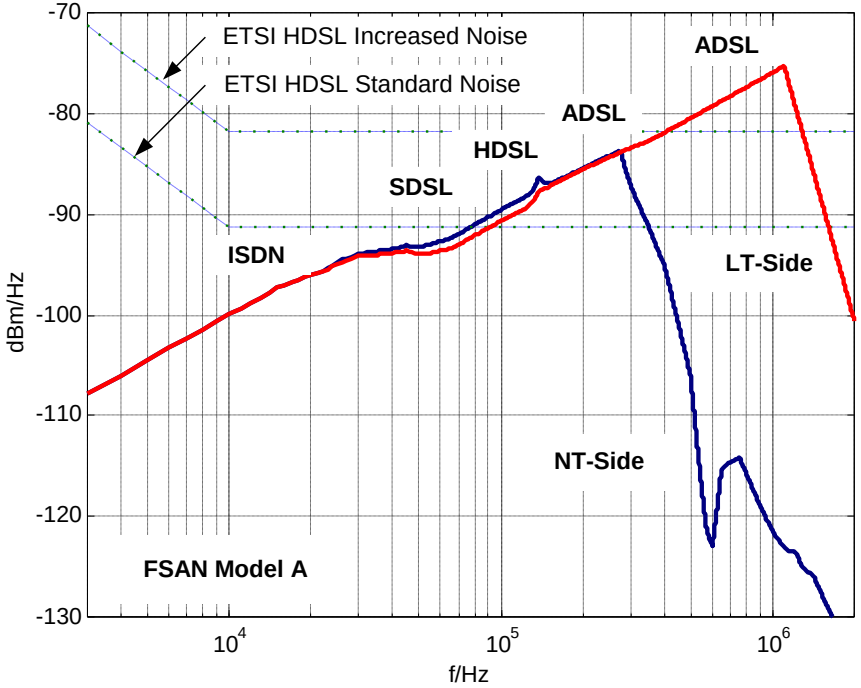
- 15 SDSL
- 10 ISDN/2B1Q
- 4 HDSL/2B1Q (2-pair)
- 10 ADSL-lite
- 5 ADSL over ISDN
- 4 ISDN-PRI/HDB3

Model D (Referece Scenario)

- 49 SDSL

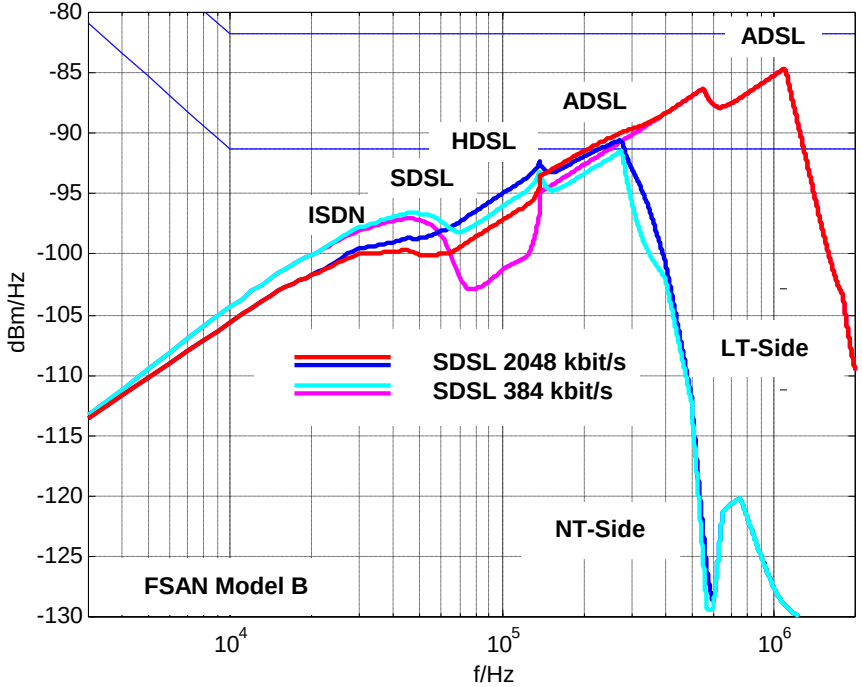
FSAN Noise Models

FSAN Model A: High Penetration Scenario



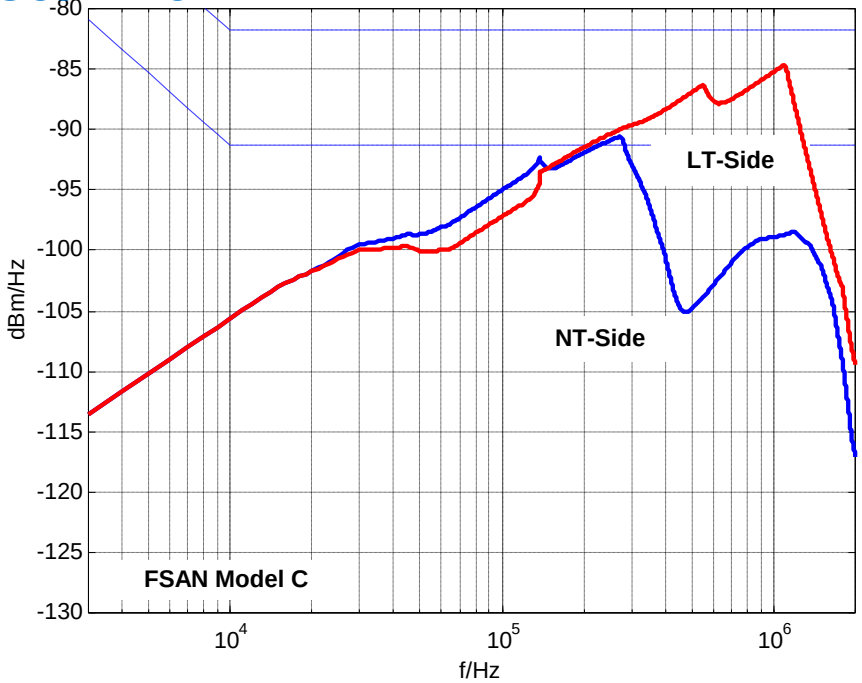
FSAN Noise Models

FSAN Model B: Medium Penetration Scenario



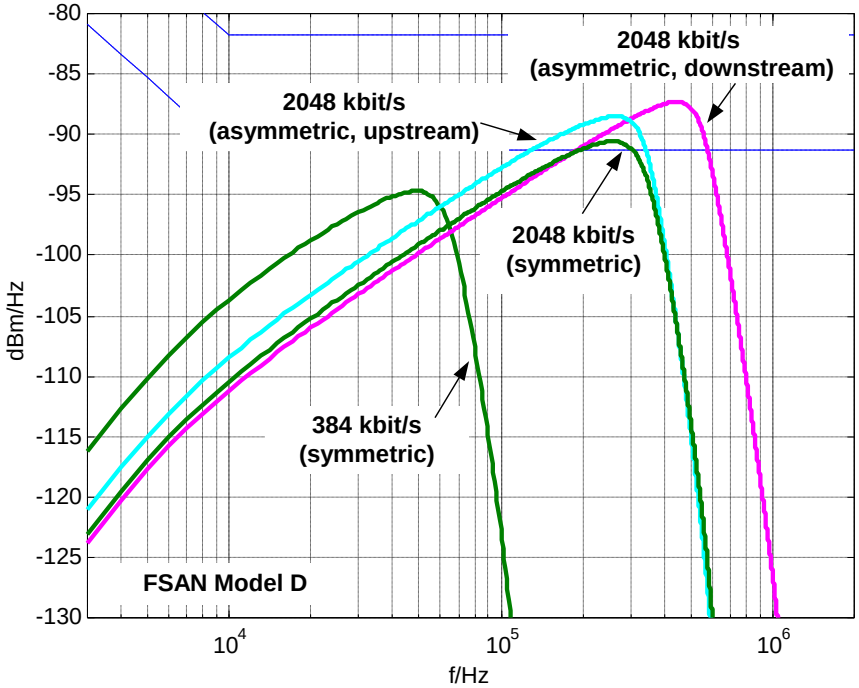
FSAN Noise Models

FSAN Model C: Legacy Scenario



FSAN Noise Models

FSAN Model D: 49 SDSL Disturbers



Other Impairments

- Bridged Taps
- Wet Cables
- RFI
- Nonlinearities (Transformers)
- Correlated Noise (Viterbi Performance)

RATE VS. REACH PERFORMANCE

32/64-PAM Extended Rates Noise-Free at PE04

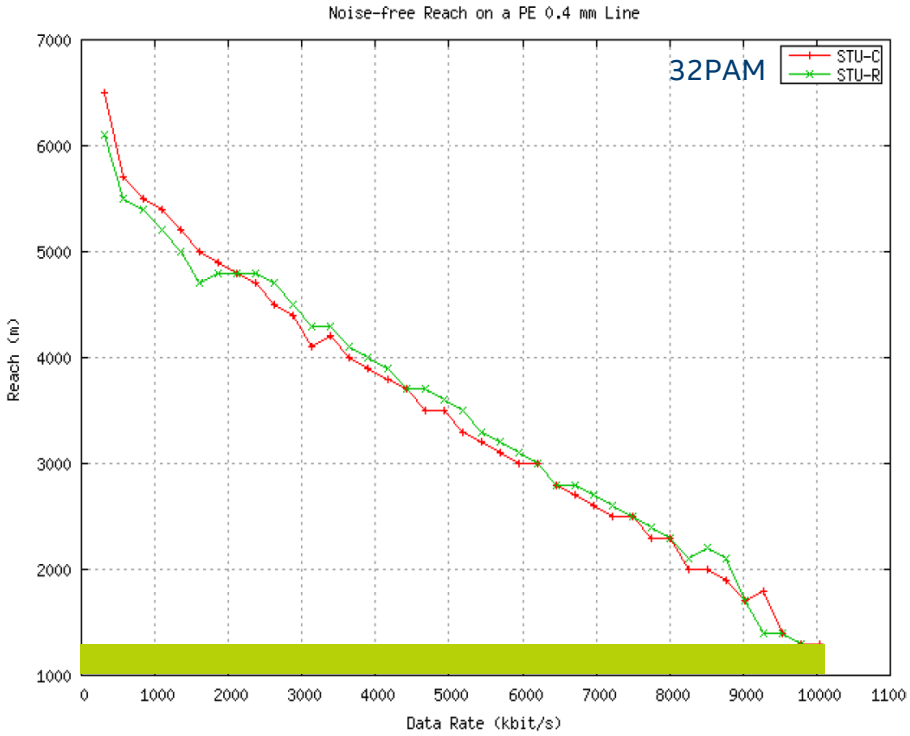


Figure 4 Noise-free Reach on a PE 0.4 mm Line

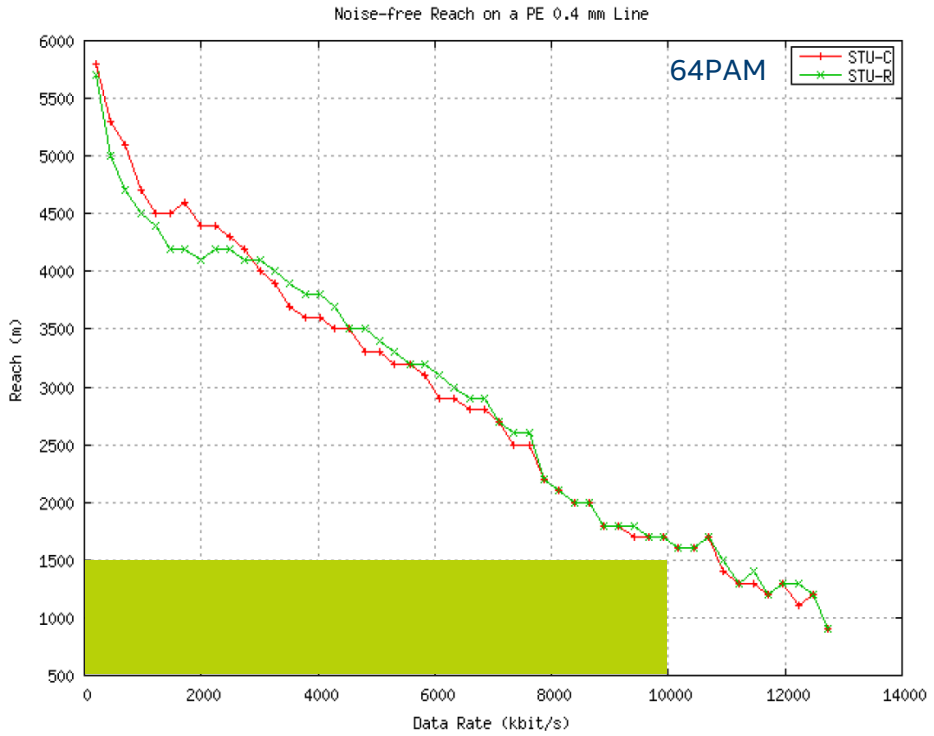


Figure 5 Noise-free Reach on a PE 0.4 mm Line

16/32-PAM Extended Rates FSAN-B at PE04

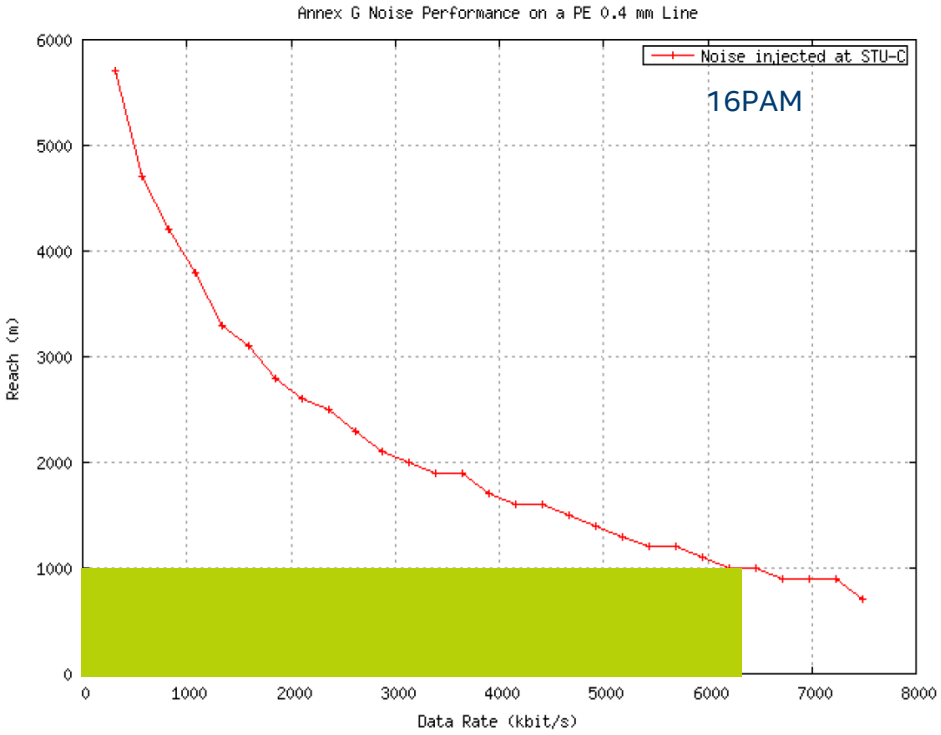


Figure 9 Annex G Reach on PE 0.4 for Extended PAM Rates under ETSI Noise B on a PE 0.4 mm Line

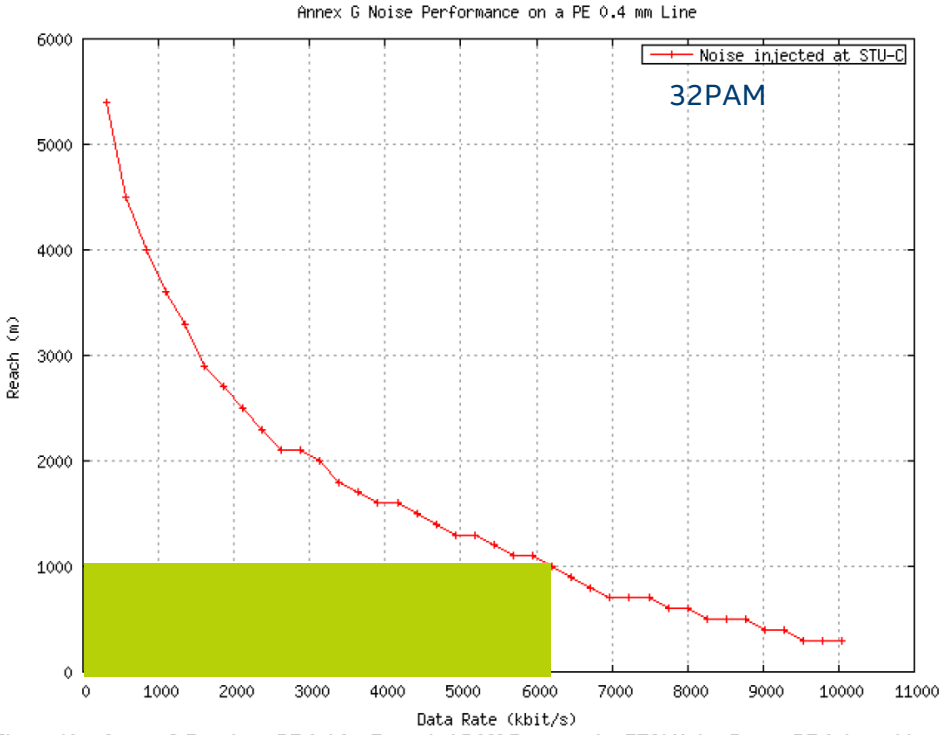
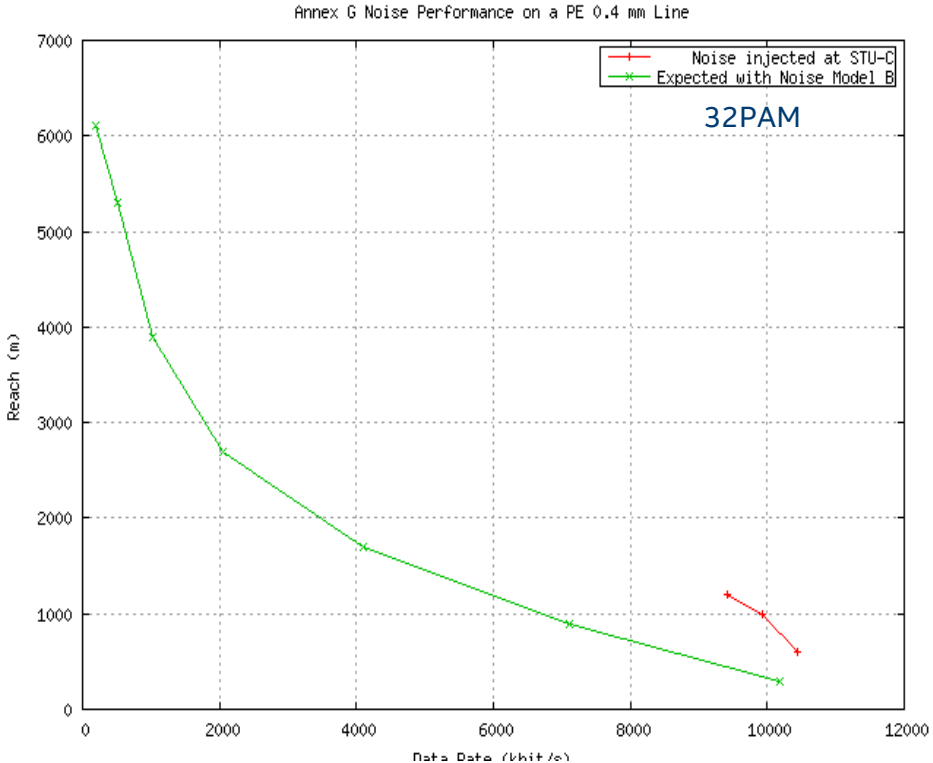
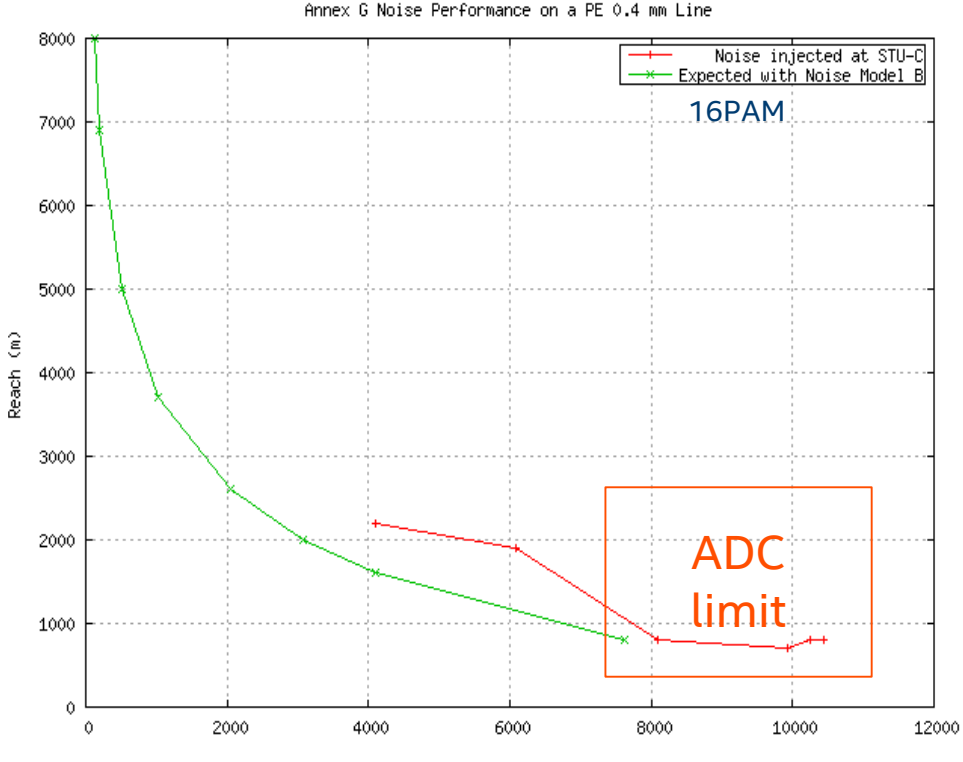


Figure 10 Annex G Reach on PE 0.4 for Extended PAM Rates under ETSI Noise B on a PE 0.4 mm Line

16/32-PAM Ext. Rates FSAN-D (49Self) at PE04





S(H)DSL APPLICATIONS

Remote Power-Feeding

Table 1 Power Feeding Ratings (cont'd)

Parameters		ETSI TS 101 524 V1.2.1[1)]	ITU G.991.2 (12/2003)
STU-R	Input voltage V_{in}	≤ 120 V	80 V ... 200 V
	Polarity	independent	independent
	Capacitance	not specified	≤ 15 µF
	permitted power consumption	≤ 2.1 W (if V_{in} < 70 V) ≤ 2.5 W (if V_{in} ≥ 70 V)	not specified

1) also refer to EN 60950

Table 3 Values Used

Parameter	Value
R_1	23 Ω ± 5%, 0.5W
R_2	20 Ω ± 5%, 0.5W
$R_{S1..4}$	2 Ω ± 5%
R_F	1.7 kΩ ± 5%
C_1	1 µF ± 10%, 250 V
C_2	1 µF ± 10%, 250 V
$C_{S1..4}$	220 nF ± 10%

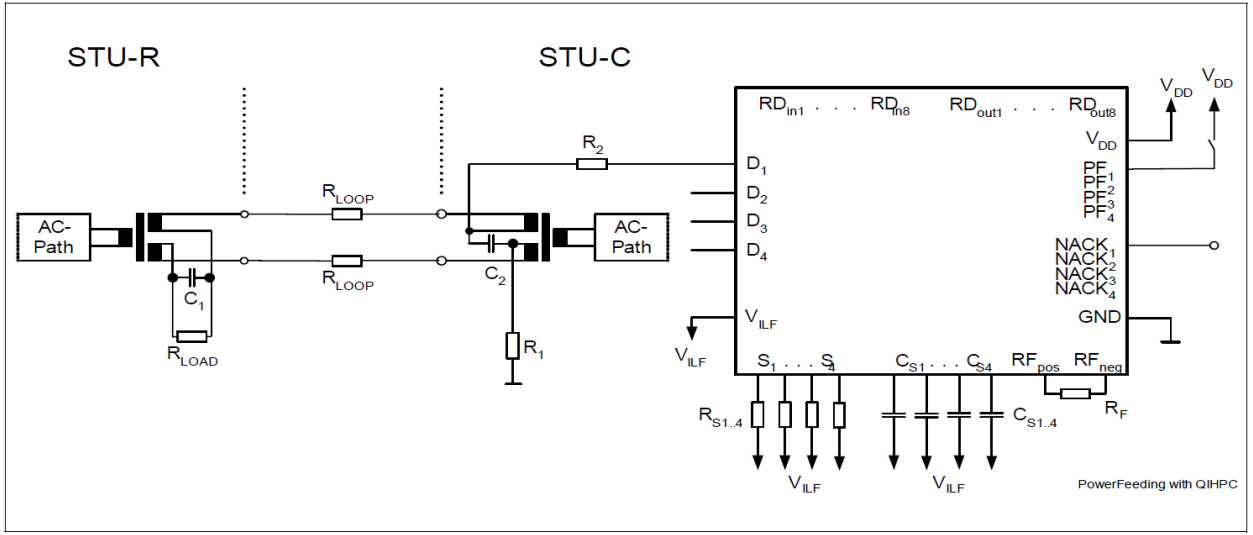
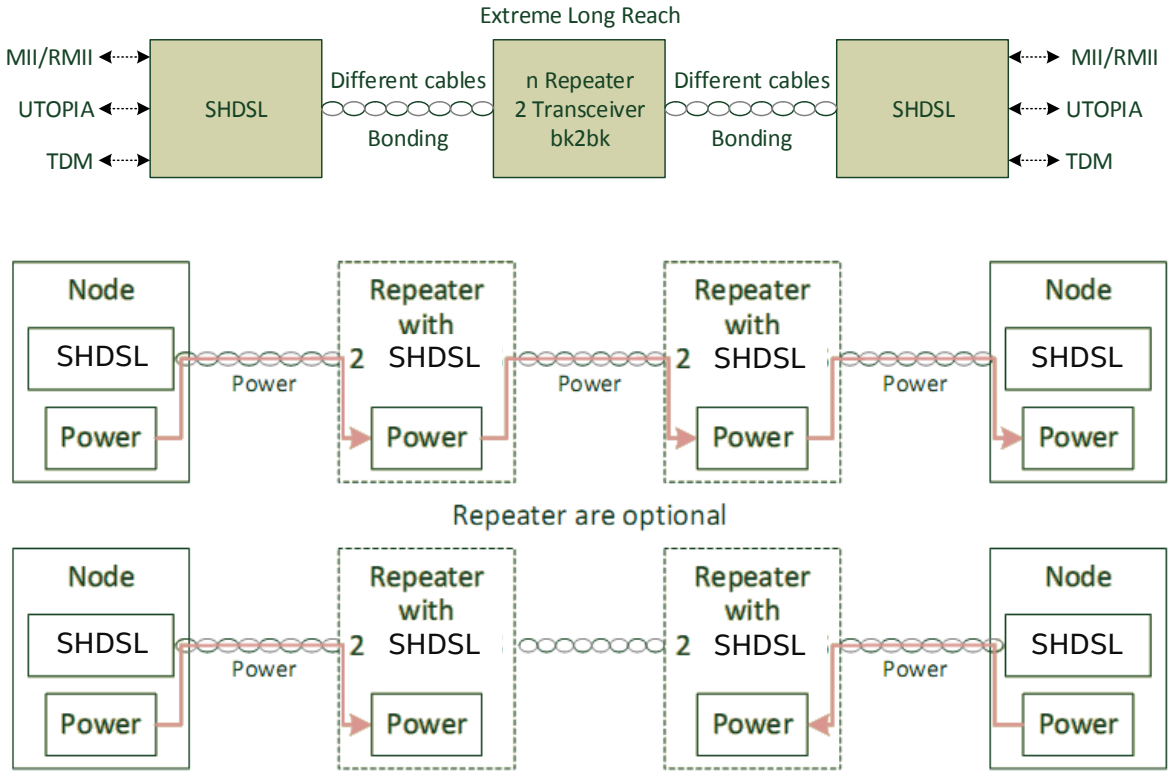
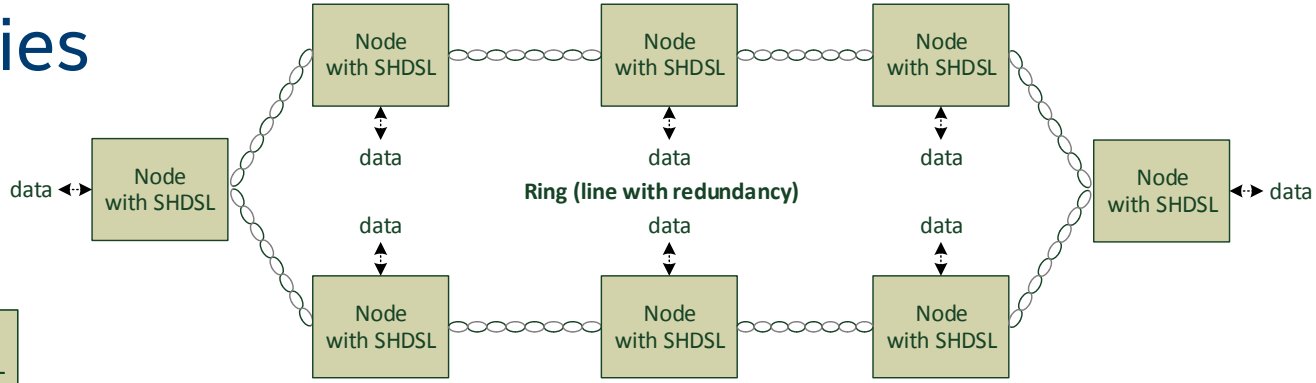


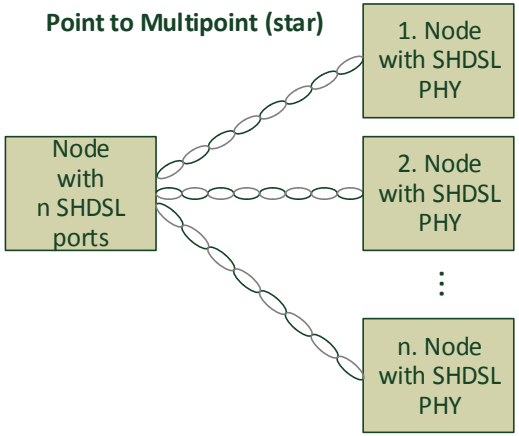
Figure 3 Power Feeding

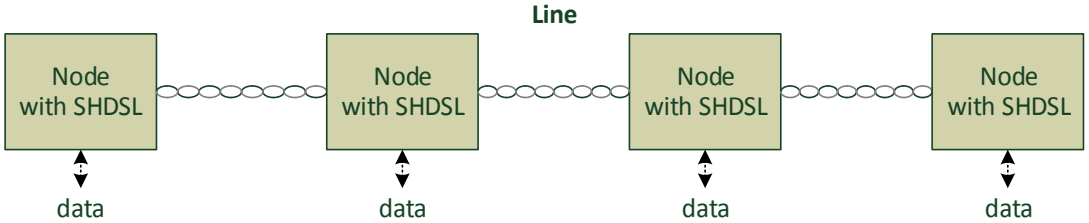
Multi-Hop “Daisy-Chain” with various RPF schemes



Loop Topologies







S(H)DSL Applications

Broadband services in new locations

Phone-booth WiFi Hot-Spot


Hotel and internet café

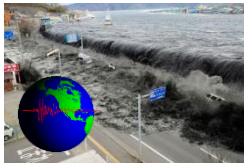
Emerging market business access


Small cells


Campus network

Energy – Military - Disaster


Oil platforms


Disaster pre-warning and seismology


Mining comms networks


Military and rescue equipment


Fire control networks

Infotainment, surveillance, ticketing and SOS


Infotainment


Surveillance camera

Public emergency SOS systems


Ticketing

Info and advisement screens

DISCUSSION

Further exploration (1)

Link Activation

- Currently Link-Activation is about 30sec including G.hs.
- With increased baud rates and reduced loop-length (1km only) the training times can be significantly reduced (at least 10x shorter, i.e. ~1sec)

Autonegotiation

- G.handshake (G.994.1) is essentially the same principle as Autoneg. For 1km of loop length it shall be verified what (trainingless) modulation scheme would serve the purpose to exchange capabilities and resolve onto a common mode.

Line-Probing

- Line-Probing can be omitted since the data-rate is fixed.

Further exploration (2)

Transformer

- Currently the XFRM (EP7 footprint) is defined by the low data-rates.
- Increasing and fixing baud-rates simplifies XFRM design and reduce cost

Line-Code (PAM modulation depth)

- Depending on noise-model, disturbance impairments and cable insertion loss the modulation scheme must be defined. Less PAM levels simplify EMI ingress disturbance handling but lift up the baud rate

Error Coding

- Currently only an inner code is defined. Parallel Bits are unprotected. Consider and outer code. Potentially Re-Tx.

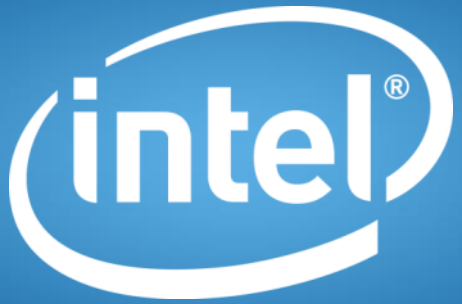
Further exploration (3)

Fast Retrain (EEE)

- A time budget of 100ms should be feasible considering that for 1000baseT the retrain is defined to be 200us at 125Mbaud vs. 100ms at 2.5MBaud. This looks yields a 10x margin considering filter lengths and convergence being similar (which it practically is in the same order of magnitude)
- The basic refresh technology could be comparable to 1000baseT-EEE for a feasibility assessment.

Transmit Signal

- In a self-NEXT limited system the transmit power does not play a major role. It's more about the alien NEXT disturbance. A reduction by 10x seems feasible considering no competing traditional telco-disturbers are in the same bundle.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