10 Mb/s Single Twisted Pair Ethernet
Implementation Thoughts – Proof of Concept

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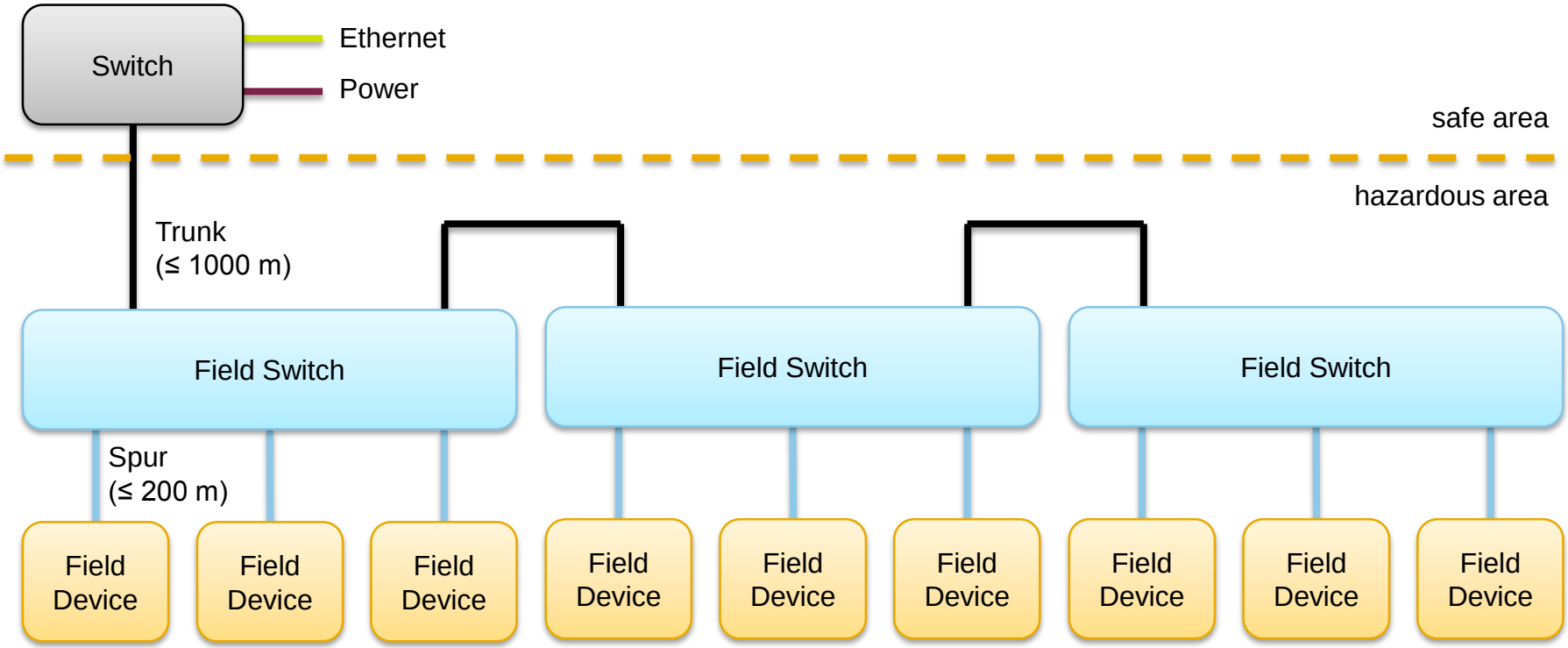
Overview

- Signal Coding
- Analog Frontend
- Receiver
- Spaced Echo Canceller
- Actual Status
- Work in Progress

Signal Coding I

- The required cable length is up to 1000 m for a trunk and up to 200 m for a spur.



- Suggested is a 4B3T line coding (7.5 MSymbols/s) with levels of +1 V, 0 V, -1 V into 100 ohms (for the trunk) and levels of +0.5 V, 0 V -0.5 V into 100 ohms (for intrinsically safe spurs). The reduction of the signal amplitude on the spur side allows to provide a higher energy to the intrinsically safe field devices.

Signal Coding II

- The 4B3T line code converts 4 data bit (16 values) into 3 triplets (27 values). The additional values can be used to code the data stream in a way so that a DC free and practically baseline wander free communication signal results.

Bit pattern	Disparity = -2	Disparity = 0 or -1	Disparity = 0 or +1	Disparity = +2
0000	+0+ (+2)	0-0 (-1)		
0001		0-+ (+0)		
0010		+-0 (+0)		
0011		00+ (+1)		--0 (-2)
0100		-+0 (+0)		
0101	0++ (+2)	-00 (-1)		
0110		-++ (+1)	--+ (-1)	
0111		-0+ (+0)		
1000		+00 (+1)		0-- (-2)
1001		+-+ (+1)		--- (-3)
1010		++- (+1)	+-- (-1)	
1011		+0- (+0)		
1100	+++ (+3)	-+- (-1)		
1101		0+0 (+1)		-0- (-2)
1110		0+- (+0)		
1111	++0 (+2)	00- (-1)		

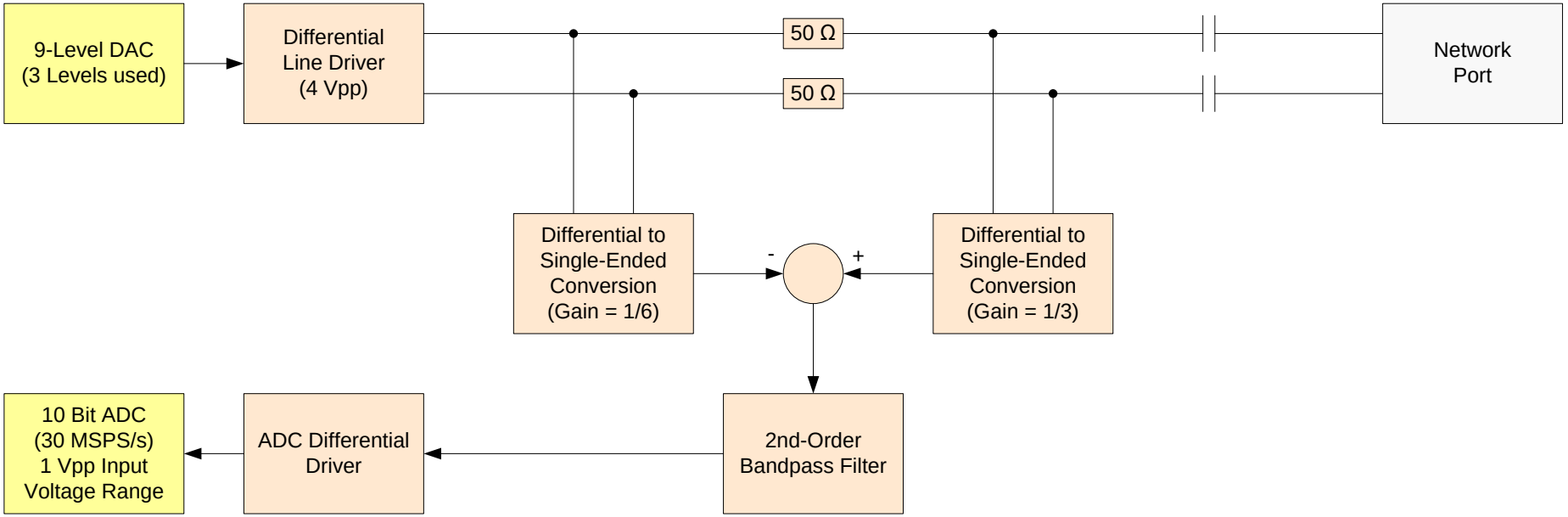
Signal Coding III

- Taking the limited overall signal amplitude into account, this results in a two times higher possible modulation amplitude (6 dB) compared to a signal with high baseline wander.
- The preamble and start of frame of the Ethernet packet are in the current implementation replaced by two different gold sequences of the same length (one for each PHY on the link), no other changes are applied to the Ethernet packet.
- The gold sequences are chosen, so that they are practically DC free, have statistical signal behavior similar to the normal communication signal, show good correlation properties to itself and have a low cross-correlation level between each other.
- Due to power constraints and implementation effort in a low-power FPGA solution, the training of the digital filters is offloaded into software.
- The gold sequences are needed to align the transmitted and the received telegrams for the filter training (mainly because the delay time of the cable is not known and the receive, near end and far end transmit signals must be aligned for the training).
- Using the gold sequences a correlation search for the beginning of the far end data stream within the ADC data stream is possible for the software training algorithm.

Signal Coding IV

- The gold sequence is also being used as a part of the training sequence for the equalizer and echo canceller.
- The transmitter sends at the symbol rate with 7.5 MSymbols/s a ternary signal (PAM-3). The analog circuit reduces the edges slightly to reduce the level of the harmonics.
- The transmitted signal is subtracted in an analog way from the summed receive signal under the assumption that to the network port an ideal 100 ohms cable is connected.
- To improve the pre-echo cancellation within the differential to single ended conversion block for the line driver a RC model of the power injection circuit (which behaves mainly capacitive due to the parasitic capacitances of the suppressor and clamping diodes) can be added. Otherwise the adaptive digital echo canceller has to filter out these side effects.

Analog Frontend



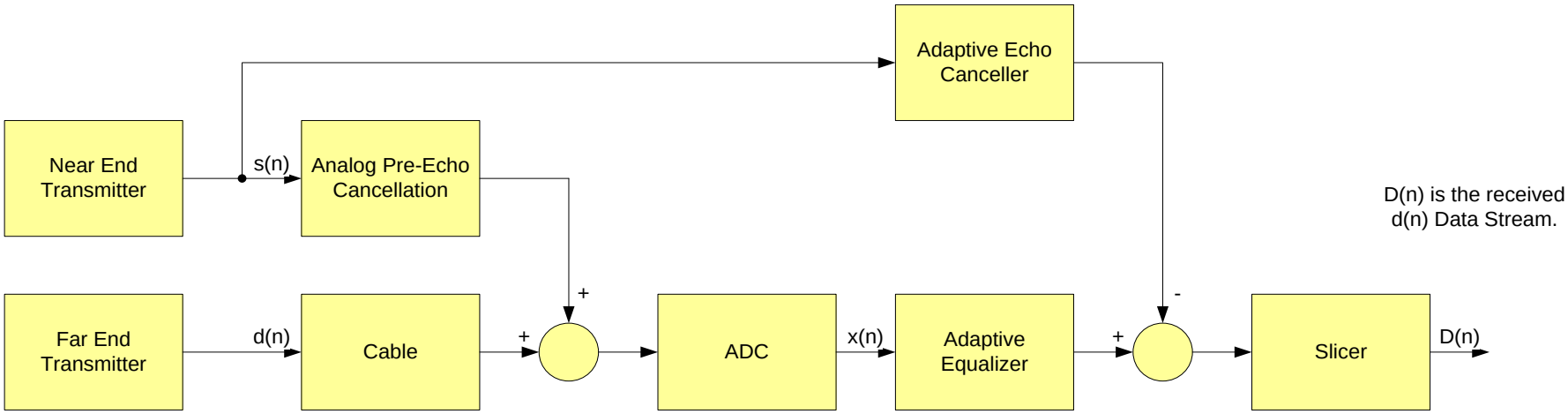
- The power consumption of a discrete implementation of the analog frontend is in the range of about 100 mW (the ADC itself running at 30 MSPS/s needs about 60 mW).
- The expectation is that the power consumption in an ASIC implementation is much less.

Receiver I

- Currently the implementation is done in a low power FPGA.
- The receiver is suggested to use a 4 times oversampling (30 MSPS/s). Currently a 10 Bit ADC is used. Depending on the noise levels which need to be reached, an 8 Bit ADC could also probably be suitable.
- The system training is done using a combined training of the echo canceller and the equalizer (otherwise an online training of the echo canceller during normal operation could be difficult when offloading the training algorithms into software).
- Therefore the standard position of the echo canceller and the equalizer are reversed. The system then is modelled as a system consisting of 2 input parameters (s(n) and x(n) and one output parameter (depending on the view d(n) or D(n)).
- The training algorithm then adopts both filters in parallel. In a running system, all relevant data are also available (instead of (d(n) then the decoded D(n) can be used).

Receiver II

- The implemented equalizer filter length is 8 taps, the implemented echo canceller filter length is also 8 taps (the echo canceller is in the structure behind the equalizer and is therefore influenced by the equalizer).
- When updating the filter coefficients due to the offline filter adoption the current coefficient set has to be faded slowly to a new coefficient set (this is due to a small change in the sampling point position between the two coefficient sets; otherwise this would temporarily lead to a step in the sampling point regulation and therefore to a narrowing of the eye opening).



Spaced Echo Canceller I

- In practical installations different cable types (with different characteristic impedances) are used within the same trunk.
- Therefore cable impedance mismatches occur not only at the PHY side, but also at multiple locations within the trunk, leading to additional return loss.
- The big difference is, that the return loss now is not directly correlated to the transmit signal but is also dependent on the cable length and the positions of the impedance mismatches.
- Assuming e. g. a length of 50 m cable to the position of the first impedance mismatch within the trunk cable, the delay time is about 2 * 50 * 5 ns = 500 ns.
- As mentioned the digital echo cancellation filter has 8 taps running at a sample rate of 30 MHz.
- Therefore the echo cancellation filter has a history of about 7 * 33.3 ns = 233 ns, which is much less than the 500 ns delay time of the cable.
- Therefore the resulting return loss would be treated simply as uncorrelated noise.

Spaced Echo Canceller II

- Taking an attenuation of at least 1.8 dB per 100 m into account (for the higher wire diameters) the first 300 m are the most critical. These 300 m add an additional attenuation to the reflected signal of 1.8 dB/100 m * 300 m * 2 = 10.8 dB, which will convert the worst case return loss of 19 dB to nearly 30 dB providing enough headroom to the 25 dB of insertion loss of the cable (neglecting the transmission factor).
- Assuming that the first 300 m are build consisting of e.g. 3 * 100 m of cable, there will be 2 additional points, where an impedance mismatch could occur and which are in the critical range.
- An echo canceller, which is able to handle the complete length of 300 m of cable would at least need 300 m * 5 ns/m * 2 / 33.3333 ns = 90 taps. Therefore a practical implementation would consist of about 100 taps for the echo canceller, which would exceed the amount of resources in low power FPGAs or significantly increase the cost for an ASIC.

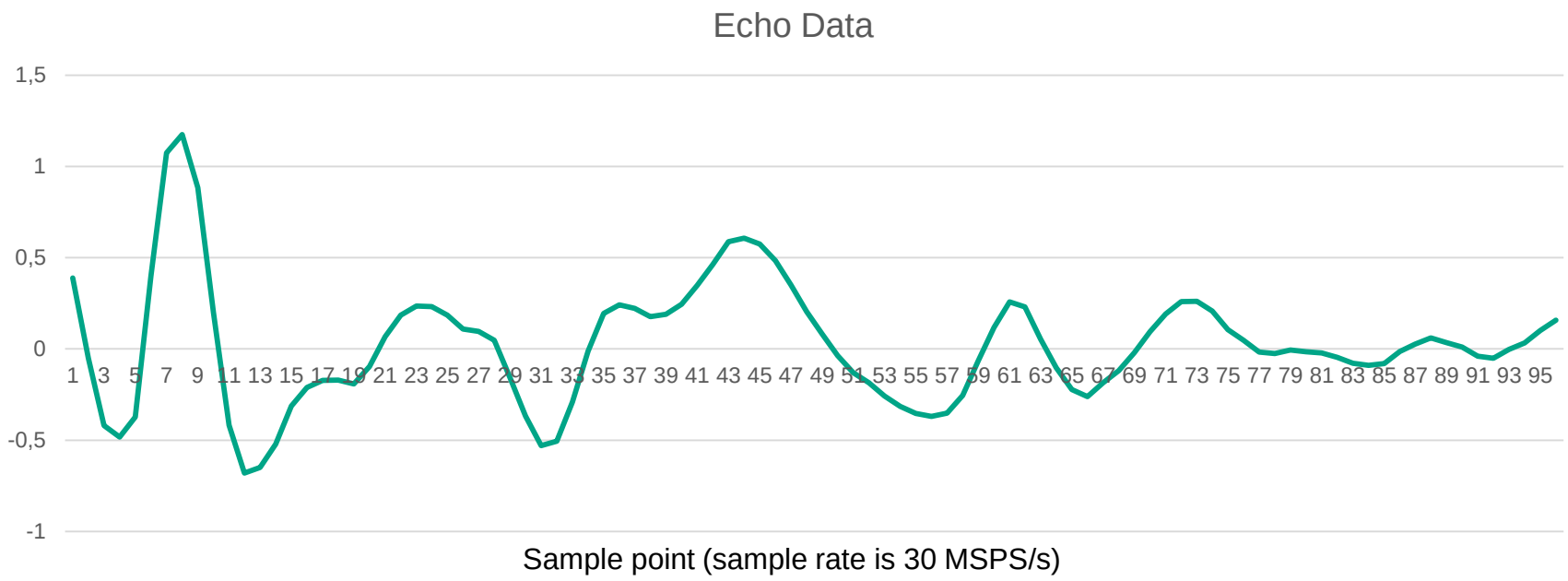
Spaced Echo Canceller III

- Therefore a new implementation idea is to use a “spaced” echo canceller, consisting of several single echo cancellers, with adaptive delay lines (FIFO memory) in between.
- Each echo canceller consists of e.g. 6 taps and can be placed in the signal chain by the adaptive delay lines exactly where the echoes coming from the impedance mismatches occur.
- The more critical impedance mismatches may occur within the first 300 m, the more additional echo cancellers/delay lines need to be implemented.
- During startup procedure the position of the reflections needs to be measured (e.g. by applying a bipolar pulse (+1, -1, 0 symbol transmission). The pulse should be DC free, to prevent side effects by the inductive power decoupling circuit.
- After getting the reflection maxima (absolute values), the echo canceller positions can be calculated.

Spaced Echo Canceller IV

- Example system consisting of:
  1 m AWG18/1 cable - 50 m AWG18/32 (cable 2) - 99 m AWG14/7 (cable 1), 48 m AWG18/32 (cable 2), 1032 m AWG18/1 (cable 6), 2 m AWG18/7

- Summed echo (32 samples):

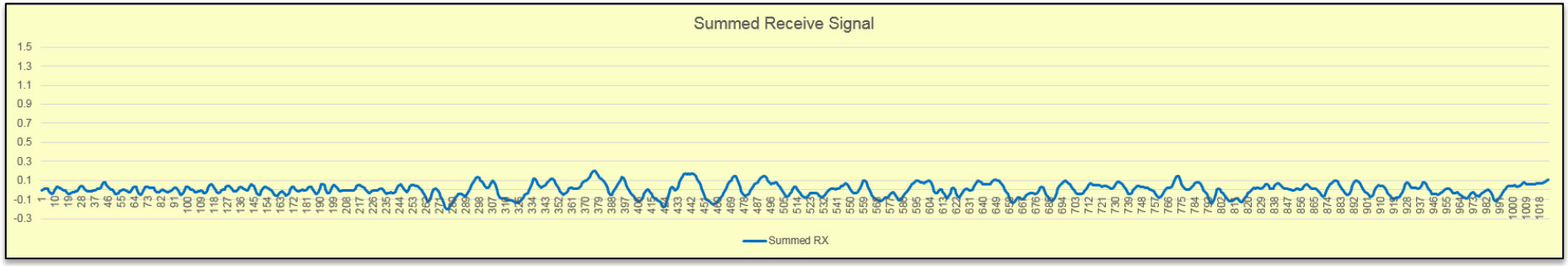


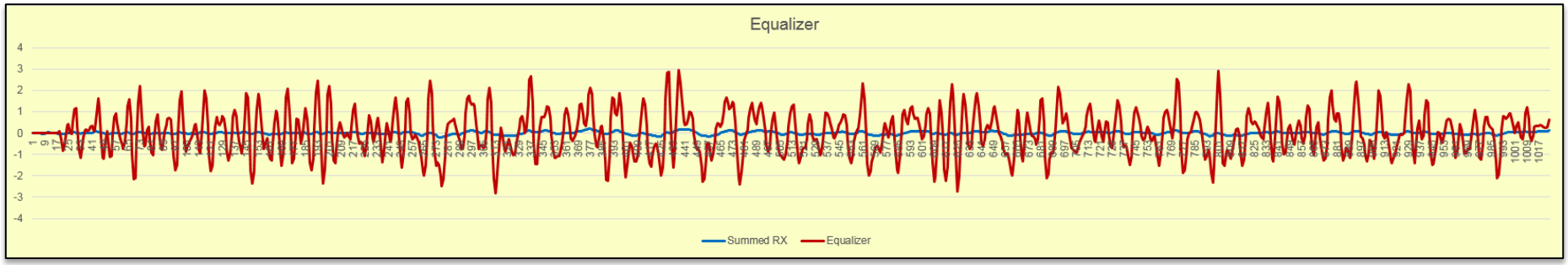
Spaced Echo Canceller V

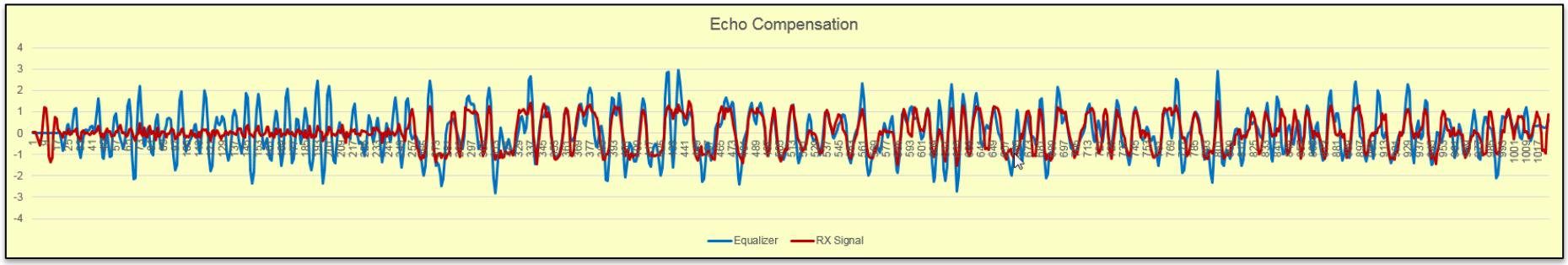
- In the current implementation the first 96 samples (3200 ns) are analyzed. This is equal to about 3200 ns / (2 * 5 ns) = 320 m of cable.
- Within the first 96 samples 8 echo cancellers with 6 taps each can be placed, depending on the worst case reflection positions.
- For the example on the previous slide the echo cancellers are placed at positions 0, 6, 12, 29, 35, 41, 52 and 60, covering most of the echoes.
- The implementation of the spaced echo canceller also significantly drops the computational power needed for the RLS algorithm compared to a full implementation of the echo canceller with 96 taps (60 (12 + 48) taps total filter size compared to 108 (96 + 12) taps total filter size reduces the computational power needed for the filter adoption by a factor of more than 3).

Actual Status I

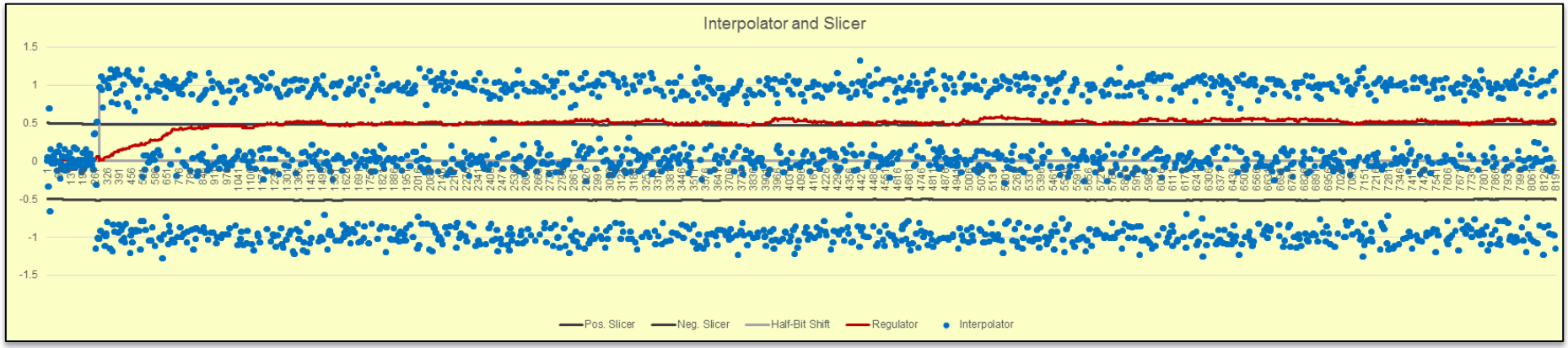
- Transmission over the before mentioned cable (total cable length 1232 m of different cables)

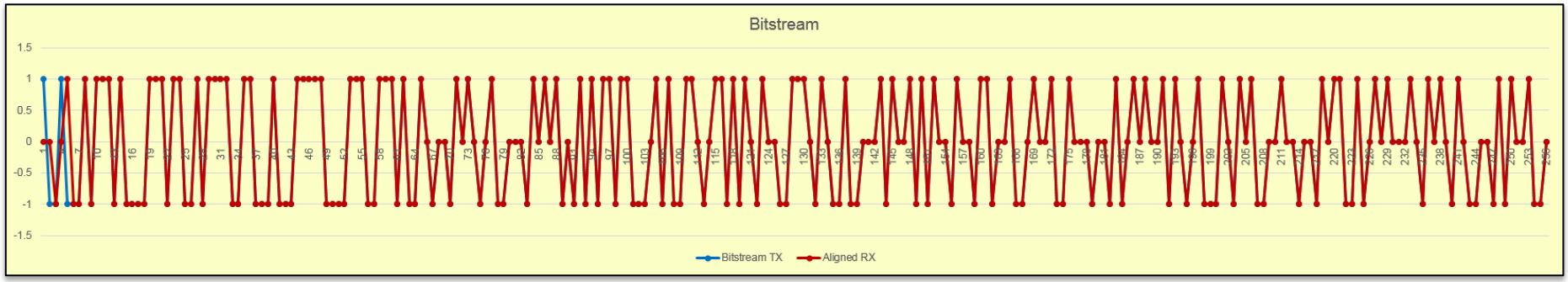






Actual Status II





- The proof of concept is based on two evaluation boards being connected to a PC.
- It could be shown, that a communication over more than 1000 m of cable is working.
- Limits of the technology need to be further analyzed and discussed.

Work in Progress

- Telegram synchronization (IDLE packets, DATA markers etc.)
- Potential use of data scrambling (depending on implementation of independent online training possibility for equalizer and echo canceller)
- Auto negotiation algorithm (master, slave, baud rate 2/10/100 MBit/s)
- Offloading of the training algorithm into software vs. permanent online training.
- VCXO oscillator (master-slave clock implementation).
- Safety margin over temperature.

Thank You