
# Optional Powering based on PoDL for 10SPE

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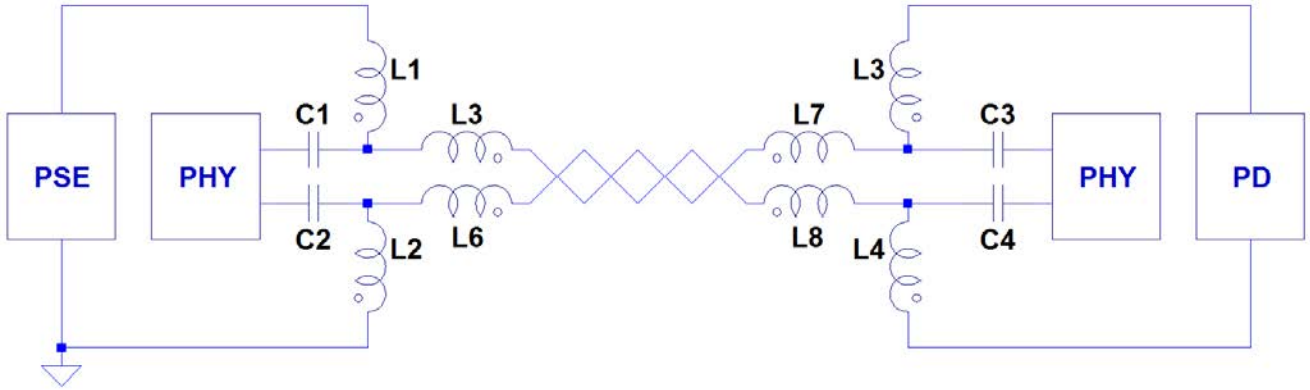
# Presentation Objectives

- Review issues relating to technical and economic feasibility of power delivery for PoDL
- Discuss potential changes to Clause 104 required to support 10PSE

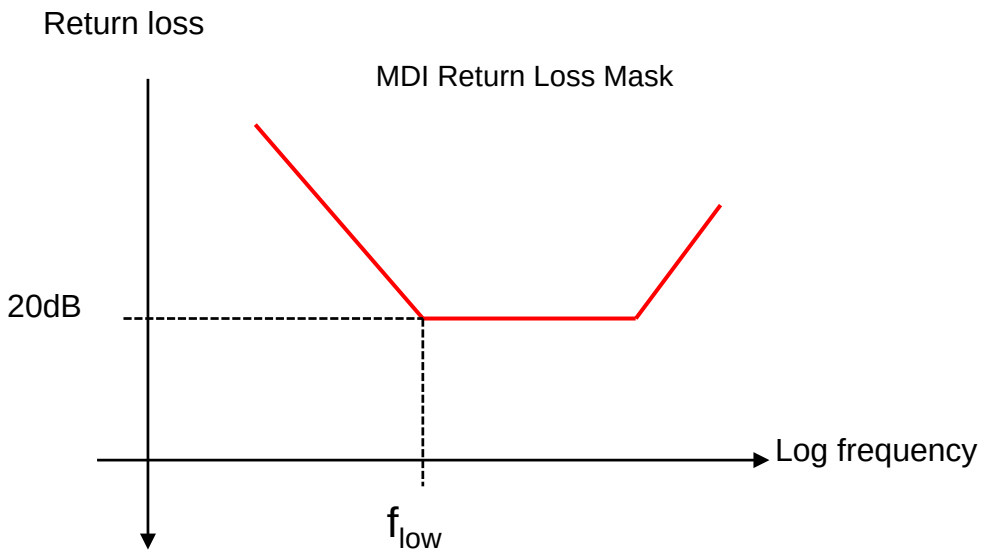
# PoDL Powering Considerations

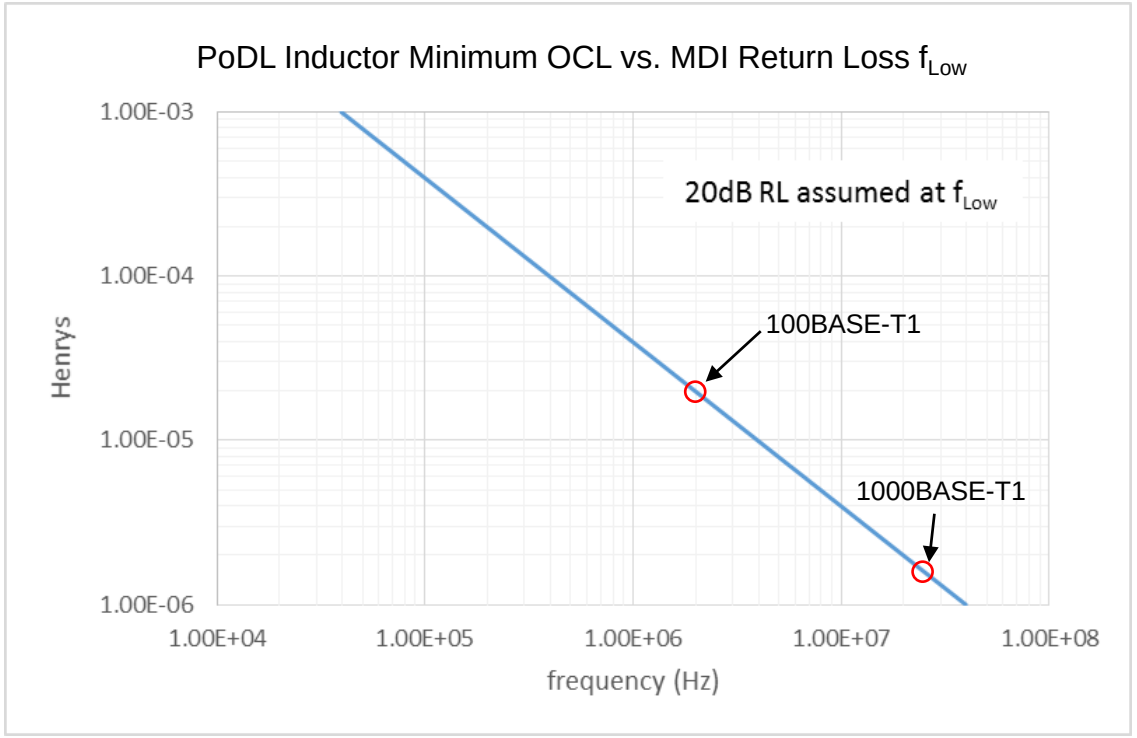
- The PoDL power coupling network must exceed the MDI return loss and mode conversion loss requirements of the PHY with adequate margins for economic feasibility.
- Ripple and transients from PoDL power converters must be filtered before the MDI – lower frequency high-pass poles in the PHYs make this more difficult.
- DCR of MDI magnetics and cable resistance limit the power available for the PD load.
- Saturation current of the MDI magnetics also limits power delivery.




PoDL Circuit Architecture

# Impact of PHY Return Loss on PoDL Coupling Inductors

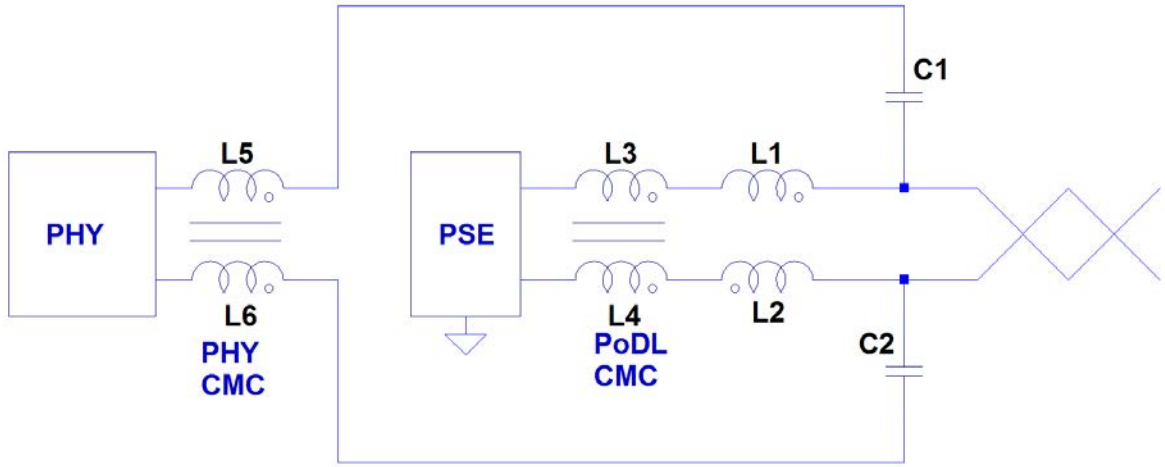



- The open-circuit inductance (OCL) of the PoDL coupling inductors is driven by the PHY MDI low-frequency return loss requirement.
- Higher OCL results in increased DCR, lower saturation current, larger core volume, and lower self-resonant frequency.

# Impact of MDI Mode Conversion Requirements on PoDL

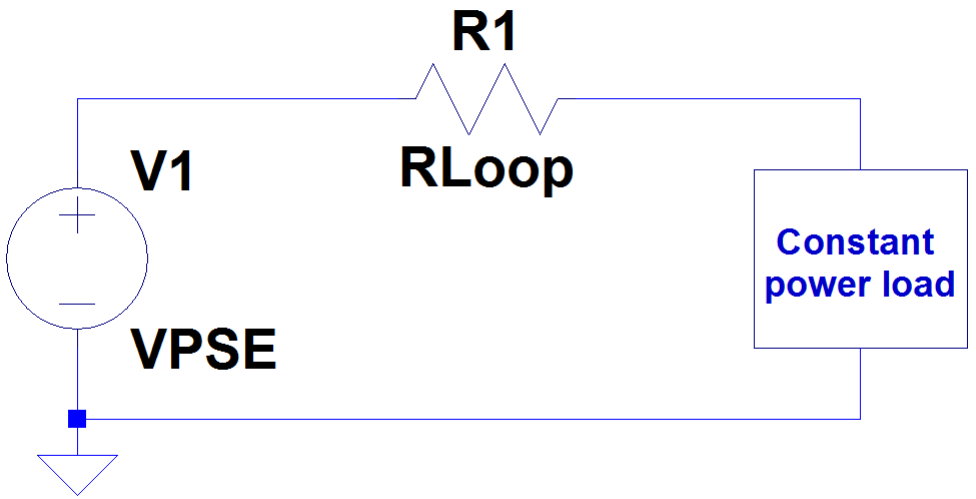
- Mismatch of PoDL coupling inductors causes mode conversion if they are connected directly at the MDI.
- Connecting the PoDL inductors to the MDI through the PHY CMC solves this problem, but the CMC's ampacity and DCR may be an issue for power delivery.
- The alternative circuit configuration shown to the right may be used, but PoDL implementers will need to engineer a power coupling network that exceeds the MDI mode conversion requirement with adequate margin.




Alternative PoDL Circuit Architecture

# PoDL Power Delivery Model

- DC model for analyzing power delivery through series resistance to a load
- Assumes constant power load (worst case assumption)
- Lumps all sources of resistance between PSE voltage source and the PD into $R_{Loop}$
- Loop power efficiency is defined as ratio of delivered load power to power sourced by $V_{PSE}$

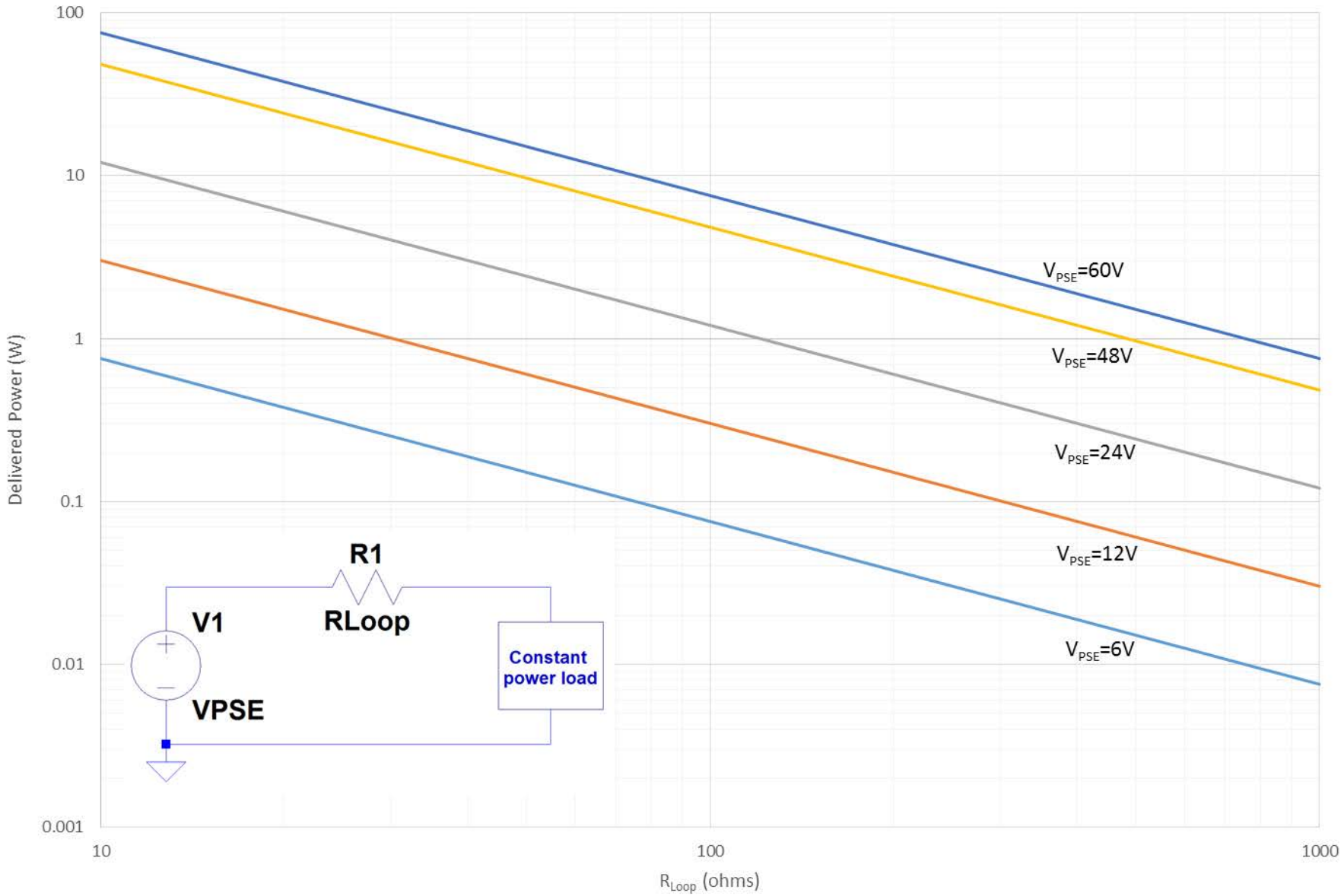



Loop power efficiency = $P_{Load}/P_{VPSE}$

# Power Delivery Efficiency vs. Loop Resistance

- Maximum power transfer occurs when the loop power efficiency is 50%, but…
- Operation at 50% loop power efficiency results in the collapse of the PD input voltage for a constant power load
- Efficiencies above 70% are typically required to ensure robust loop stability
- See darshan_3bu_01_0114.pdf for analytical derivation

# Delivered Power vs. Loop Resistance at 70% Efficiency



# Current Clause 104 Power Class Table

- The current power Class table assumes less than 6.5 ohms of cable resistance
- PSE voltages from 6V to 60V are supported
- Delivered power ranges from 0.5W to 50W depending on PSE output voltage, resistance, and current
- All existing power classes require operation at loop power efficiencies greater than 70%

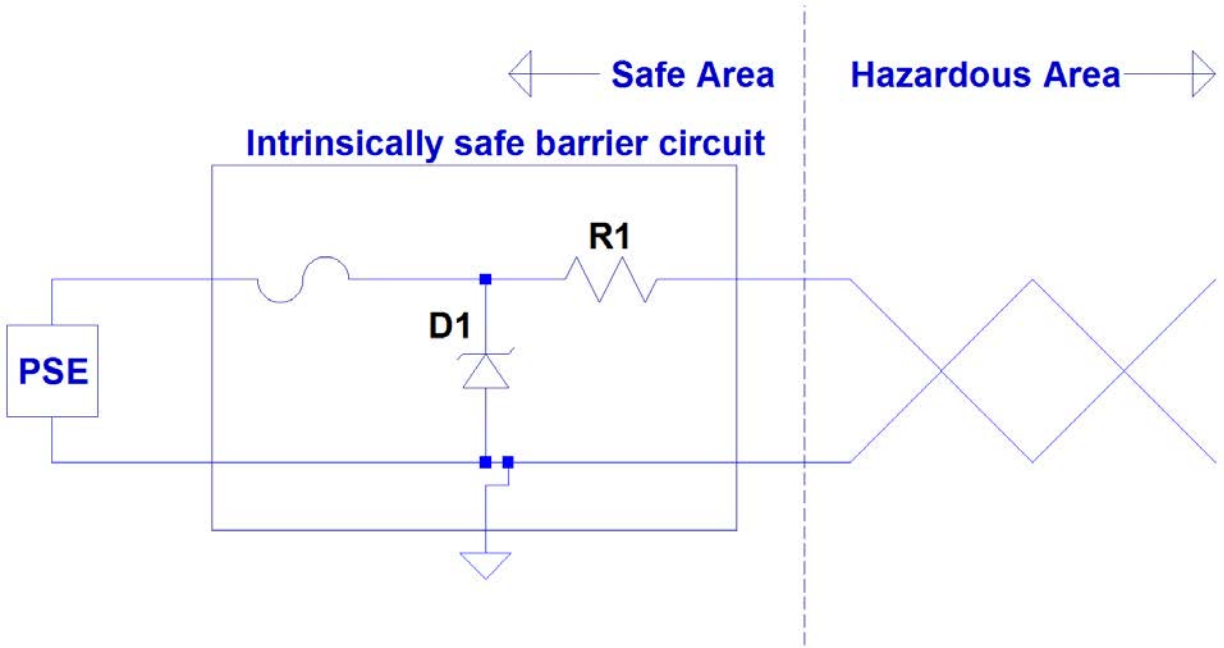
**Table 104–1—Class power requirements matrix for PSE, PI, and PD**

| | 12 V unregulated PSE | | 12 V regulated PSE | | 24 V unregulated PSE | | 24 V regulated PSE | | 48 V regulated PSE | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Class** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| $V_{PSE(max)}$ (V)[a] | 18 | 18 | 18 | 18 | 36 | 36 | 36 | 36 | 60 | 60 |
| $V_{PSE\_OC(min)}$ (V)[b] | 6 | 6 | 14.4 | 14.4 | 12 | 12 | 26 | 26 | 48 | 48 |
| $V_{PSE(min)}$ (V) | 5.6 | 5.77 | 14.4 | 14.4 | 11.7 | 11.7 | 26 | 26 | 48 | 48 |
| $I_{PI(max)}$ (mA)[c] | 101 | 227 | 249 | 471 | 97 | 339 | 215 | 461 | 735 | 1 360 |
| $P_{Class}$ (W) | 0.566 | 1.31 | 3.59 | 6.79 | 11.4 | 3.97 | 5.59 | 12 | 35.3 | 65.3 |
| $V_{PD(min)}$ (V) | 4.94 | 4.41 | 12 | 10.6 | 10.3 | 8.86 | 23.3 | 21.7 | 40.8 | 36.7 |
| $P_{PD}$ (W)[d] | 0.5 | 1 | 3 | 5 | 1 | 3 | 5 | 10 | 30 | 50 |

[a] $V_{PSE}$ is the voltage measured at the PSE PI over the full range of operating conditions.
[b] $V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI.
[c] $I_{PI(max)}$ is the maximum current flowing at the PSE and PD PIs except during inrush or an overload condition. $I_{PI(max)}$ may be exceeded during inrush or an overload (see 104.4.6.2). Users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations (see 104.8.1).
[d] $P_{PD}$ is the maximum average available power at the PD PI.

# Intrinsic Safety and PoDL

- Intrinsic safety barrier circuits prevent external transients from propagating into the hazardous area while also limiting power dissipation if there is a fault in the hazardous area.
  - Example: An IIC explosive gas class safety barrier circuit limits power dissipation to less than 1.3W during a fault condition using a simple series resistor
- PoDL will need to address detection, classification, and power delivery through the resistance of safety barrier circuits.



# Summary of Potential Changes to Clause 104 for 10SPE

- Detection
  - Fast detection (<3ms) is supported by Clause 104 and is intended for engineered system applications with cable resistance less than 6.5 ohms
  - Support for substantially higher cable resistance and intrinsic safety barrier resistors will require a revised detection scheme
- Classification
  - The serial communication classification protocol (SCCP) is used to classify PDs in non-engineered systems
  - PDs that require classification do not present a detection signature
  - Support for higher cable resistance and intrinsic safety barrier resistors will require a revised classification scheme
- PSE and PD Types
  - New PSE and PD Types will need to be added to support signal integrity requirements for 10SPE PHYs
- Power Classes
  - New Classes will need to be added to support power delivery through long reach cables and intrinsic safety barrier resistors

# Questions?

# Thank You!