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Proposal for
Very Short Reach Objective for Scale Up
Introducing 1060nm wavelength as option to meet CSD

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Contribution outline

- Objective and Proposal
- Scale Up Interconnect (Backend XPU and accelerator ASIC)
- Motivation for 1060nm wavelength
- Conclusion

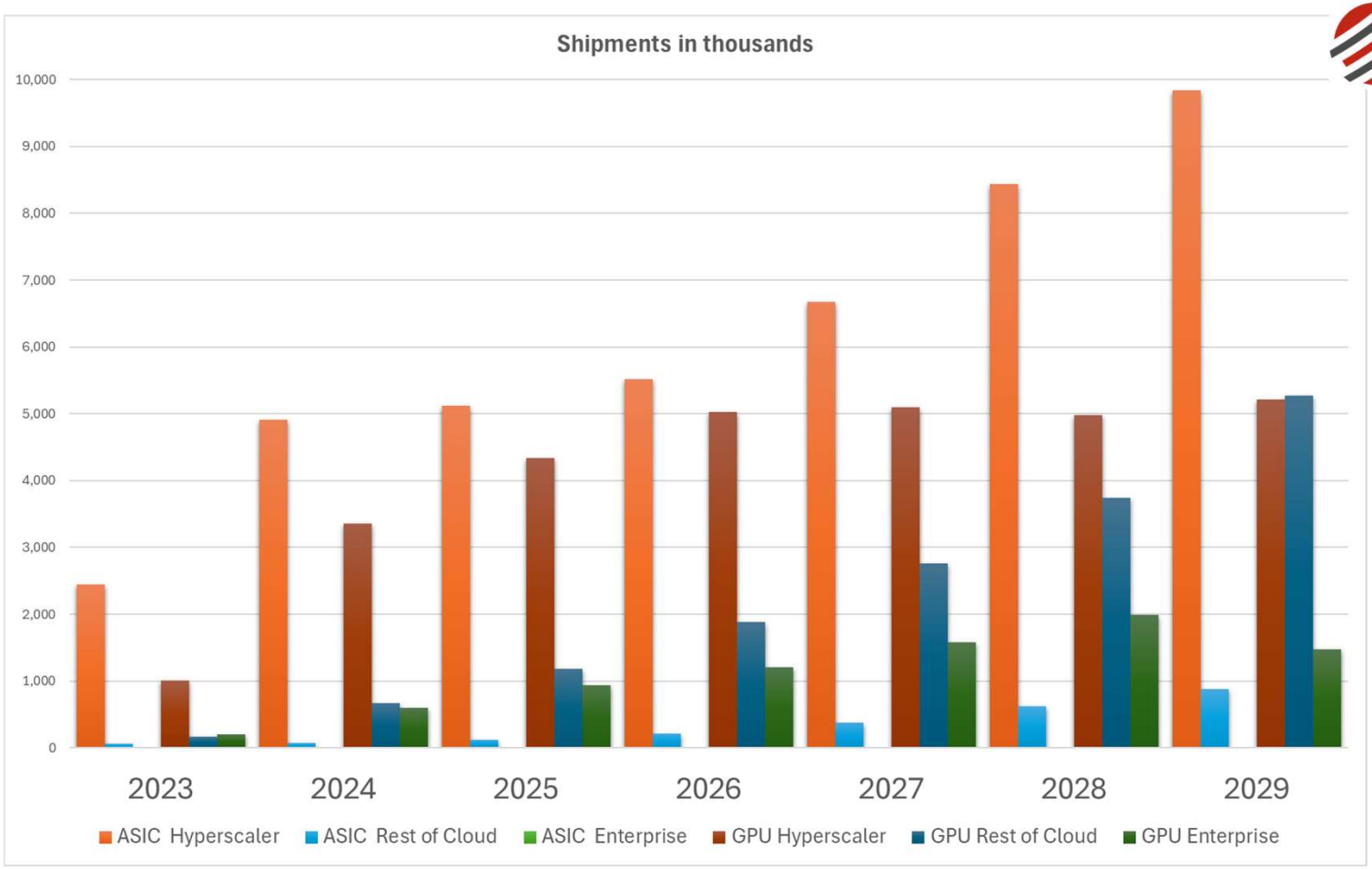
Supporters

- Ali Ghiasi

Objective

- After IEEE 802.3 200G MMF CFI approval, this is a proposal to the Study Group to consider Very Short Reach objective for up to at least 10m targeting the Scale Up interconnect application (AI/ML GPU and accelerator ASICs)
  - During the preparations of the CFI, concept of VCSEL/PD arrays using longer wavelength, i.e. 1060nm and their technical benefits were introduced as option for such objective
  - The present contribution also supports the CSD that will be reviewed by the SG, specifically Broad Market Potential, Technical Feasibility, and Economic Feasibility
- Industry wide initiatives to investigate and define requirements for Scale Up interconnect (OIF, OCP, Ethernet Alliance, HoTI, Hot Chips, etc…).
  - Beyond 2028 need for very high capacity, high reliability and very low power optical interconnect for 500+ GPU/accelerator “row level” clusters
  - The IO capacities for such interconnect will quickly exceed bidirectional 50Tbps per ASIC

Custom ASIC and GPU forecast (Datacenter Only)



650 GROUP
Market Intelligence Research

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- AI ASIC on 2Y refresh cycle with scale up IO capacity doubling from gen to gen

Use cases and connectivity examples

Now

Table 3-1 - Example calculation for a UALink_200 1.0 connected Pod

Parameter	Value	Notes
Accelerator I/O Bandwidth	6.4T	Unidirectional I/O bandwidth for local accelerator connections
Number of Switches	16	Each accelerator connects to all switches in a full mesh
Bandwidth per Link (accelerator BW / number of switches)	400G	Bandwidth per switch coming from an accelerator
Link configuration (link bandwidth / 212.5G per link)	x2	Number of 212.5G lanes comprising the link
Switch I/O Bandwidth	25.6T	Total unidirectional I/O bandwidth supported per switch
Number of Accelerators in the Pod (switch capacity / bandwidth per link)	64	Number of accelerators connected to the switch

Table 3-2 Current generation connectivity example

Configurations for 425G per Link	Lanes per Link				
	x2	x4	x8	x16	x32
ASIC Electrical Interface Type	UALink_200 1.0	UCIe 3.0	UCIe 3.0	UCIe 3.0	UCIe 3.0
Transceiver Location	Pluggable On-Board Co-packaged	Co-packaged	Co-packaged	Co-packaged	Co-packaged
ASIC Electrical Interface Lane Rate [G]	212.5	32	32	32	32
Optical Lane Rate [G]	212.5	106.25	53.125	26.5625	13.28125
Link Options	**Number of Cu Pairs or Fibers/Cores Required (Tx+Rx)**				
Cu pair (KR/CR) or 1λ per fiber (PSM/DR)	4	8	16	32	64
1λ per fiber (BiDir2)	2	4	8	16	32
2λ per fiber (CWDM2)	2	4	8	16	32
2λ per fiber (BiDir4)	1	2	4	8	16
4λ per fiber (CWDM4, WDM4)		2	4	8	16
8λ per fiber (WDM8)			2	4	8
16λ per fiber (WDM16)				2	4

Near Term

Table 3-3 Hypothetical next generation Pod

Parameter	Value	Notes
Accelerator I/O Bandwidth	12.8T	Unidirectional I/O bandwidth for local accelerator connections
Number of Switches	16	Each accelerator connects to all switches in a full mesh
Bandwidth per Link (accelerator BW / number of switches)	800G	Bandwidth per switch coming from an accelerator
Link configuration (link bandwidth / 212.5G per link)	x4	Number of 212.5G lanes comprising the link
Switch Capacity	51.2T	Total unidirectional I/O bandwidth supported by one switch
Number of Accelerators in the Pod (switch capacity / bandwidth per link)	64	Number of 212.5G lanes comprising the link

Table 3-5 - Next generation connectivity example with 425G lanes

Configurations for 850G per Link	Lanes per Link				
	x1	x2	x4	x8	x16
ASIC Electrical Interface Type	UALink @ 400G	UALink_200 1.0	UCIe 3.0	UCIe 3.0	UCIe 3.0
Transceiver Location	Pluggable On-Board Co-packaged	Pluggable On-Board Co-packaged	Co-packaged	Co-packaged	Co-packaged
ASIC Electrical Interface Lane Rate [G]	425	212.5	32	32	32
Optical Lane Rate [G]	425	212.5	106.25	53.125	26.5625
Link Options	**Number of Cu Pairs or Fibers/Cores Required (Tx+Rx)**				
Cu pair (KR/CR) or 1λ per fiber (PSM/DR)	2	4	8	16	32
1λ per fiber (BiDir2)	1	2	4	8	16
2λ per fiber (CWDM2)		2	4	8	16
2λ per fiber (BiDir4)		1	2	4	8
4λ per fiber (CWDM4, WDM4)			2	4	8
8λ per fiber (WDM8)				2	4
16λ per fiber (WDM16)					2

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200G MMF is the PMD of choice for most scale up protocols (Ethernet, UALink and NVLink)

Motivation for 1060nm from VCSEL + PD perspective (I)

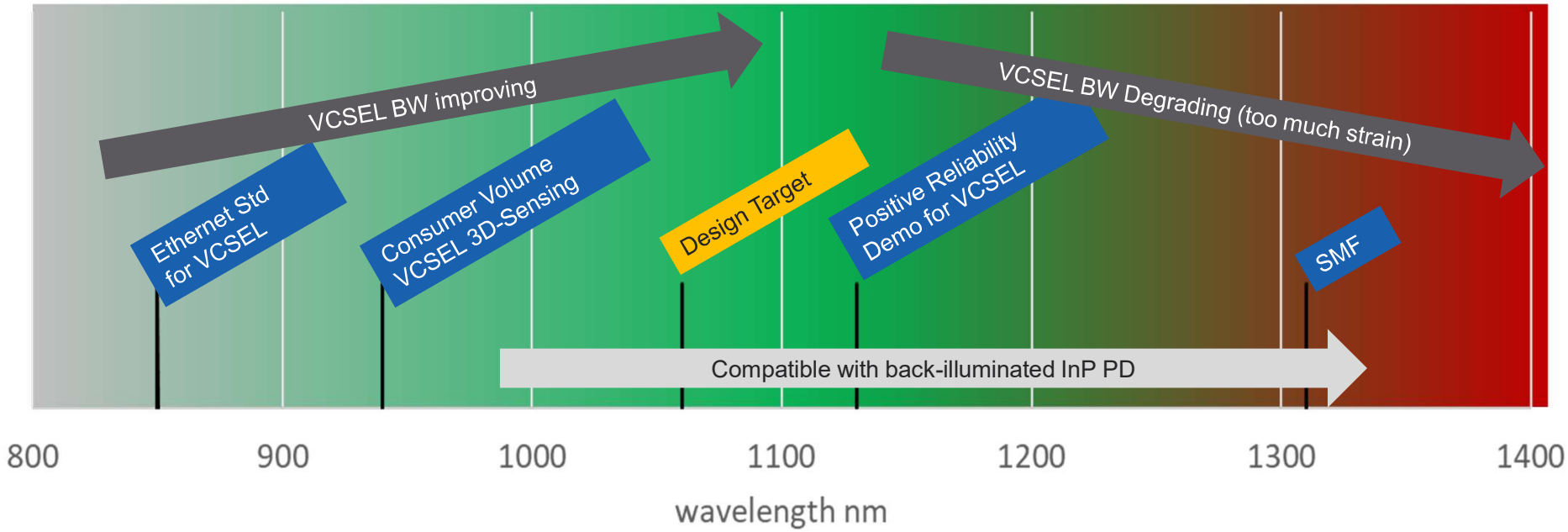
850nm
- First standard, 1999
- Set from fiber / laser technology in 90's.

940nm
- 3D sensing introduced, 2017
- Pushes industry to HVM - billions of emitters shipped

980nm
- Automotive introduced, 2021
- Forces High temperature, high reliability interconnects inside automobiles

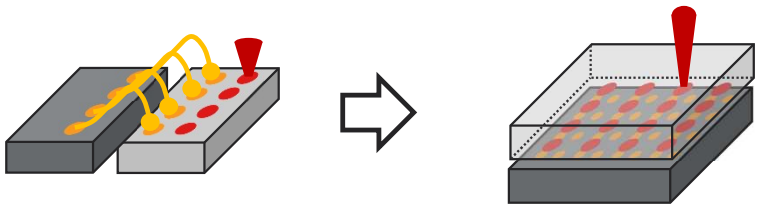
1060nm
- High density interconnect proposed, 2025
- Builds on 3Ds, Automotive, adds bandwidth, density, signal integrity, manufacturability

Motivation for 1060nm from VCSEL + PD perspective (II)



- Higher intrinsic RF bandwidth in 1000-1100nm range - best (operating) power efficiency
- Proven 940nm reliability, 1130nm showing even better reliability performance

1060nm VCSEL technical benefits summary

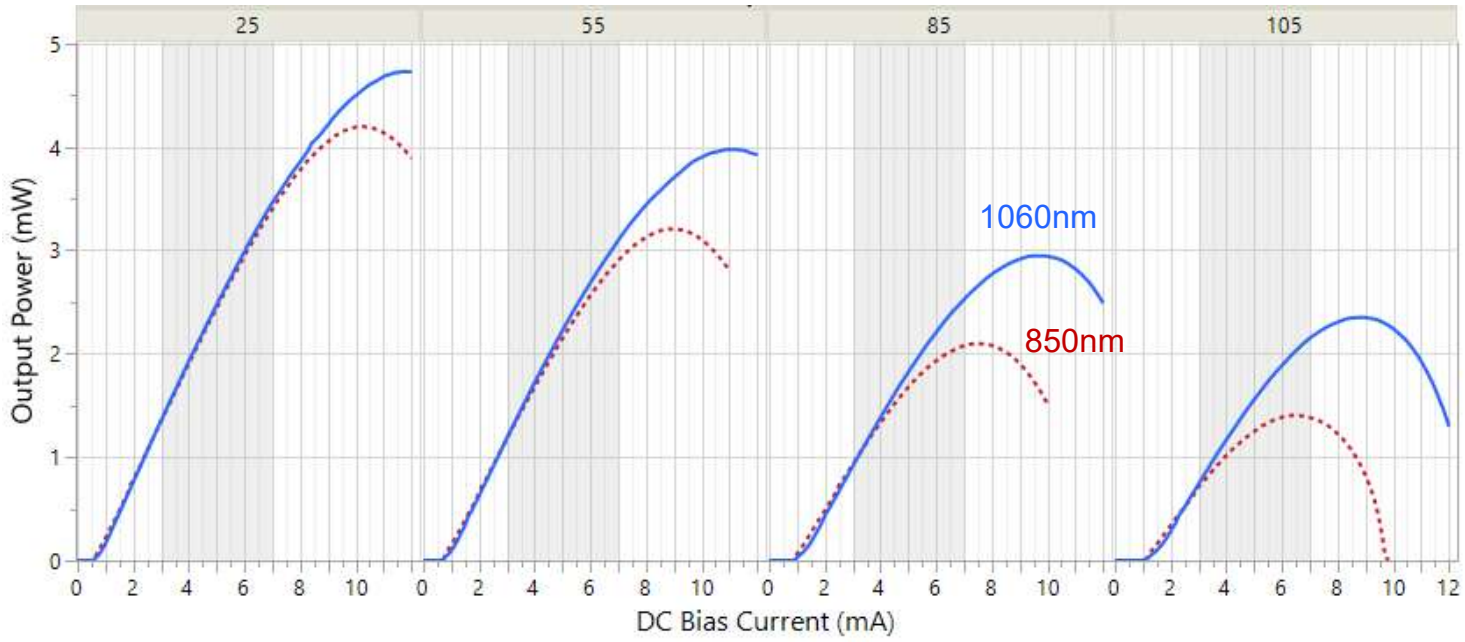


Metric	850nm	1060nm	Context
Fiber BW	+	-	**Help needed from fiber manufacturers** to confirm reach at 1060nm
Wall plug efficiency	+	+	Roughly equivalent efficiency, slightly lower voltage at 1060nm.
Emitter BW	-	+	Strained InGaAs active layer design enables 1.3x intrinsic BW, higher differential gain and efficiency
Signal Integrity	-	+	Flip chip integration removes group delay impedance issues known with wire-bonding..
Reliability	-	+	Flip chip and channel sparing takes FIT below 1. Al free active region enable high temp/high power reliability.
Detector technology	-	+	Flip chip detectors - higher speed / better responsivity than wire-bonded equivalent
Density	-	+	2D VCSEL arrays for high density interconnect including channel sparing
Thermal management	-	+	>20C lower laser junction, >20C lower ASIC temperature from flip chip driver/TIA assemblies
Manufacturability	-	+	Flip chip for mass reflow or TCB, also enables high accuracy placement for assembly
Volume	-	+	Builds on largest VCSEL deployments in history, reuses MFG partners, test, assembly supply chain

1060nm VCSEL | Example L-I Curves over Temperature (I)

Example DC L-I Curves for Top-Emitting VCSELs vs. Heat-Sink Temperature

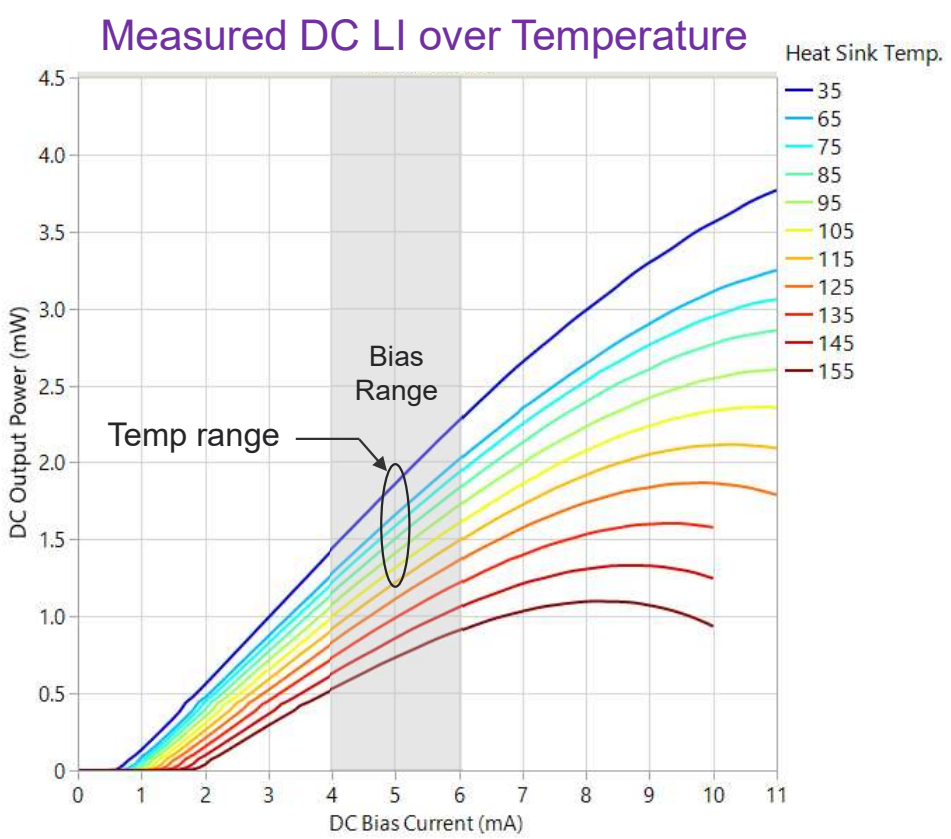
similar ~5um OA and 25ºC slope eff. devices selected

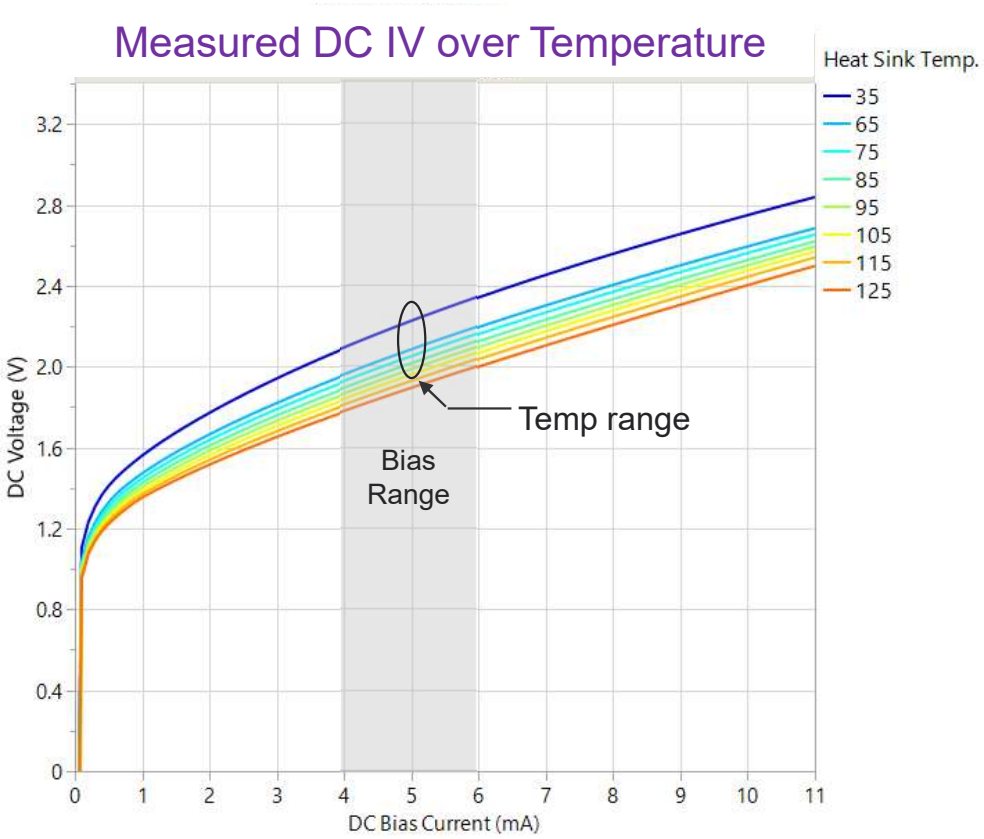


Typical bias range 5±2mA

- 1060nm device with higher strain and deeper wells are more linear at higher current and temperature

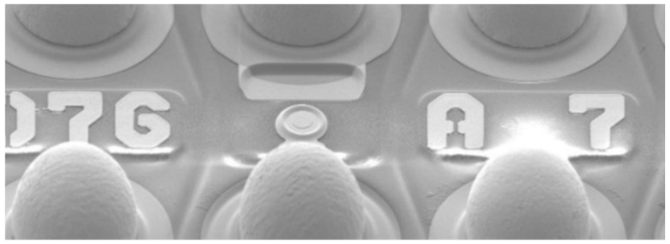
1060nm VCSEL | Example L-I Curves over Temperature (II)



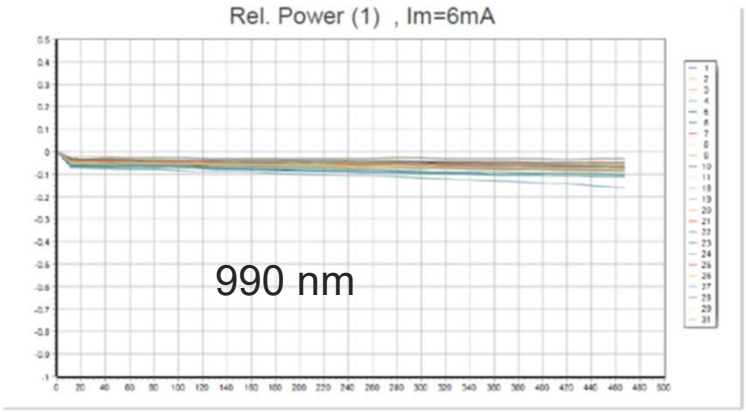


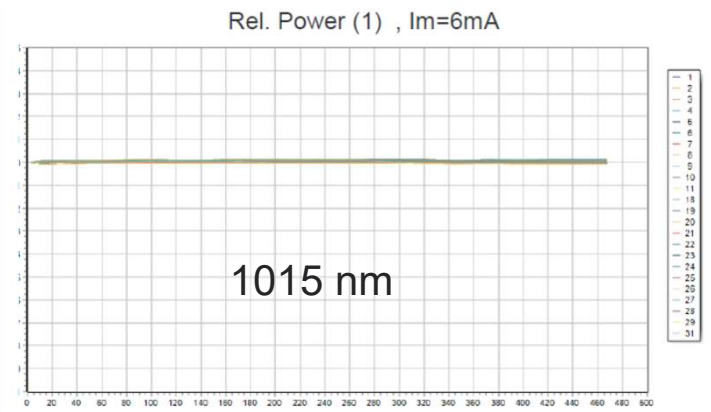
- Excellent performance with >155C operating temperature

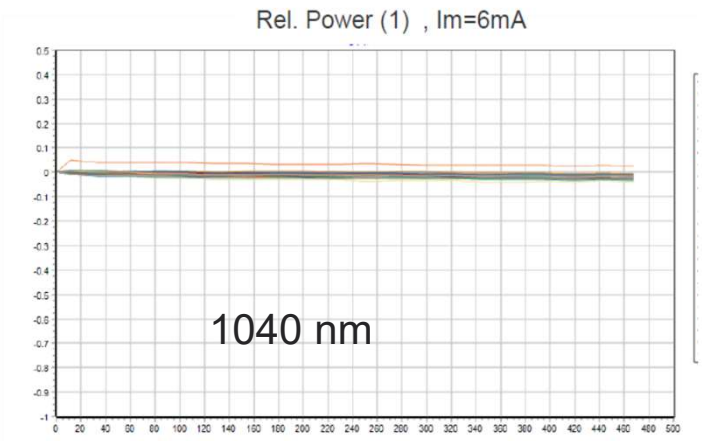
Industry Example – High Reliability to 1065nm and Bottom-Emitting

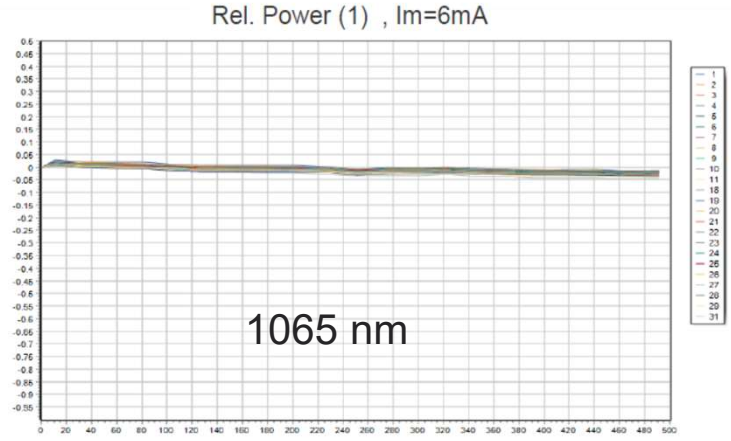


- 170ºC (high acceleration) 8mA stress
- Flip-chip bottom emitting







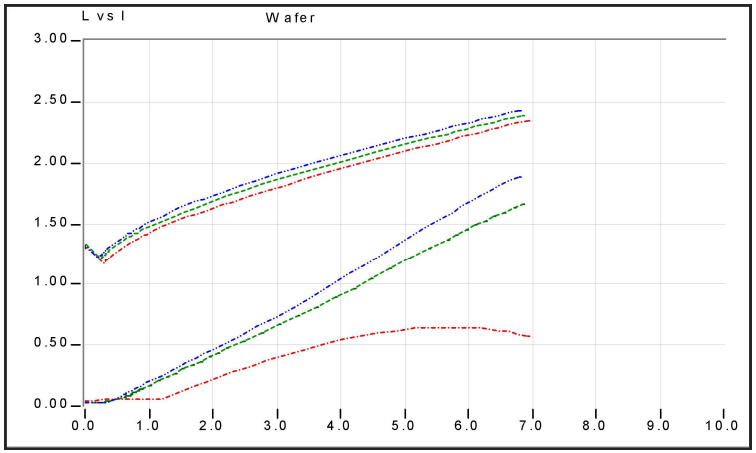


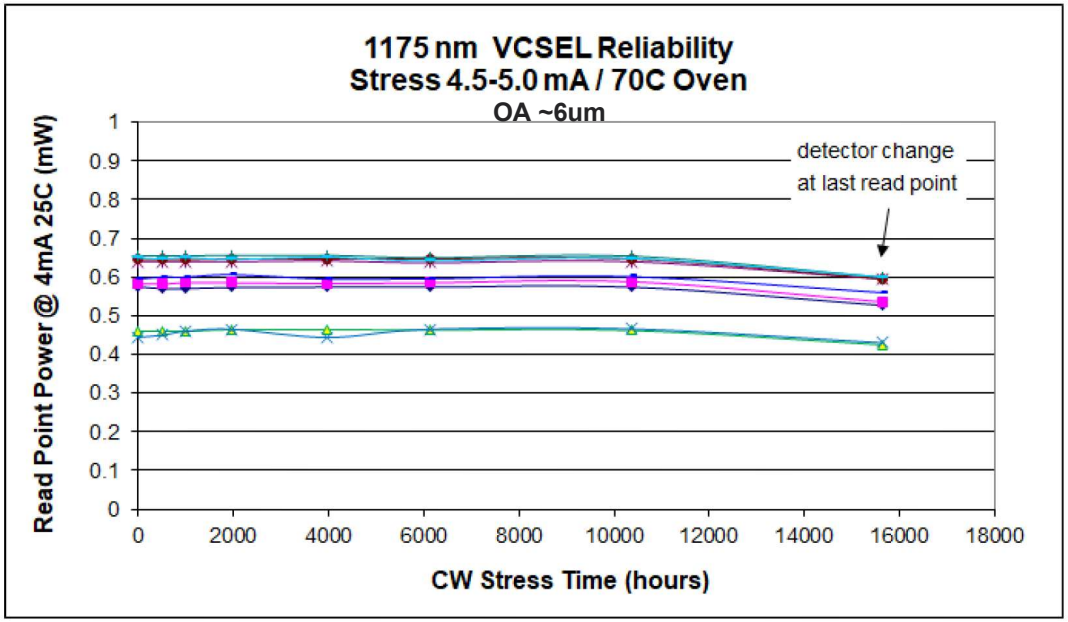
- Samples from 4 different wafers (4 different EPI designs): 0 fails after 500hrs

Example – Demonstrating High Reliability to 1175nm

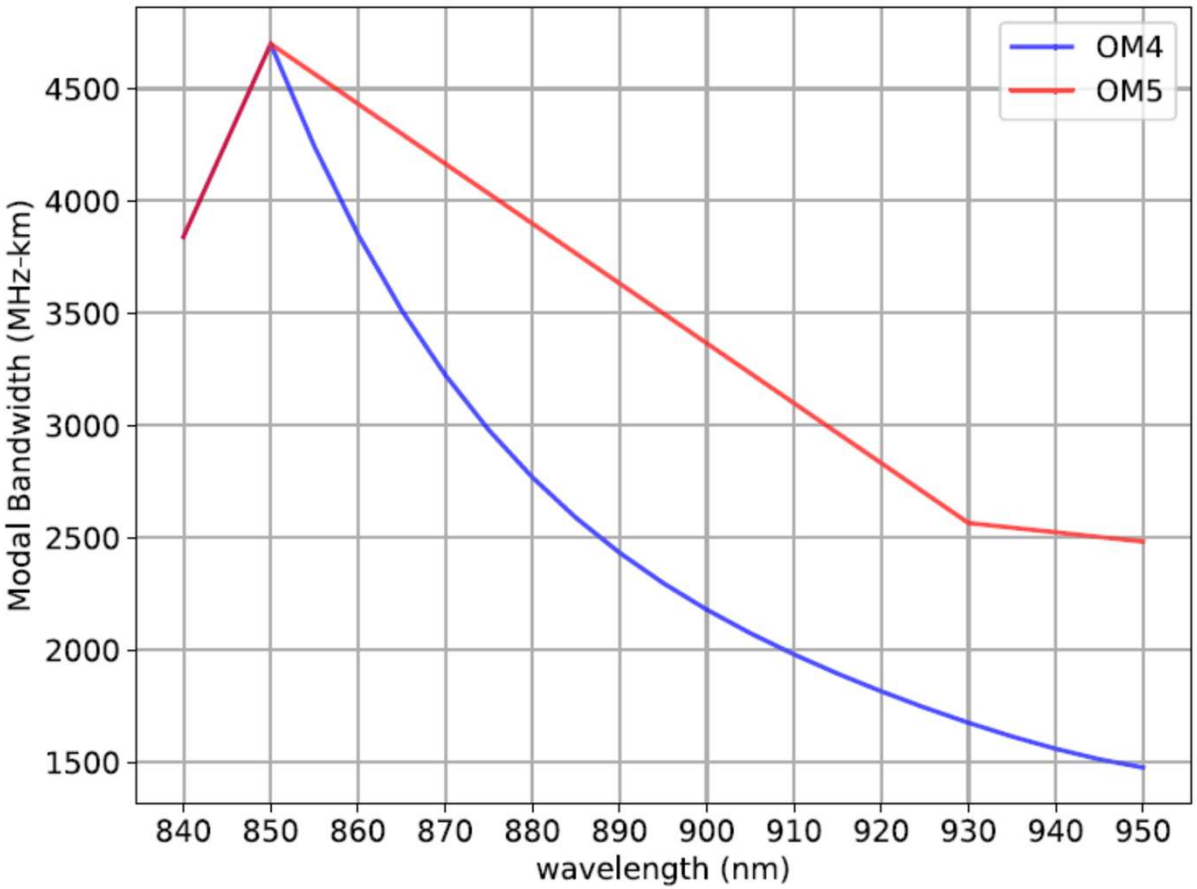
- Early reliability of designs targeting datacom applications
- VCSELs run for ~16k hours with no significant degradation
  - Provided confidence in reliability of Lumentum InGaAs based active region design. Excellent reliability for 1060nm or below was proven

Example 1175nm Datacom CW LIV
Test Temperatures 5, 25 and 70°C





> 950nm VCSEL OM4 and OM5 fiber constraints



- Need to specify OM4/OM5 fiber EMB beyond 950nm vs achievable reach for “–VSR”

Conclusion

- We demonstrated industry need for optical interconnect targeting next gen AI/ML clusters and the opportunity to leverage new technologies including advanced packaging
- Proposing IEEE802.3 200G MMF SG to approve the objective at a minimum reach of 10 m (VSR) and technical benefits of 1060 nm wavelength VCSEL and the ability to enable the proposed VSR objective
  - We also recommend objectives for up to 30 m and up to 50 m reaches. We believe these longer-reach objectives will be best met with 850 nm wavelength VCSELs
- The proposal assumes using broadband PDs designed to support 850 to 1100nm wavelengths
- Calling for assistance from fiber manufacturers to provide EMB guidance on existing OM4/OM5 fibers at 1060nm wavelengths
- Adding such objective with set IEEE802.3 for next gen AI interconnect needs. The project should not be restricted ‘transceiver focused’ 850nm

Proposed Objectives (using IEEE802.3db and .df objectives as a template)

- Define a physical layer specification that supports 200 Gb/s operation over 1 pair of MMF with lengths up to at least 10 m
- Define a physical layer specification that supports 400 Gb/s operation over 2 pairs of MMF with lengths up to at least 10 m
- Define a physical layer specification that supports 800 Gb/s operation over 4 pairs of MMF with lengths up to at least 10 m
- Define a physical layer specification that supports 1.6 Tb/s operation over 8 pairs of MMF with lengths up to at least 10 m

Thank you