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Proposal for 200Gbps 30m and 50m MM Reach objectives using 1060nm.

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September 17th, 2025
IEEE 802.3 200 Gb/s per Wavelength MMF PHYs Study Group Interim Meeting

Contribution outline

- Revised Objective and Proposal
- Scale Up Interconnect (Backend XPU and accelerator ASIC)
- Motivation for 1060nm wavelength
- Conclusion

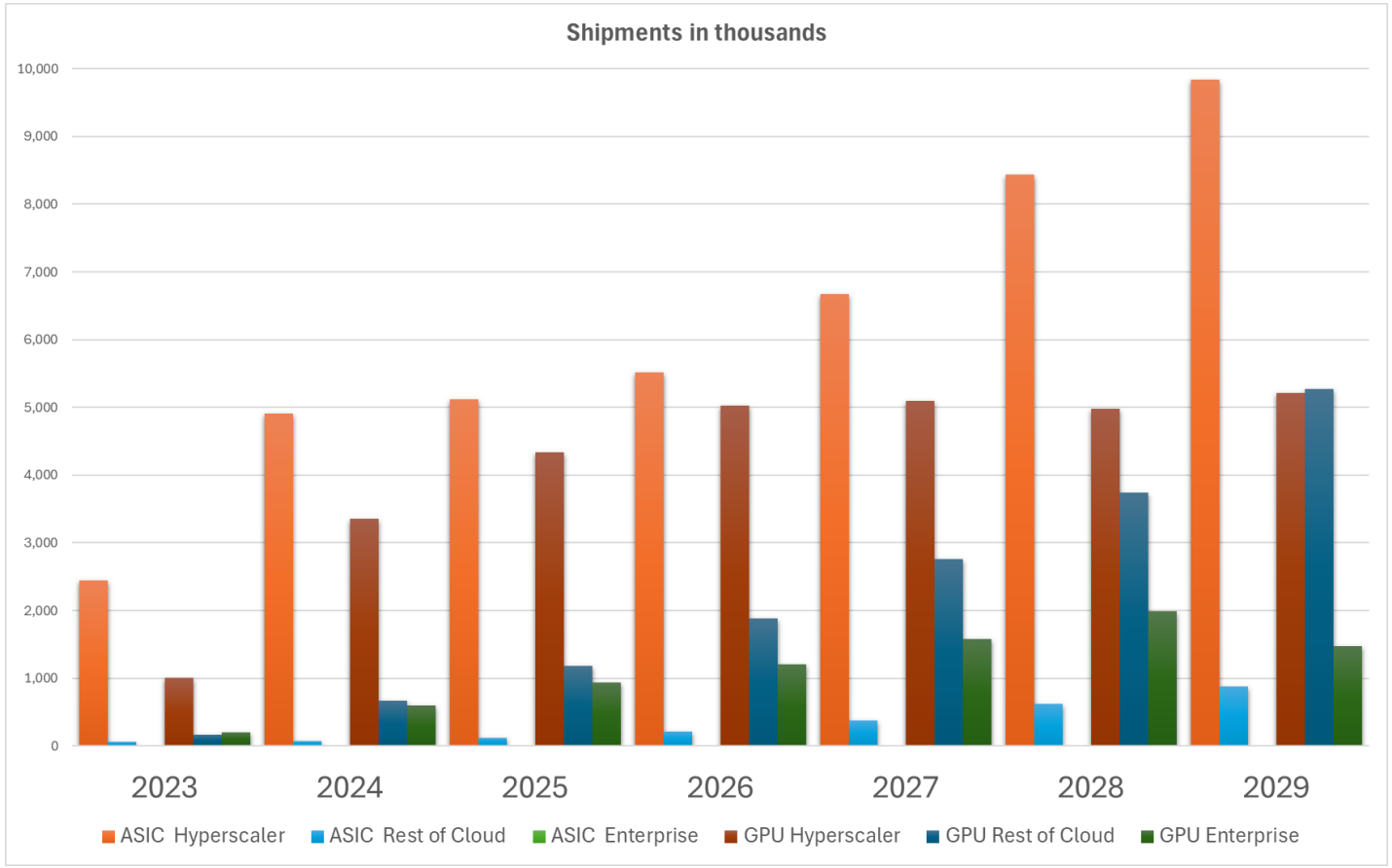
Supporters

- Chris Cole, Coherent
- Ali Ghiasi, Ghiasi Quantum
- Ram Huggahalli, Microsoft
- Fotini Karinou, Microsoft
- Chris Kocot, Coherent
- Daniel Kuchta, Nvidia
- Jeffery Maki, Juniper Networks / HPE
- Roberto Rodes, Coherent
- Ashkan Seyedi, Nvidia
- Hans Spruit, TRUMPF Photonic Components B.V.
- Craig Thompson, Nvidia

Objective

- This is a revised proposal for 30m and 50m reach objectives for high density AI networks.
  - During CFI preparations, we proposed longer wavelength VCSEL/PD as an option 200G MM reach objective. This proposal updates the reach to cover 30 and 50m.
  - Our intent is to meet the Broad Market Potential, Technical Feasibility, and Economic Feasibility CSD objectives.
- The proposal written with the scale up optical interconnect as primary focus, which is mainly a greenfield deployment not bound by backwards compatibility

Custom ASIC and GPU forecast (Datacenter Only)



650 GROUP
Market Intelligence Research

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- AI ASIC on 2Y refresh cycle with scale up IO capacity doubling from gen to gen

Use cases examples

Now

Table 3-1 - Example calculation for a UALink_200 1.0 connected Pod

Parameter	Value	Notes
Accelerator I/O Bandwidth	6.4T	Unidirectional I/O bandwidth for local accelerator connections
Number of Switches	16	Each accelerator connects to all switches in a full mesh
Bandwidth per Link (accelerator BW / number of switches)	400G	Bandwidth per switch coming from an accelerator
Link configuration (link bandwidth / 212.5G per link)	x2	Number of 212.5G lanes comprising the link
Switch I/O Bandwidth	25.6T	Total unidirectional I/O bandwidth supported per switch
Number of Accelerators in the Pod (switch capacity / bandwidth per link)	64	Number of accelerators connected to the switch

Table 3-2 Current generation connectivity example

Configurations for 425G per Link	Lanes per Link				
	x2	x4	x8	x16	x32
ASIC Electrical Interface Type	UALink_200 1.0	UCIe 3.0	UCIe 3.0	UCIe 3.0	UCIe 3.0
Transceiver Location	Pluggable On-Board Co-packaged	Co-packaged	Co-packaged	Co-packaged	Co-packaged
ASIC Electrical Interface Lane Rate [G]	212.5	32	32	32	32
Optical Lane Rate [G]	212.5	106.25	53.125	26.5625	13.28125
Link Options	**Number of Cu Pairs or Fibers/Cores Required (Tx+Rx)**				
Cu pair (KR/CR) or 1λ per fiber (PSM/DR)	4	8	16	32	64
1λ per fiber (BiDir2)	2	4	8	16	32
2λ per fiber (CWDM2)	2	4	8	16	32
2λ per fiber (BiDir4)	1	2	4	8	16
4λ per fiber (CWDM4, WDM4)		2	4	8	16
8λ per fiber (WDM8)			2	4	8
16λ per fiber (WDM16)				2	4

Near Term

Table 3-3 Hypothetical next generation Pod

Parameter	Value	Notes
Accelerator I/O Bandwidth	12.8T	Unidirectional I/O bandwidth for local accelerator connections
Number of Switches	16	Each accelerator connects to all switches in a full mesh
Bandwidth per Link (accelerator BW / number of switches)	800G	Bandwidth per switch coming from an accelerator
Link configuration (link bandwidth / 212.5G per link)	x4	Number of 212.5G lanes comprising the link
Switch Capacity	51.2T	Total unidirectional I/O bandwidth supported by one switch
Number of Accelerators in the Pod (switch capacity / bandwidth per link)	64	Number of 212.5G lanes comprising the link

Table 3-5 Next generation connectivity example with 425G lanes

Configurations for 850G per Link	Lanes per Link				
	x1	x2	x4	x8	x16
ASIC Electrical Interface Type	UALink @ 400G	UALink_200 1.0	UCIe 3.0	UCIe 3.0	UCIe 3.0
Transceiver Location	Pluggable On-Board Co-packaged	Pluggable On-Board Co-packaged	Co-packaged	Co-packaged	Co-packaged
ASIC Electrical Interface Lane Rate [G]	425	212.5	32	32	32
Optical Lane Rate [G]	850	425	212.5	106.25	53.125
Link Options	**Number of Cu Pairs or Fibers/Cores Required (Tx+Rx)**				
Cu pair (KR/CR) or 1λ per fiber (PSM/DR)	2	4	8	16	32
1λ per fiber (BiDir2)	1	2	4	8	16
2λ per fiber (CWDM2)		2	4	8	16
2λ per fiber (BiDir4)		1	2	4	8
4λ per fiber (CWDM4, WDM4)			2	4	8
8λ per fiber (WDM8)				2	4
16λ per fiber (WDM16)					2

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200G MMF PHY is a candidate for most scale up protocols (Ethernet, UALink and NVLink)

Why 1060nm?

850nm

- First standard, 1999
- Set from fiber / laser technology in 90's.

940nm

- 3D sensing introduced, 2017
- Pushes industry to HVM - billions of emitters shipped

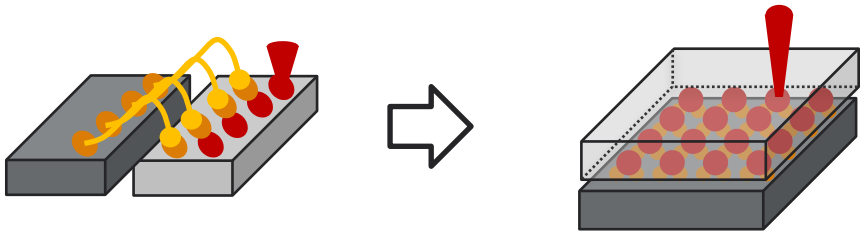
980nm

- Automotive introduced, 2021
- Forces High temperature, high reliability interconnects inside automobiles

1060nm

- High density interconnect proposed, 2025
- Builds on 3Ds, Automotive, adds bandwidth, density, signal integrity, manufacturability

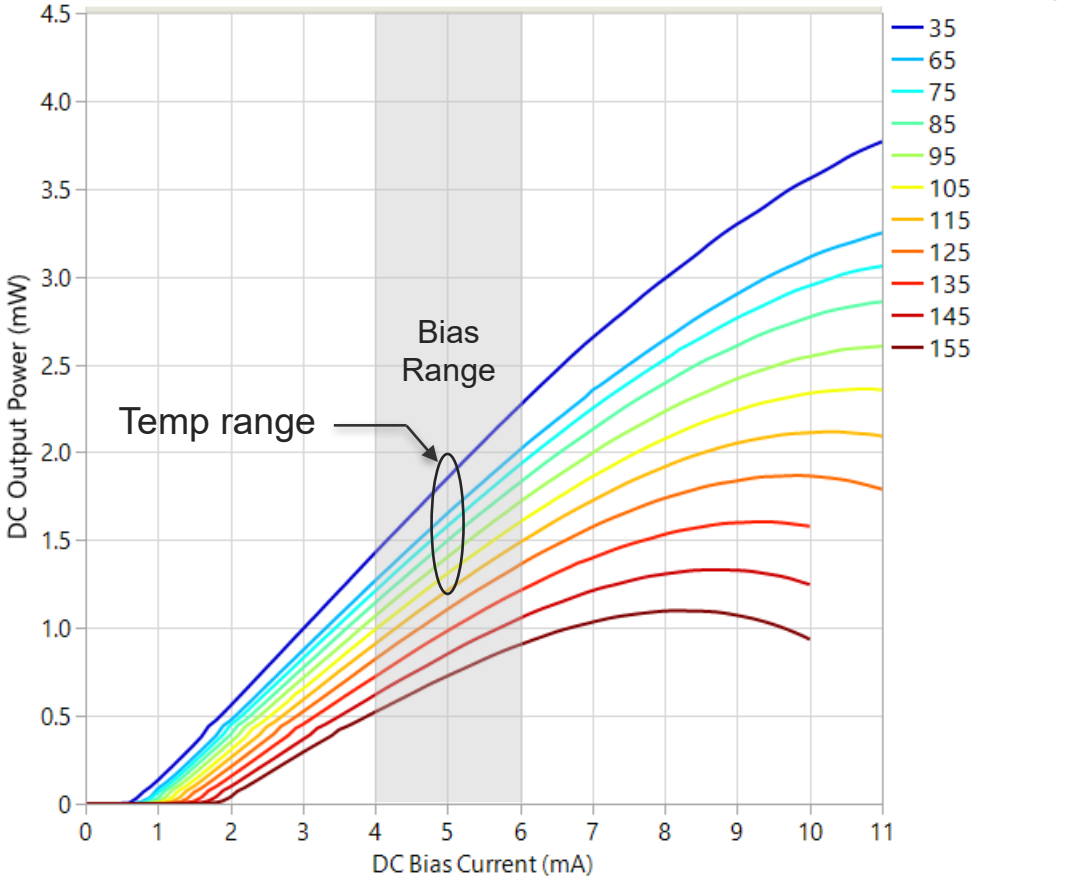
1060nm VCSEL technical benefits



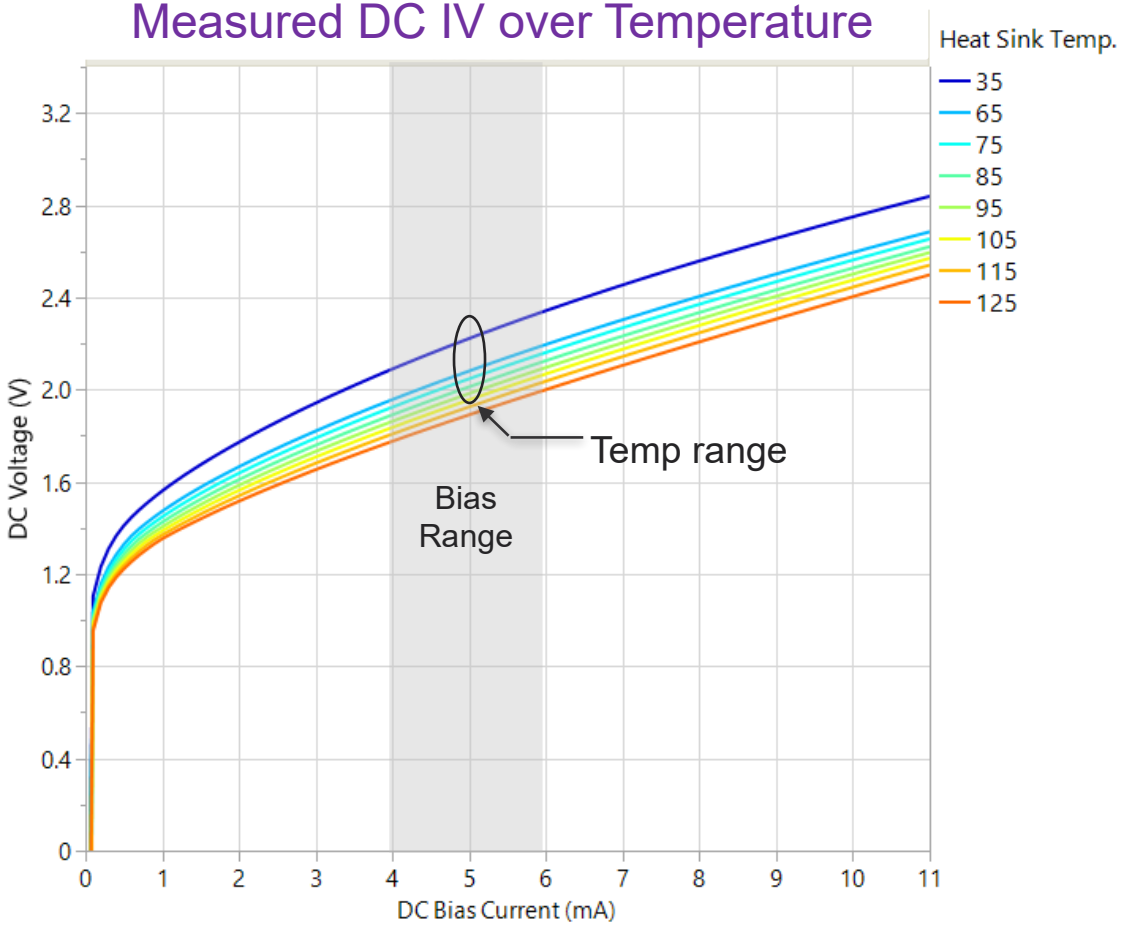
Metric	850nm	1060nm	Context
Fiber BW	+	-	Working fiber manufacturers on best path to 30m and 50m reach at 1060nm
Wall plug efficiency	+	+	Roughly equivalent efficiency, slightly lower voltage at 1060nm.
Emitter BW	-	+	Strained InGaAs active layer design enables 1.3x intrinsic BW, higher differential gain and efficiency
Signal Integrity	-	+	Flip chip integration removes group delay impedance issues known with wire-bonding..
Reliability	-	+	Flip chip and channel sparing takes FIT below 1. Al free active region enable high temp/high power reliability.
Detector technology	-	+	Flip chip detectors - higher speed / better responsivity than wire-bonded equivalent
Density	-	+	2D VCSEL arrays for high density interconnect including channel sparing
Thermal management	-	+	>20C lower laser junction, >20C lower ASIC temperature from flip chip driver/TIA assemblies
Manufacturability	-	+	Flip chip for mass reflow or TCB, also enables high accuracy placement for assembly
Volume	-	+	Builds on largest VCSEL deployments in history, reuses MFG partners, test, assembly supply chain

1060nm VCSEL | Example L-I Curves over Temperature (II)

Measured DC LI over Temperature

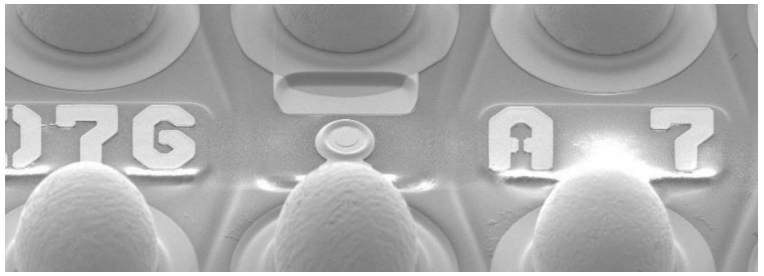


Measured DC IV over Temperature

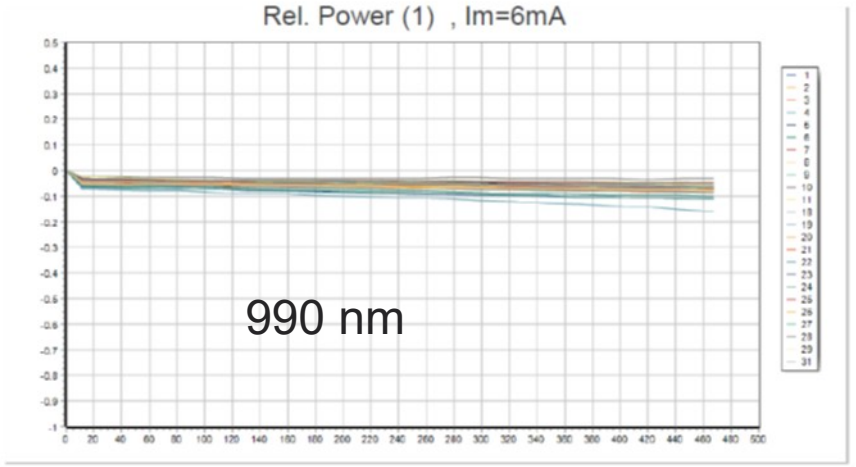


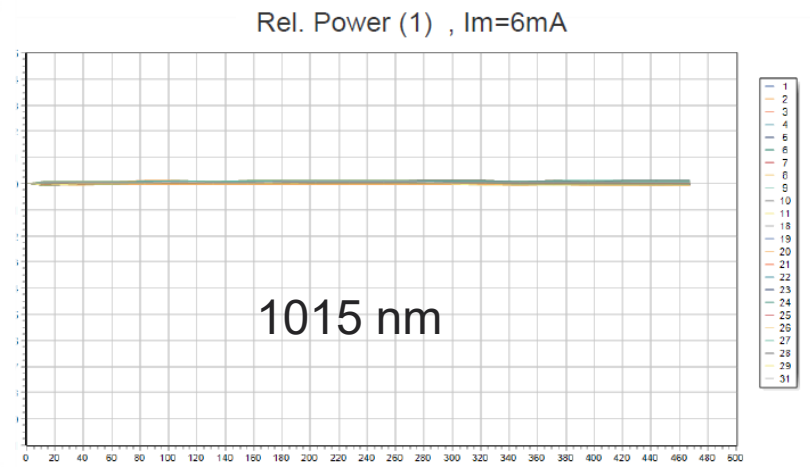
- Excellent performance with >155C operating temperature

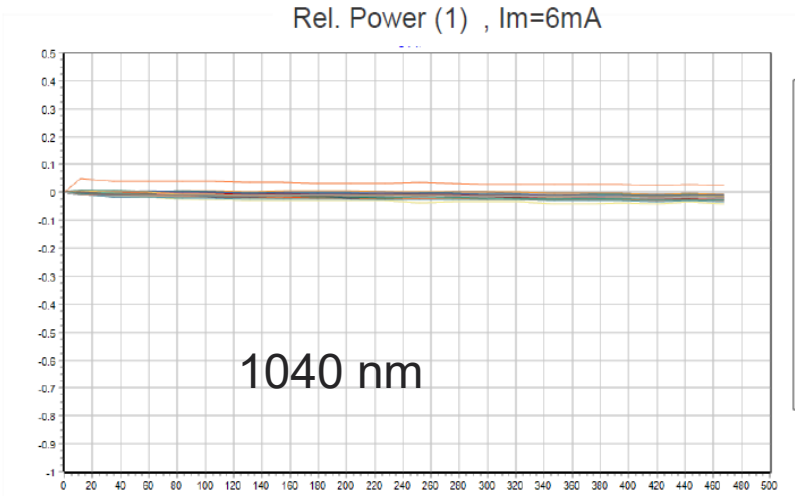
Industry Example – High Reliability to 1065nm and Bottom-Emitting

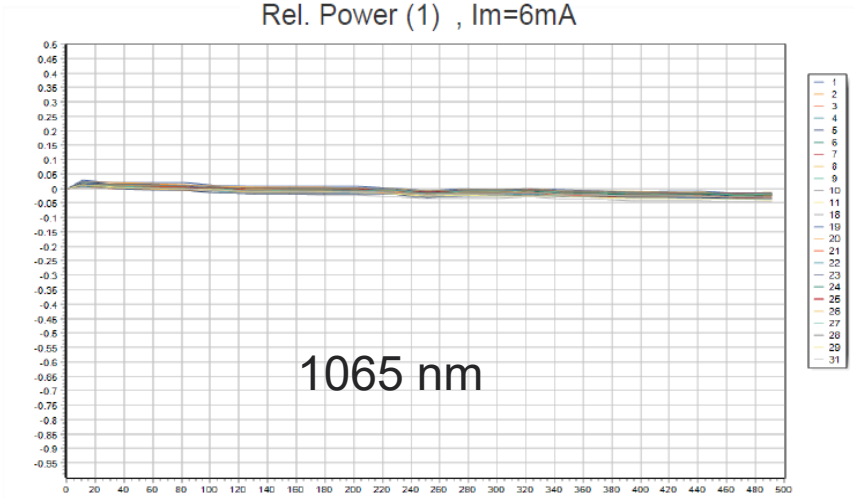


- 170°C (high acceleration) 8mA stress
- Flip-chip bottom emitting



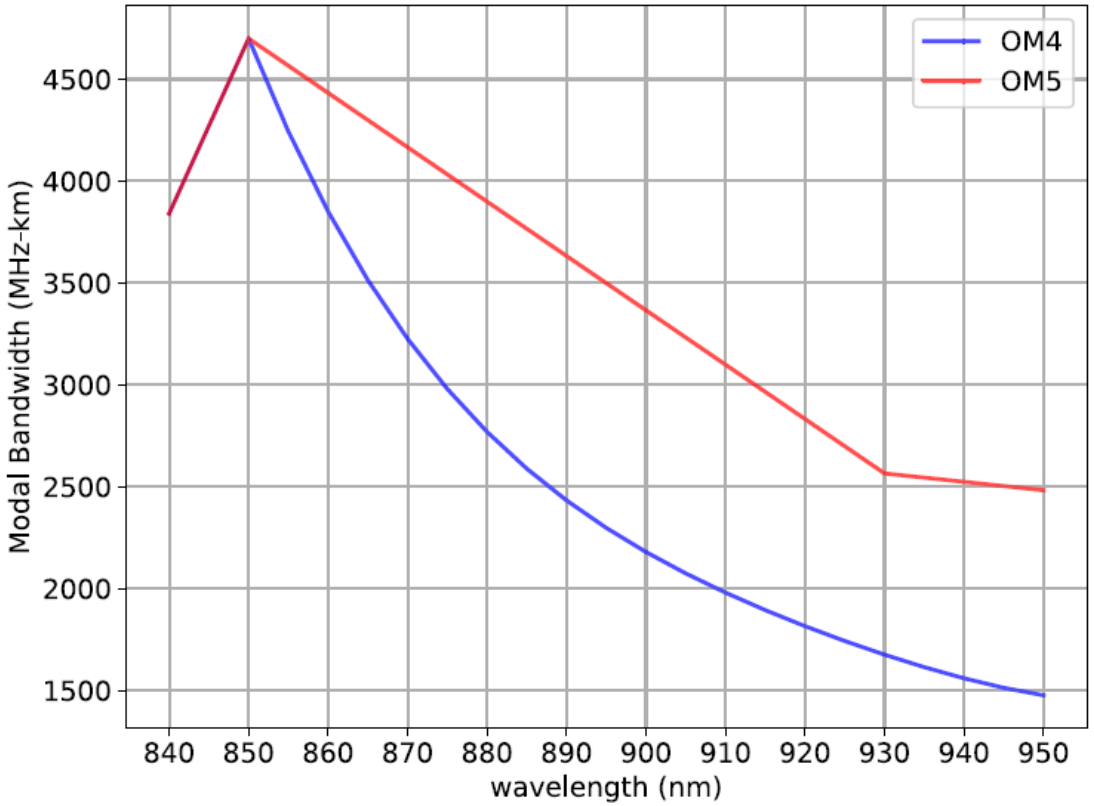






- Samples from 4 different wafers (4 different EPI designs): 0 fails after 500hrs

Fiber requirements at 1060nm



- Worst case standard OM4 EMB at 1060nm is estimated to ~820MHz*km. This suggests approximatly 10-meter reach at 200Gbps which does not meet 30 and 50m objectives
- We are proposing a new fiber with high enough EMB for 30m and 50m at 1060nm.

Conclusion

- We clarified the broad market potential for an optical interconnect targeting next gen AI datacenter clusters and the opportunity to leverage new optics technologies including advanced packaging
- Proposing IEEE802.3 200G MMF SG to approve both 30m and 50m objectives
  - Recommending the TF to consider using both 850 to 1060 nm wavelengths (with the implication of introducing two types of fiber)
- The proposal assumes using broadband PDs designed to support 850 to 1060nm wavelengths
- Calling for fiber manufacturers to contribute with information to solidify the path towards optimized fibers for 1060 nm
  - Also Requesting that the IEEE802.3 provides liaison report to the IEC SC86A/WG1 to investigate the possibility and timeline of such option

Thank you