Package-Level Considerations for 400GPL Feasibility

Examining Evaluation Boundaries Using a Correlated PKG Model

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Why Package Evaluation Matters at 400GPL

- 400GPL → Nyquist frequency exceeding 100 GHz (depending on modulation/lane rate).
- PKG insertion loss becomes more crucial in end-to-end channel than 200G/L generation.
- Simple extension of existing PKG assumptions is risky.
- PKG evaluation increasingly influences feasibility assessments.
- Current risk: pessimistic conclusions due to measurement artifacts

Problem: Feasibility Conclusions Are Boundary-Dependent

- Feasibility conclusions depend strongly on:
  - test point definition
  - inclusion/exclusion of pads & breakout

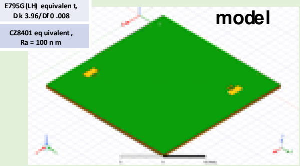
- Without consistent boundaries, results are incomparable

Approach: Correlating Measurement and EM to Enable Fair Evaluation

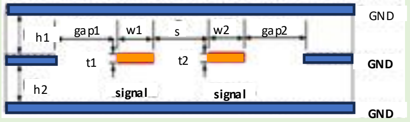
(1) original PKG design/model

material parameters
Dk, Df, Ra
“catalog values”

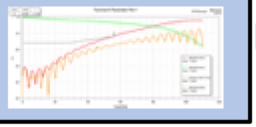
	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
Core thickness(*2)	1280 um
Cu thickness	15 um
dielectric thickness	30 um
trace line/Space (designed)	15 um /15 um (min) 23 um /63 um (BGA/NPC) 20 um /49 um (CPC)
BU material(*1)	GL107 equivalent, Dk 3.40/Df 0.0030
Core material(*1)	E795G(LH) equivalent, Dk 3.96/Df 0.008
Surface treatment(*4)	CZ8401 equivalent, Ra = 100 nm



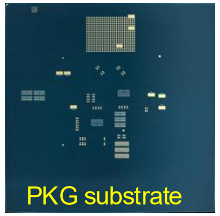
designed dimension



(2) EM-sim
designed PKG S-parameter

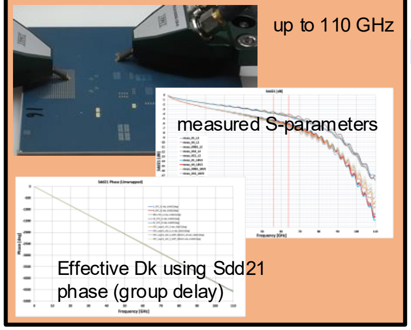


(3) PKG substrate manufacturing



(4) S-parameter measurement

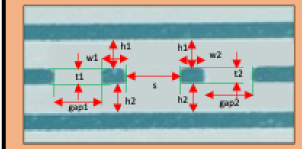
up to 110 GHz



measured S-parameters

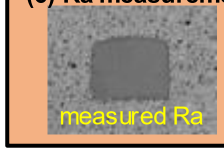
Effective Dk using Sdd21 phase (group delay)

(5) physical dimension measurement



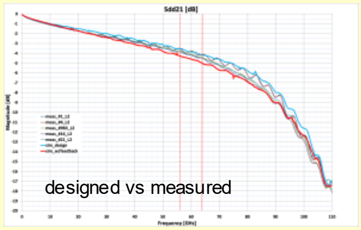
measured physical dimension

(6) Ra measurement



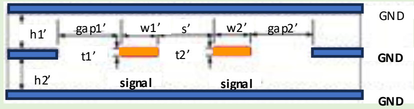
Cu surface roughness

(7) designed PKG vs measurement



designed vs measured

(8) modified PKG model based on physical dimension and measured S-parameter



Dk, Df, Ra

	spec/target
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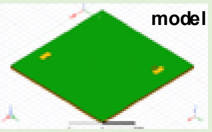
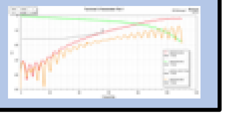
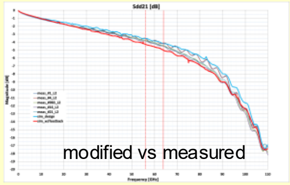


(9) EM-sim



(10) modified model vs measurement



modified vs measured

“Iteration“
- Fill the gap between design and measurement by modifying dimension, parameters in PKG model.

(11) correlated PKG model based on physical dimension and measured S-parameter

correlated dimension

material parameters
Dk, Df, Ra
“correlated values”

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
Core thickness(*2)	1280 um
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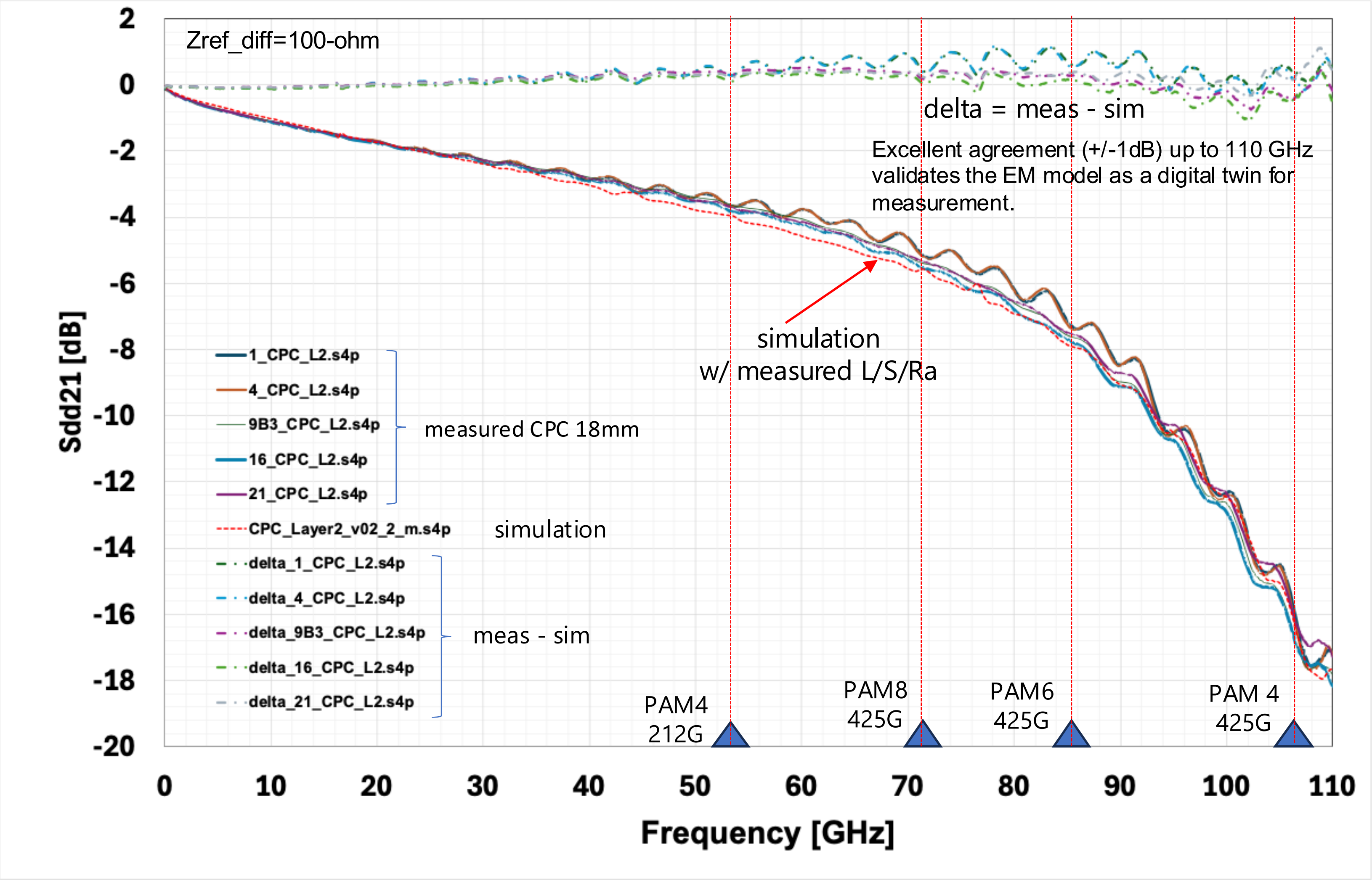
correlated PKG model

- ✓ - Measurement–EM correlation
- ✓ - Parameter refinement (Dk/Df/Ra/dimension)
- ✓ - Stepwise artifact removal

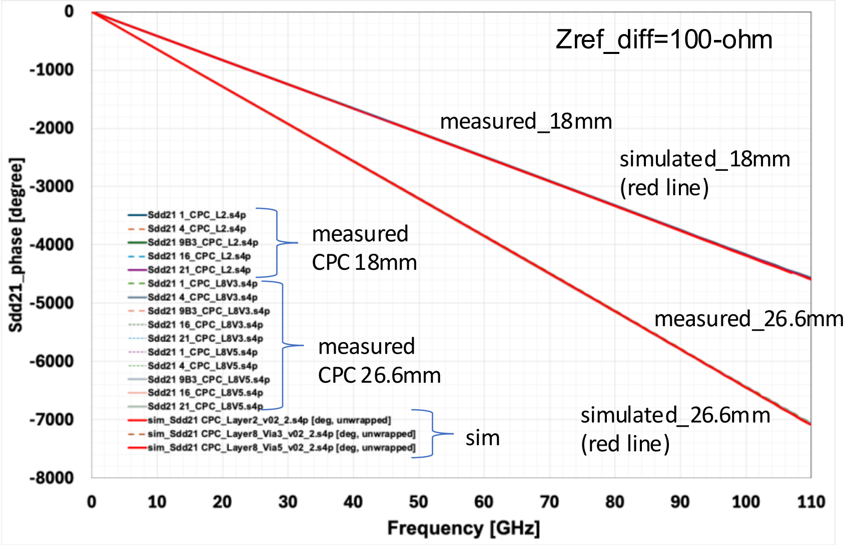
Correlated PKG Model: Agreement with Measurement



Excellent agreement (+/-1dB) up to 110 GHz validates the EM model as a digital twin for measurement.

The measured results correlate well with the simulated results of the PKG trace with the RF probe pad.

- Both bump pads and CPC pads are with RF probe pads for measurement.



- Also, simulated Sdd21 phase correlates well with measured results. (Dk_eff was derived from group delay fitting to ensure phase accuracy.)

How We Isolate Intrinsic Package Behavior

Step A: De-embedding RF Probe Interfaces:

- Remove the artifacts of the pitch GSGSG probe pads and the associated escape routing.
- This shifts the reference plane from the probe tip to the TP0d/TP5d (die-side bump pad).

Step B: Extraction of Intrinsic Channel (TP0p to TP5p):

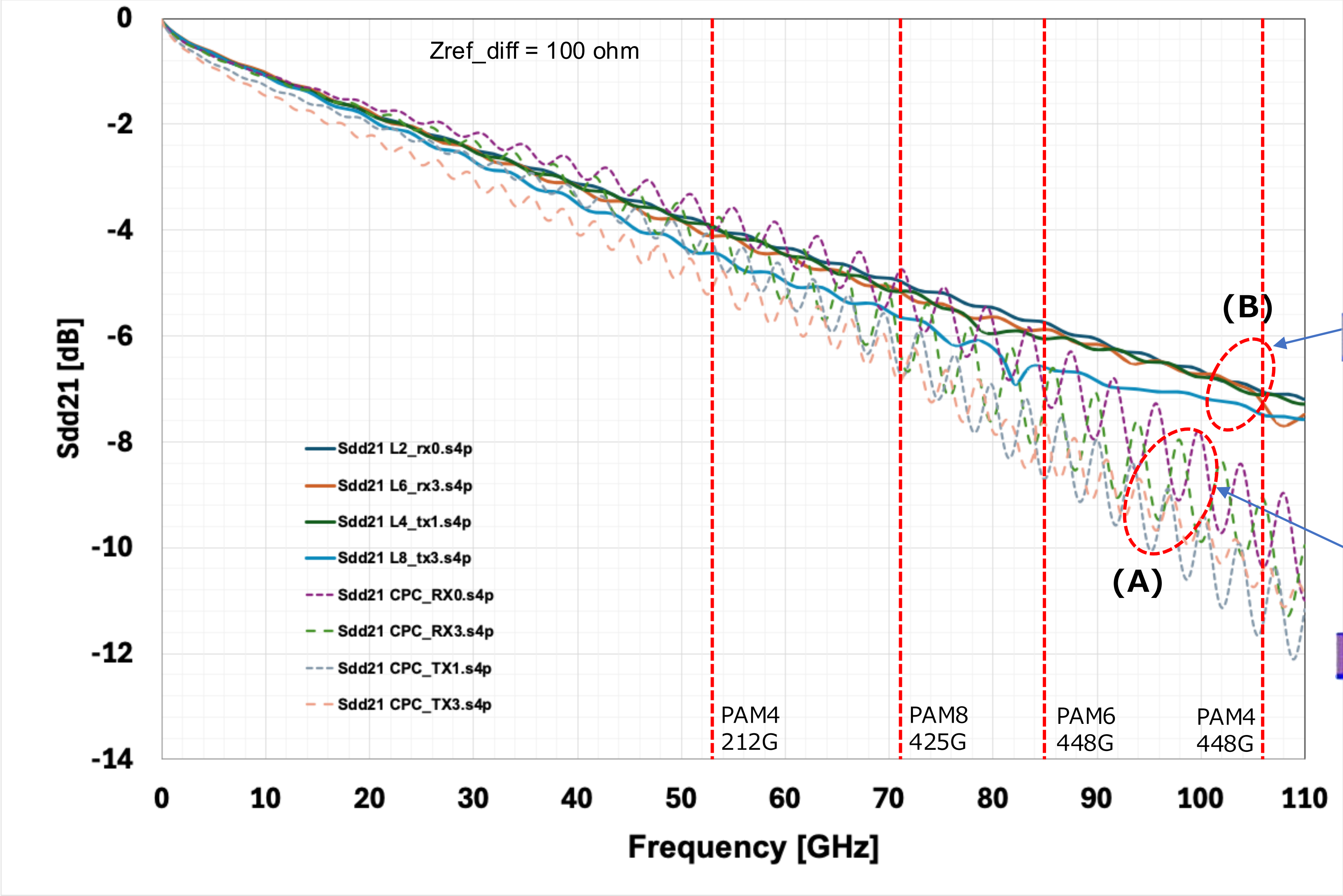
- Remove the CPC pad and the breakout region (defined as the pad plus approximately of routing).
- This isolates the intrinsic trace, leaving only the through-via and the horizontal routing.

Step C: Comparative Roll-off Analysis:

- Compare the S-parameters of the "Full Interface Model" vs. the "Intrinsic Model" to quantify the exact contribution of the CPC pad to the insertion loss roll-off.

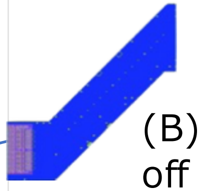
Conclusion: CPC pad dominates > 70 GHz in this measurement configuration

Observation: The >70 GHz Roll-Off Originates from Interface Effects



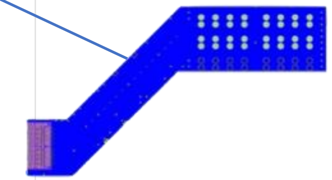
trace length [mm]

trace	(A)	(B)
L2_rx0	19.6	16.9
L6_rx3	19.5	15.8
L4_tx1	23.3	16.5
L8_tx3	25.2	16.0



(B) Without CPC pad, no significant roll off is observed even with bump pad.

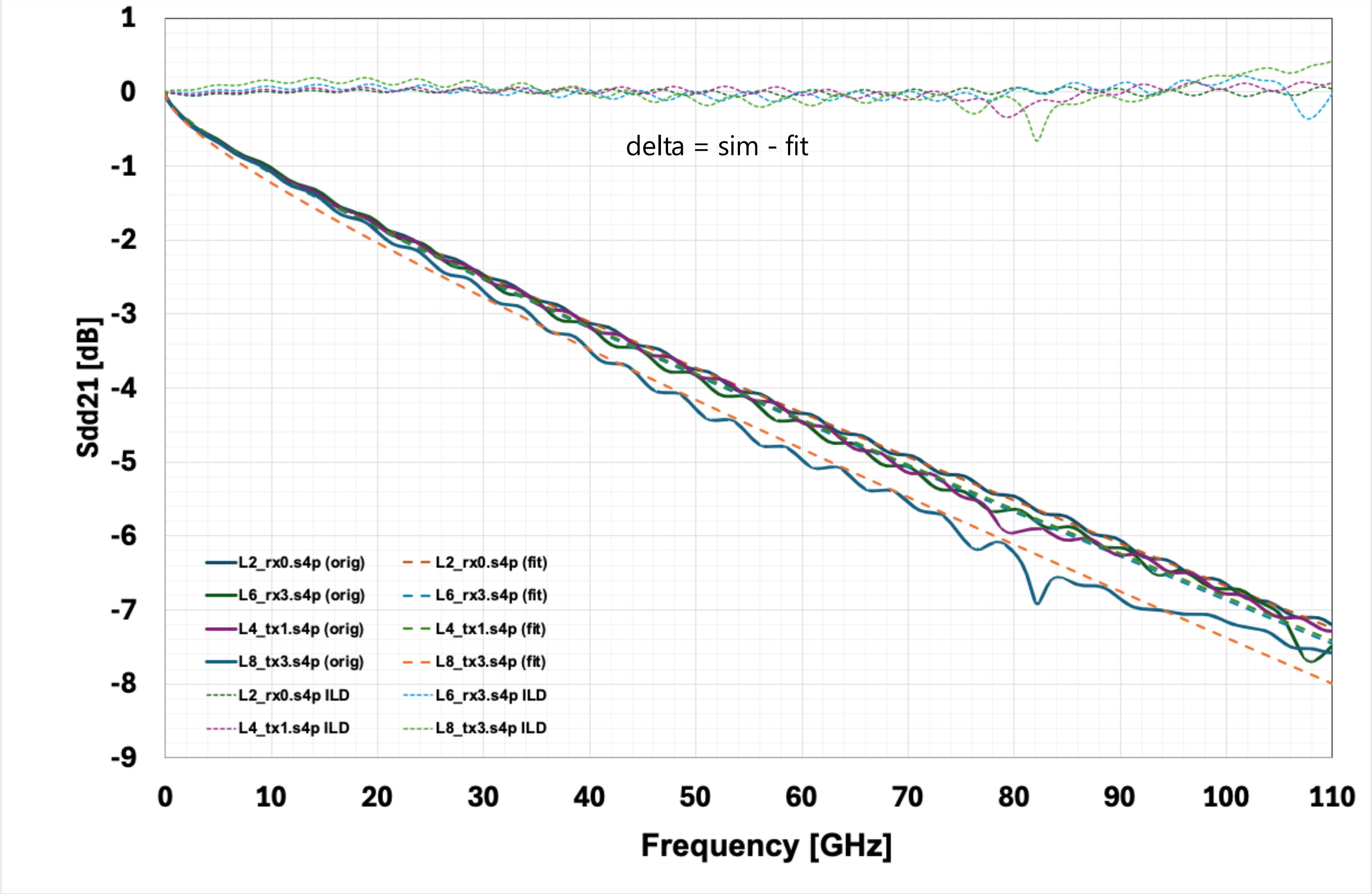
(A) Without RF probe pad and with CPC pad, significant roll off is still observed.



	RF probe pad	CPC pad/ breakout	bump pad	PKG channel
(A)	no	yes	yes	TP0d/TP5d ~ TP0p/TP5p
(B)	no	no	yes	TP0d/TP5d ~ TP0/TP5

CPC pad & breakout dominate the observed roll-off in this configuration.

Intrinsic PKG Traces Without Interface Effects



(B) Without CPC pad, fitting to simple equation

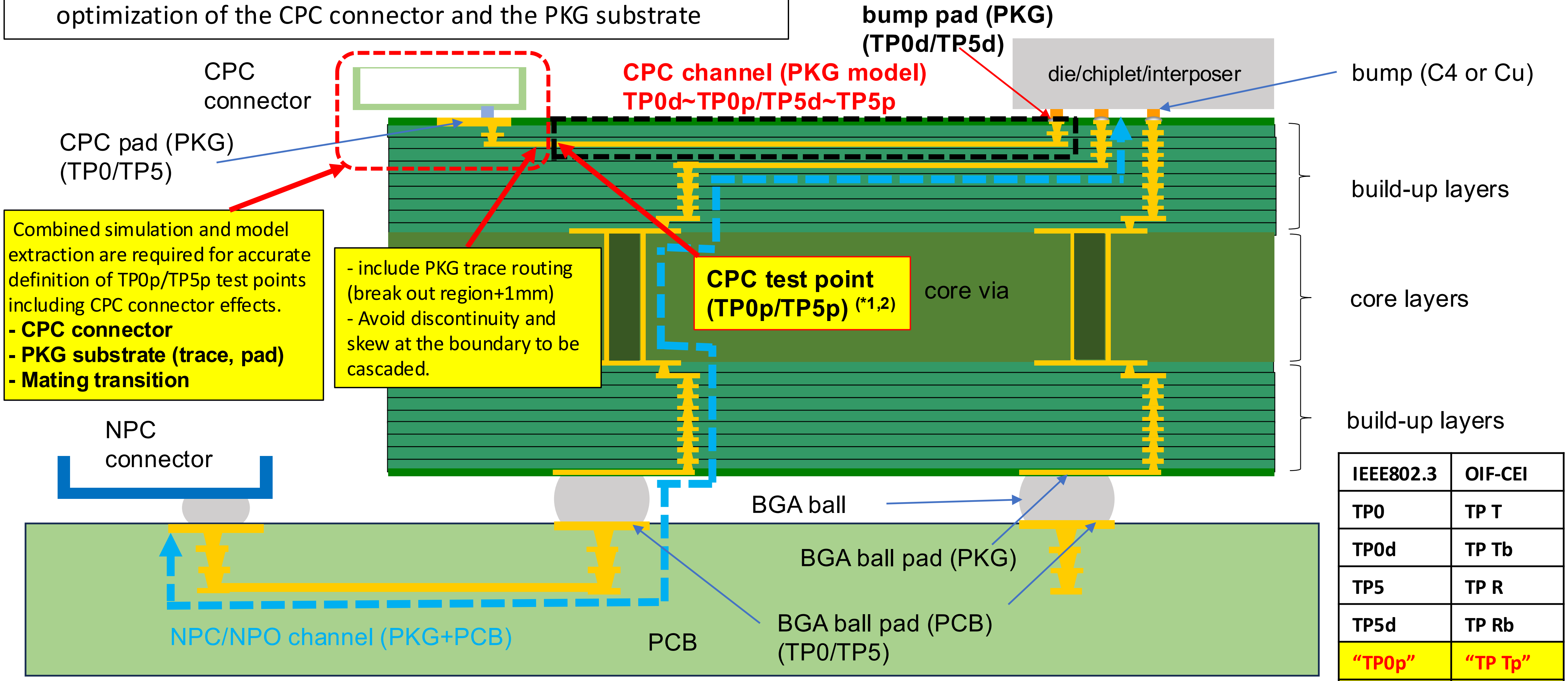
$$Sdd21_{fit} = a1 \cdot f^{0.5} + a2 \cdot f$$

(intrinsic PKG trace only) correlates well with the model. (~+/-0.5dB up to 110 GHz)

- No fundamental roll-off is observed up to ~110 GHz under the evaluated boundary conditions.

Implication: CPC Interfaces Require Co-Design

- Clear ownership boundaries: TP0p/TP5p allow for independent optimization of the CPC connector and the PKG substrate



Combined simulation and model extraction are required for accurate definition of TP0p/TP5p test points including CPC connector effects.

- CPC connector

- PKG substrate (trace, pad)

- Mating transition

- include PKG trace routing (break out region+1mm)
- Avoid discontinuity and skew at the boundary to be cascaded.

IEEE802.3	OIF-CEI
TP0	TP T
TP0d	TP Tb
TP5	TP R
TP5d	TP Rb
"TP0p"	**"TP Tp"**
"TP5p"	**"TP Rp"**

- Tentative definition and it is under discussion.

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*1: "Co-Package Copper for 400G", oif2025.465.00 (page-3)

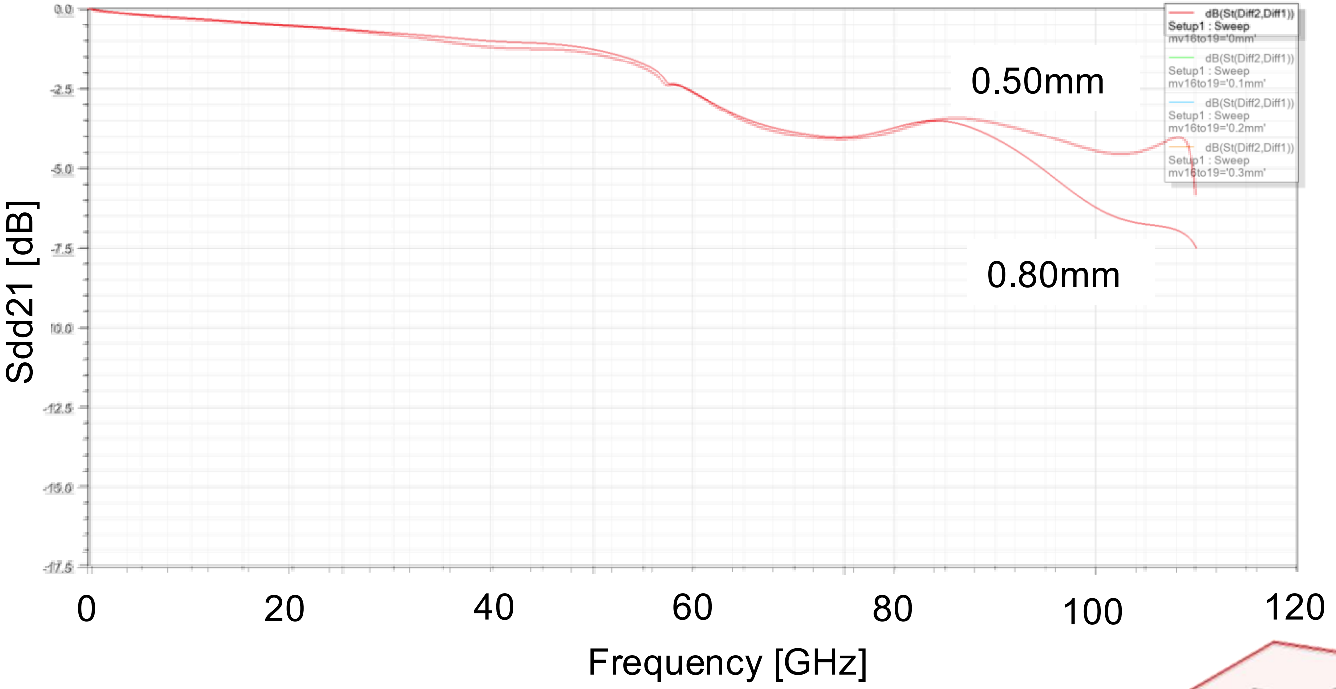
*2: "Refined Test Points for 400 Gb/s CPC AI Use Cases", mellitz_e4ai_01_251023.pdf

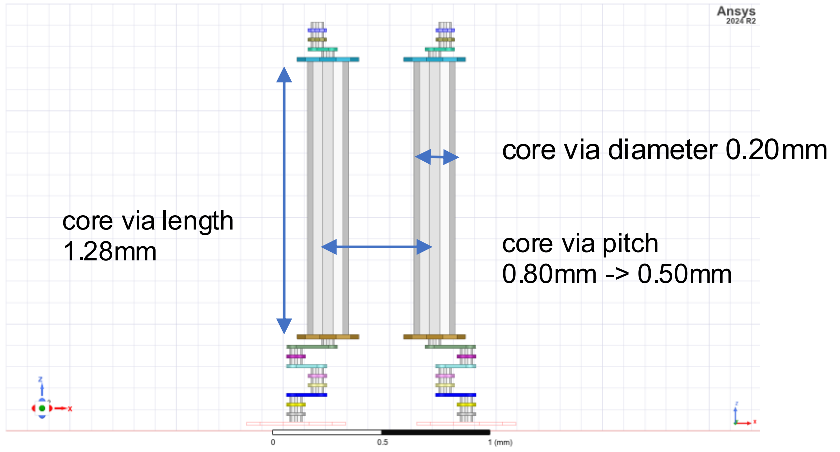
NPC/BGA: Directional Considerations for Future Work

- Simply reduce core via pitch as a trial.
  0.80mm -> 0.50 mm

- > 85 GHz IL improvement is observed.

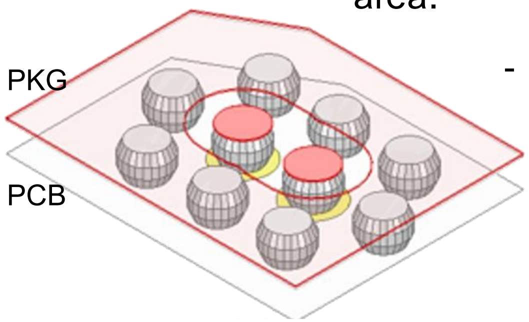
Sdd21 (core via + BU via only, no trace or pad included)





- With more tuning, the characteristics may be improved further.
  - via size, via length (thickness),
  - GND via (number, distance)
  - core material (Dk, Df, conductivity)

- It is also necessary to consider BGA pad and ball itself, together with PCB footprint, breakout, and GND layout.
  - For this portion, it is also required co-simulate PKG and PCB together, like what is required for CPC connector area.



- On the other hand, BGA pitch reduction involves a critical trade-off between > 85 GHz IL improvement and long-term thermo-mechanical reliability.

What This Means for Early 400GPL SG Discussions

- **Importance of boundary definition for performance evaluation**

- **PKG/channel (CPC/PCB) co-design is critical.**

- **Informs realistic assumptions for 400G+class standardization and PKG/channel co-design.**

Summary and Discussion Points

- **Correlated EM models reveal intrinsic potential of package traces.**

- **The >70 GHz roll-off is dominated by distributed parasitic effects at the CPC pad interface, including impedance mismatch and energy diversion (e.g., radiation).**

- RF probe pads and bump pads have minor impact compared to CPC pads/breakout.

- Standardized boundary definitions (TP0p/TP5p) are a prerequisite for fair and comparable feasibility assessments.

- This work does not claim all CPC pads cause the same roll-off, but demonstrates a methodology to separate intrinsic PKG characteristics from pad-induced artifacts.

- Avoids overestimating high-frequency limits by separating CPC pad/breakout effects from PKG traces.

- We hope this contribution provides useful input for early SG discussions on consistent package-level evaluation assumptions.

- TP0p/TP5p boundaries used here are tentative and subject to SG discussion.

Appendix

A. Test PKG Overview
B. Model correlation with measured data
C. How we isolate intrinsic PKG behavior
D. COM PKG model Assumptions and Scope
E. Material Sensitivity

A. Test PKG Overview

	spec/target
PKG Size	65.0 mm x 65.0 mm
Trace Length: Bump Pad ~ BGA Ball	33.0 mm/45.0 mm
Trace Length: Bump Pad ~ CPC Pad	18.0 mm/26.6 mm
BGA Ball Pitch / Size	0.8 mm (hexagonal) / 0.50mm (dia)
CPC Pad Pitch / Size	PN pair: 0.6 mm Tx-Tx/Rx-Rx: 1.2 mm (vert) Tx-Tx/Rx-Rx: 1.8 mm (horz) Tx-Rx: 1.8 mm (vert) / 0.43mm (dia)
Differential Impedance	92.5 ohm

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total Thickness	2176 um
Core Thickness (*2)	1280 um
Cu thickness	15 um
Dielectric Thickness	30 um
Trace Line/Space (designed)	15 um /15 um (min) 23 um/63 um (BGA/NPC) 20 um/49 um (CPC)
BU Material(*1)	GL107 equivalent, Dk 3.40/Df 0.0030
Core Material(*1)	E795G(LH) equivalent, Dk 3.96/Df 0.008
Surface Treatment(*4)	CZ8401 equivalent, Ra = 100 nm

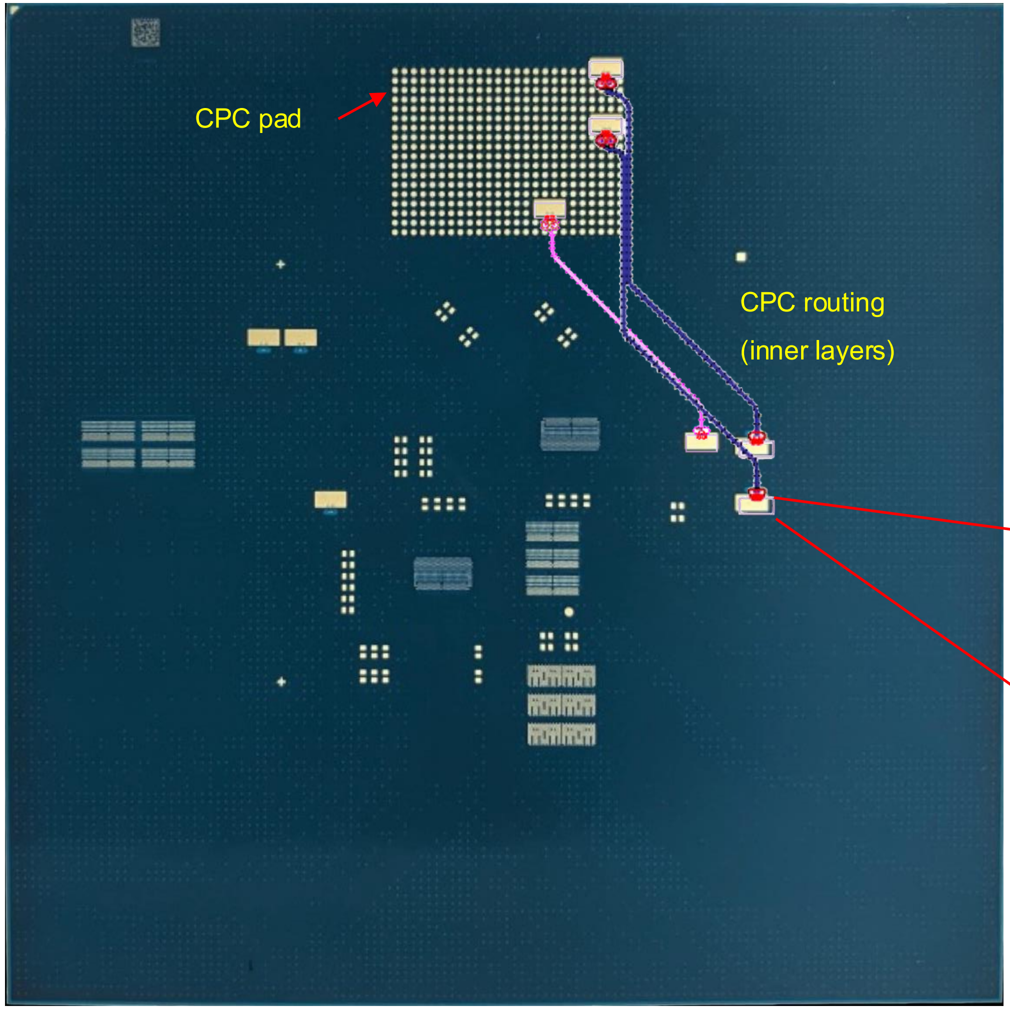
- Assuming "class B(*3)" equivalent usage.
  - high radix/lane count
  - high density
  - no skip layers

(*1): at Room Temp. @60 GHz
- material vendor's "table value"
(*2): Assuming large PKG size ~120 mm-sq,
- Also to mitigate PKG warpage.
(*3): Please refer to IEEE P802.3dj draft.
(*4): Vendor's "catalog value"

CPC: Co-Packaged Copper
NPC: Near Package Copper (Using BGA ball and PCB connection)
BU: Build Up

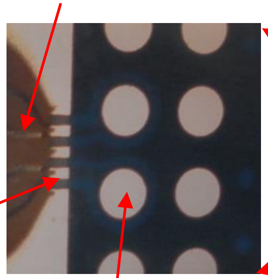
A.1 PKG Substrate (CPC)

top view (bump/CPC side)



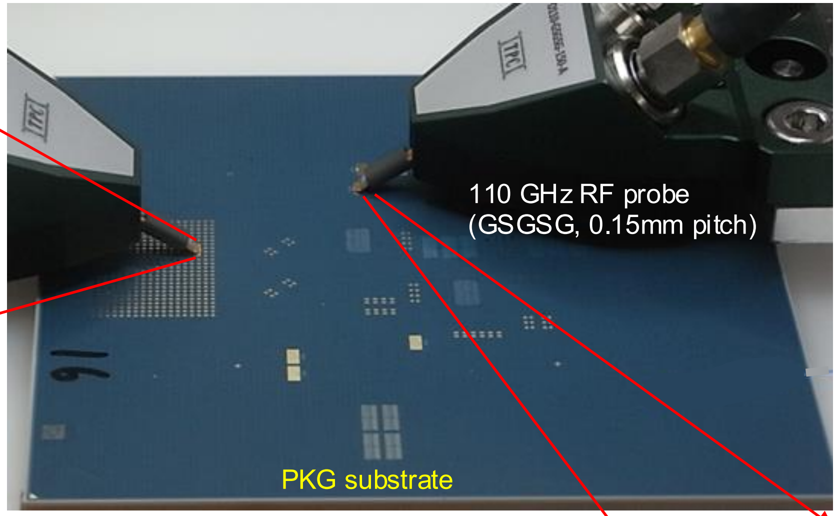
Both bump pads and CPC pads are with RF probe pads for measurement.

RF probe

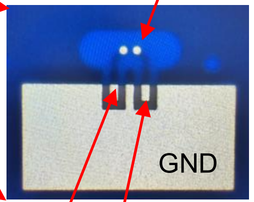


RF probe pad
0.15mm pitch
0.08mm W

CPC pad
0.60 mm pitch
0.43mm dia



bump pad



signal

RF probe pad

- To measure up to 110 GHz, 0.15mm pitch GSGSG RF probe was used.
- To absorb the different pitch (CPC pad, bump pad), additional PKG routing was required to the RF probe pads.

- We understand this may introduce artificial effects in measurement. By taking correlation and measurement, we can build the correlated model and eliminate these effect in simulation.

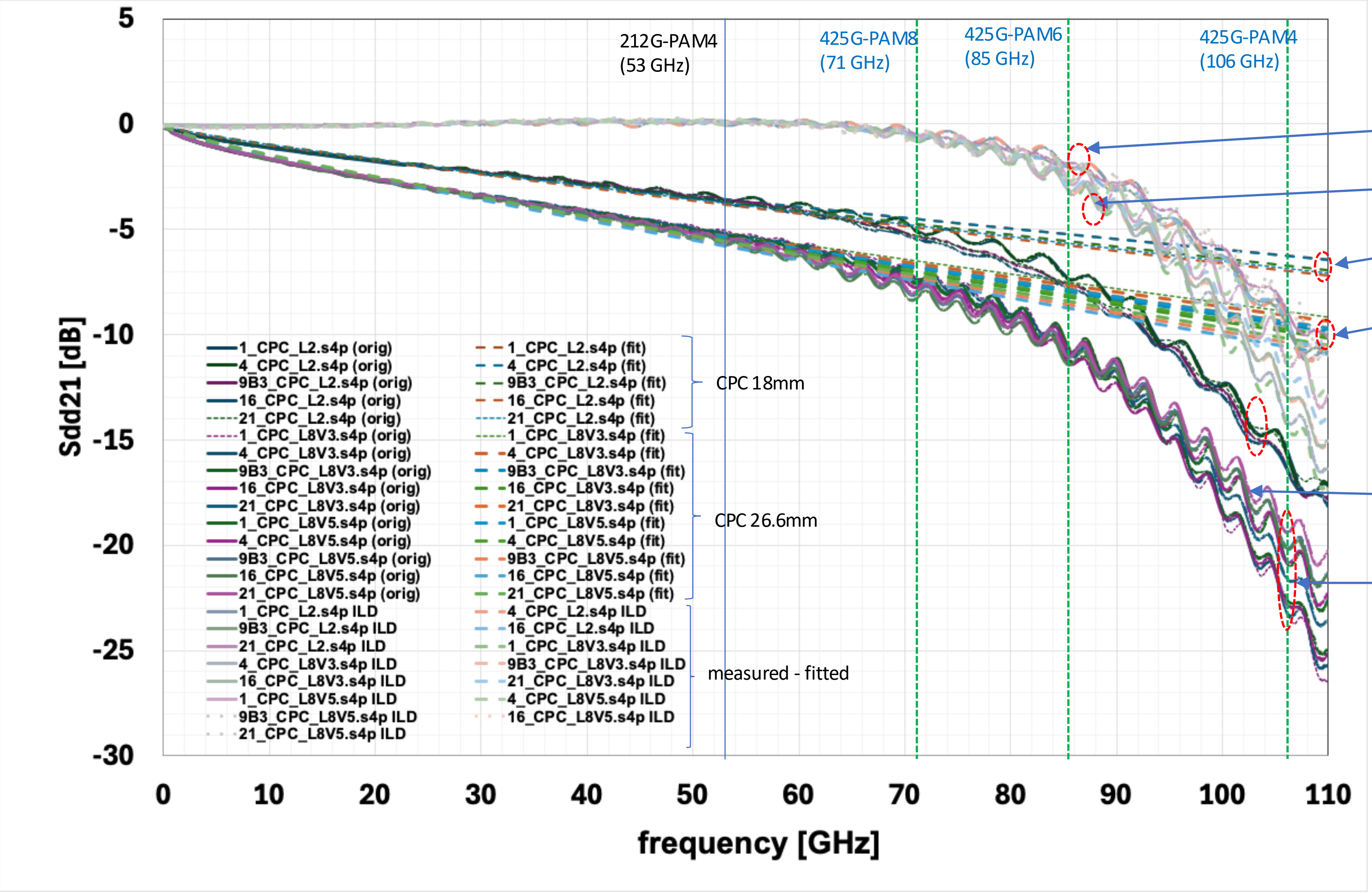
RF probe

reference plane
at RF probe tip
(calibration is done here)

A.1.1 measured Sdd21 (CPC)

fitting function

$$Sdd21_{fit} = \underbrace{a1 \cdot f^{0.5}}_{\text{conductor}} + \underbrace{a2 \cdot f}_{\text{dielectric}}$$



measured - fitted_18mm

measured - fitted_26.6mm

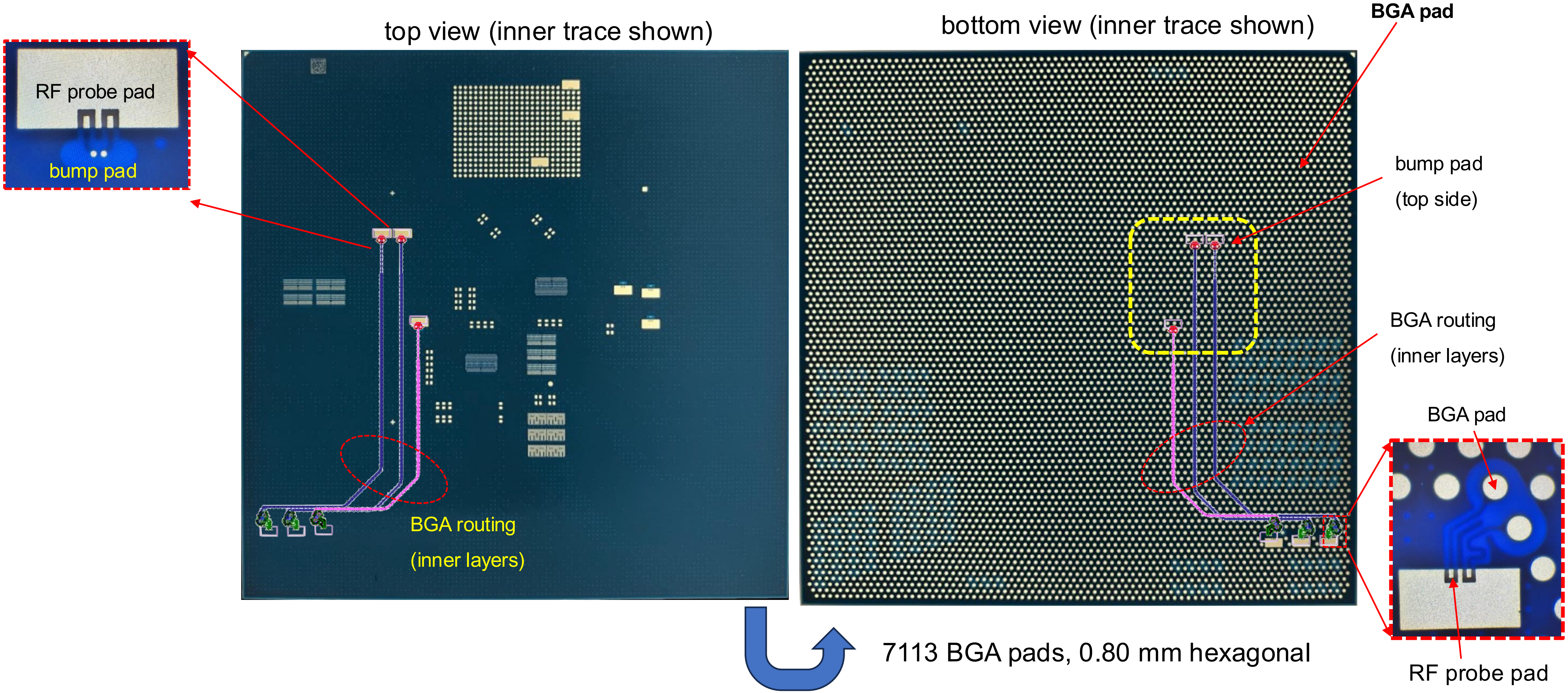
fitted_18mm(up to 70 GHz)

fitted_26.6mm(up to 70 GHz)

measured_18mm (5-samples)

measured_26.6mm (2-type x 5-samples)

A.2 Test Package Substrate (NPC/BGA)

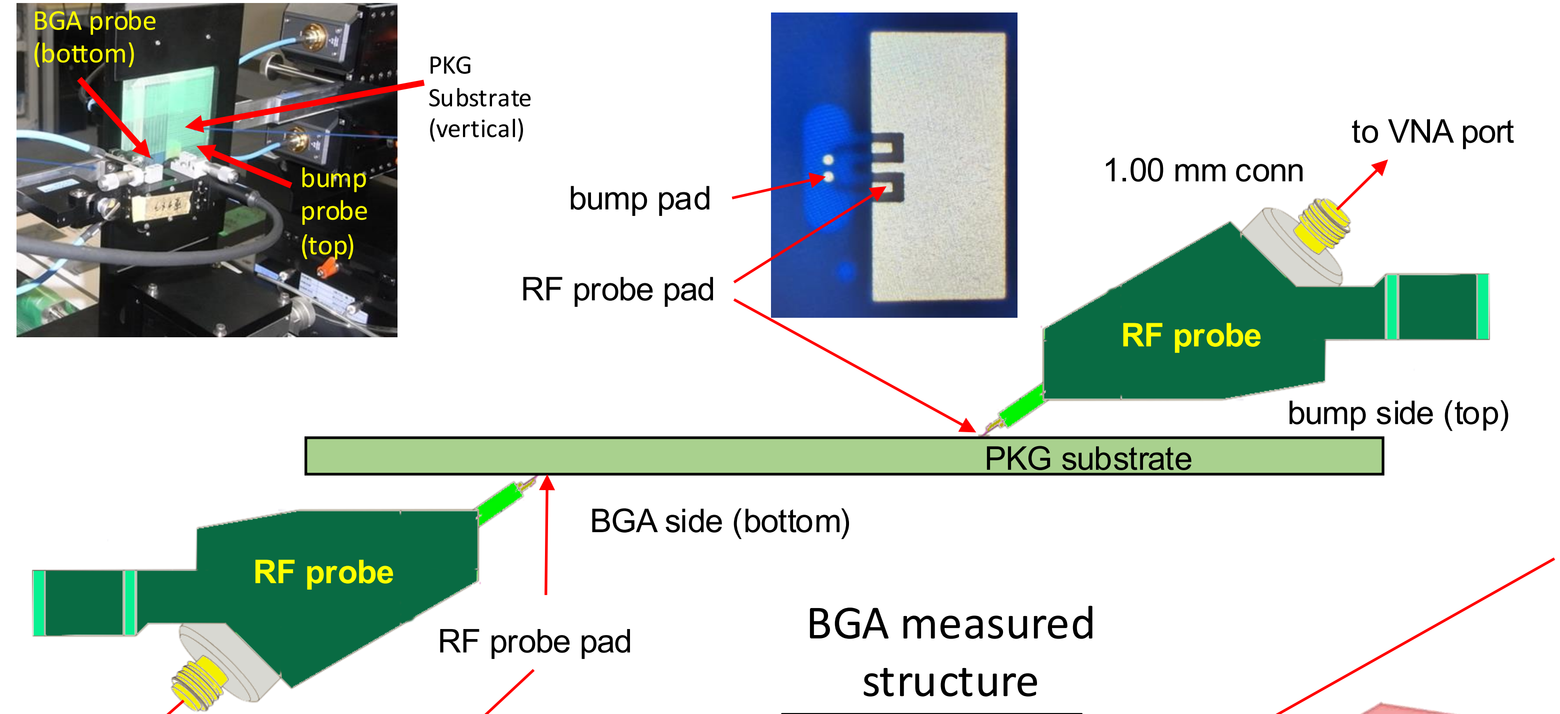


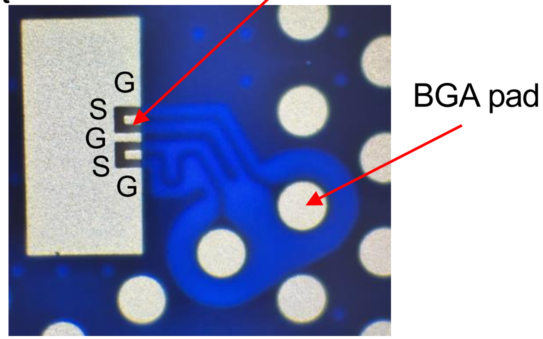
top view (inner trace shown)

bottom view (inner trace shown)

7113 BGA pads, 0.80 mm hexagonal

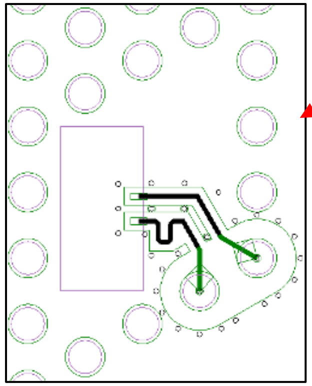
A.2.1 PKG Substrate (NPC/BGA) Measurement

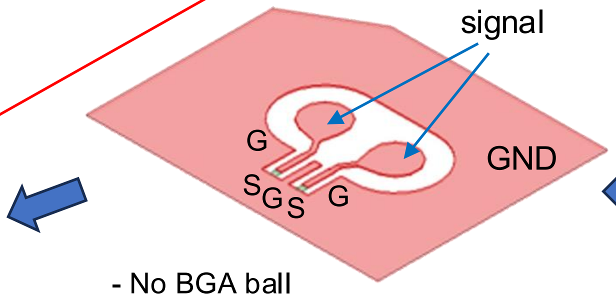




- Measurement of the NPC/BGA substrate required simultaneous probing from both top and bottom sides to capture through-path characteristics.
- This caused "fixed" RF probe direction for stable measurement.
- As the BGA balls are hexagonally placed, it is necessary to route from BGA ball pad to RF probe pad with "non-straight" routing lines.

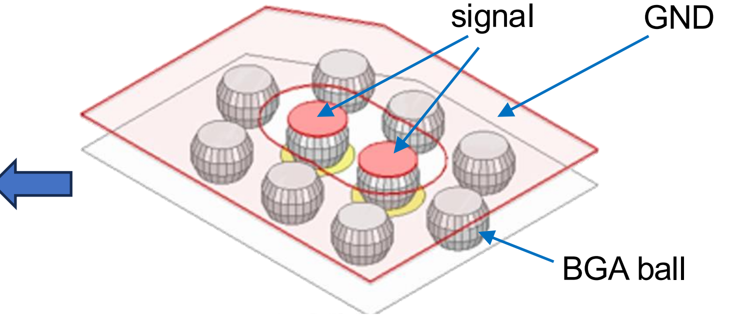
BGA measured structure





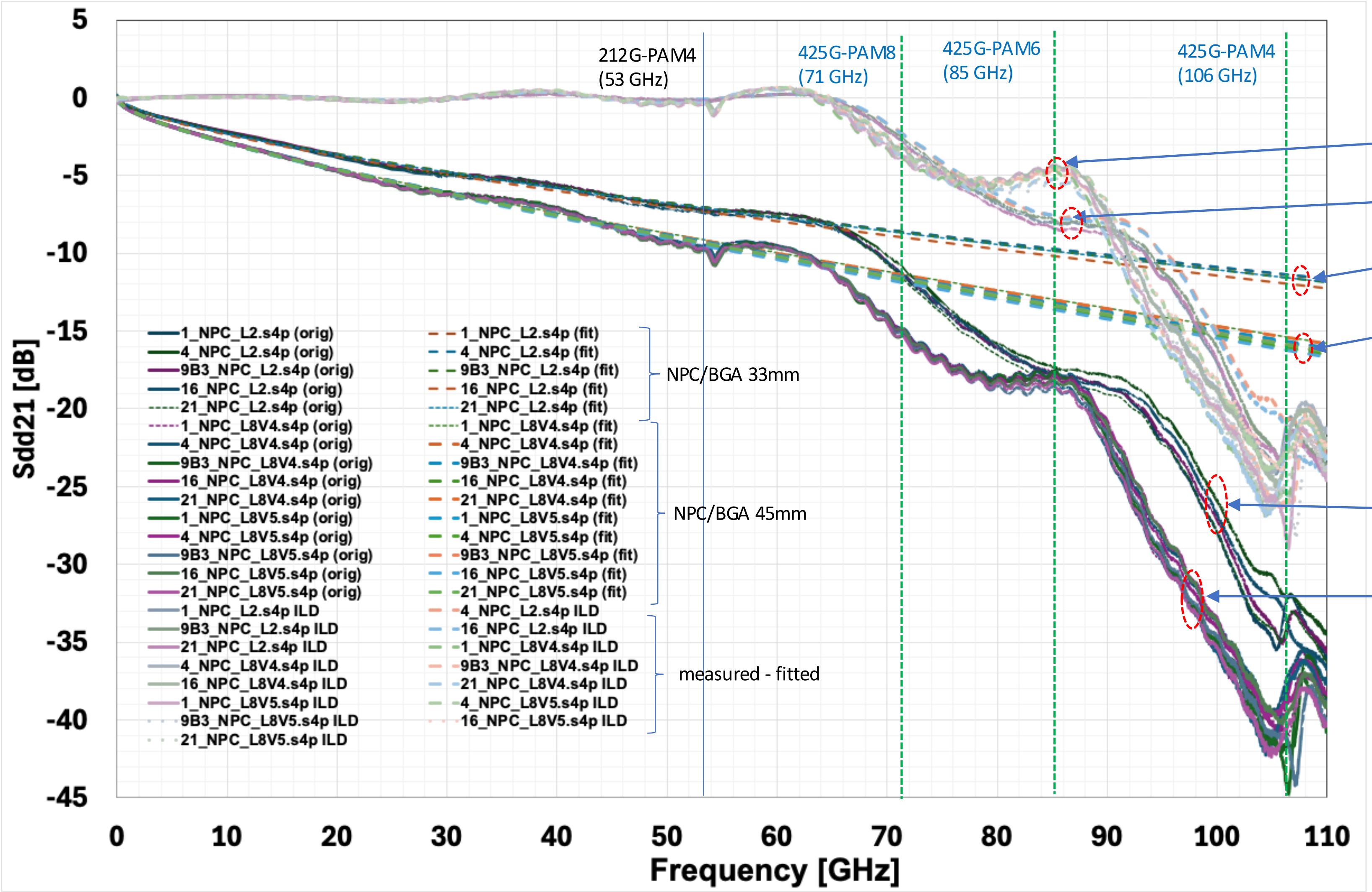
- No BGA ball
- 150um RF probe pitch
- GSGSG

BGA actual structure



- RF probe cannot probe directly, due to pad pitch (0.8mm).
- Need "GSGSG" structure for 110 GHz measurement.

A.2.2 measured Sdd21 (NPC/BGA)



fitting function

$$Sdd21_{fit} = \underbrace{a1 \cdot f^{0.5}}_{\text{conductor}} + \underbrace{a2 \cdot f}_{\text{dielectric}}$$

measured - fitted_45mm

measured - fitted_33mm

fitted_33mm(up to 70 GHz)

fitted_45mm(up to 70 GHz)

measured_33mm (5-samples)

measured_45mm (2-types x 5-samples)

B. Model correlation with measured data

(1) original PKG design/model

material parameters
Dk, Df, Ra
"catalog values"

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
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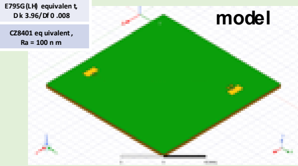
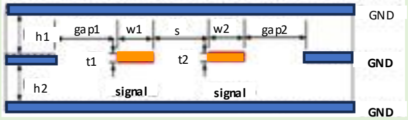
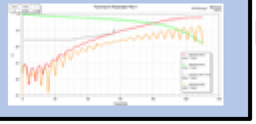


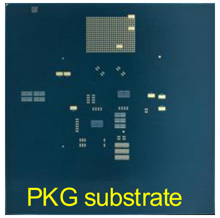
designed dimension



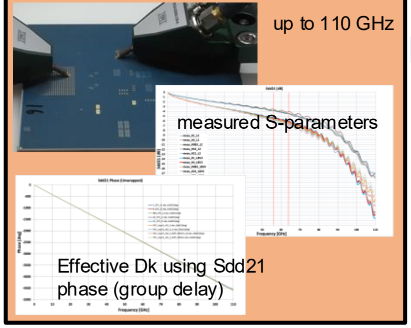
(2) EM-sim
designed PKG S-parameter



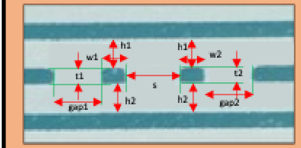
(3) PKG substrate manufacturing



(4) S-parameter measurement

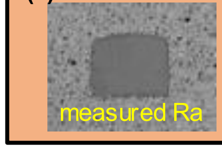


(5) physical dimension measurement



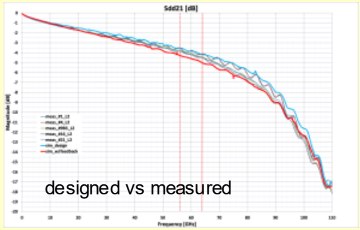
measured physical dimension

(6) Ra measurement

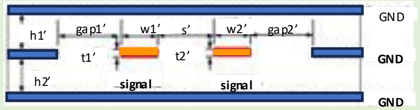


Cu surface roughness

(7) designed PKG vs measurement



(8) modified PKG model based on physical dimension and measured S-parameter

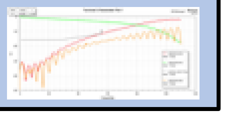


Dk, Df, Ra

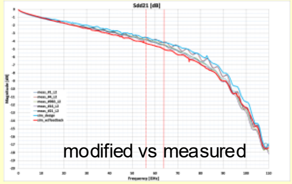
	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
Core thickness$^{(*2)}$	1280 um
Cu thickness	15 um
dielectric thickness	30 um
trace line/Space (designed)	15 um /15 um (min) 23 um /63 um (BGA/NPC) 20 um /49 um (CPC)
BU material$^{(*1)}$	GL107e quivalent, Dk 3.40/Df 0.0030
Core material$^{(*1)}$	E795G(LH) equivalent, Dk 3.96/Df 0.008
Surface treatment$^{(*4)}$	CZ8401 equivalent, Ra = 100 nm

* The physical dimension values do not always exactly match to "electrical" dimension.

(9) EM-sim



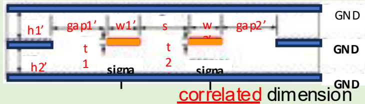
(10) modified model vs measurement



"Iteration"
- Fill the gap between design and measurement by modifying dimension, parameters in PKG model.

"less discrepancies"
"improved agreement"

(11) correlated PKG model based on physical dimension and measured S-parameter



correlated dimension

material parameters
Dk, Df, Ra
"correlated values"

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
Core thickness$^{(*2)}$	1280 um
Cu thickness	15 um
dielectric thickness	30 um
trace line/Space (designed)	15 um /15 um (min) 23 um /63 um (BGA/NPC) 20 um /49 um (CPC)
BU material$^{(*1)}$	GL107e quivalent, Dk 3.40/Df 0.0030
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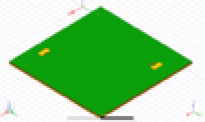
Surface treatment$^{(*4)}$	CZ8401 equivalent, Ra = 100 nm

correlated PKG model



(1) dimension: trace width, space, dielectric thickness,
- material parameters: Dk, Df, Ra, conductivity
  - "catalog" values, material vendor parameters (raw material measured)
- The model includes structures for measurement. (RF probe pad and trace) And also bump pad and BGA pad.

(8) dimension: measured values from cross sectional measurement (L/S,h/t, Ra) (5) (6)
(4) Dk_eff: fitting to measured Sdd21 phase (group delay)

C. How we isolate intrinsic PKG behavior

Step A: De-embedding RF Probe Interfaces:

- Remove the artifacts of the 0.15mm pitch GSGSG probe pads and the associated escape routing.
- This shifts the reference plane from the probe tip to the TP0d/TP5d (die-side bump pad).

Step B: Extraction of Intrinsic Channel (TP0p to TP5p):

- Remove the CPC pad and the breakout region (defined as the pad plus approximately of routing).
- This isolates the intrinsic trace, leaving only the through-via and the horizontal routing.

Step C: Comparative Roll-off Analysis:

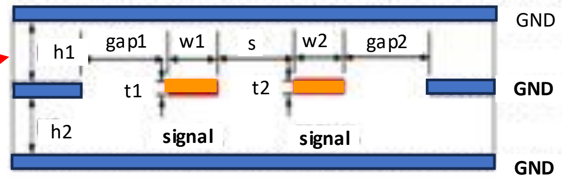
- Compare the S-parameters of the "Full Interface Model" vs. the "Intrinsic Model" to quantify the exact contribution of the CPC pad to the insertion loss roll-off.

Conclusion: CPC pad dominates > 70 GHz in this measurement configuration

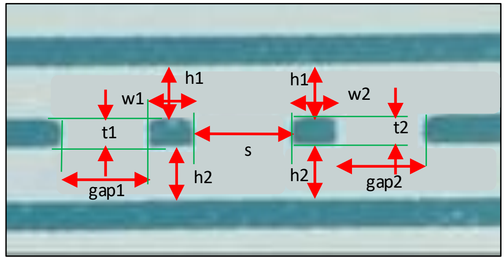
C.1 Excluding Measurement Effects

- 1st step : (1), (2)
  - dimension: trace width, space, Cu/dielectric thickness,
  - material parameters: Dk, Df, Ra, conductivity
    - “catalog” values, material vendor parameters (raw material)

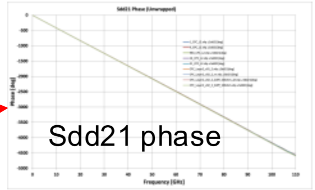
Designed

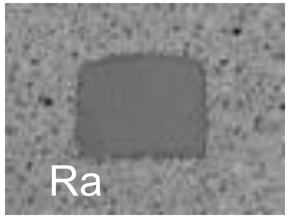


Measured

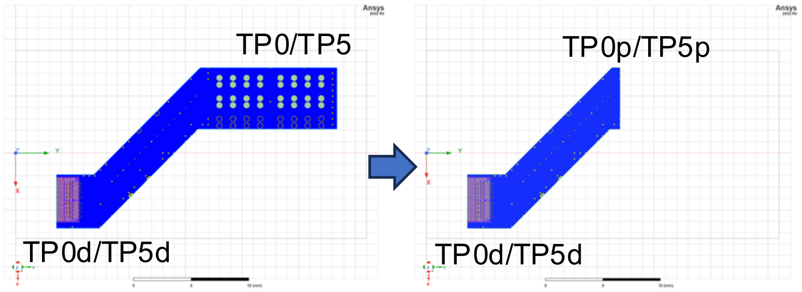


- 2nd step: (5),(6),(8),(9)
  - dimension: measured values from cross sectional measurement (L/S,h/t, Ra)
  - Dk_eff: fitting to measured Sdd21 phase/ group delay





- Exclude CPC pad and RF probe pad effects by simulation model modification.
  - Update COM PKG model using updated CPC PKG trace model (tentative TP0p/TP5p)



- 3rd step (next steps): Modify dimension, structure and material parameters will be available for production in 2~3 years.

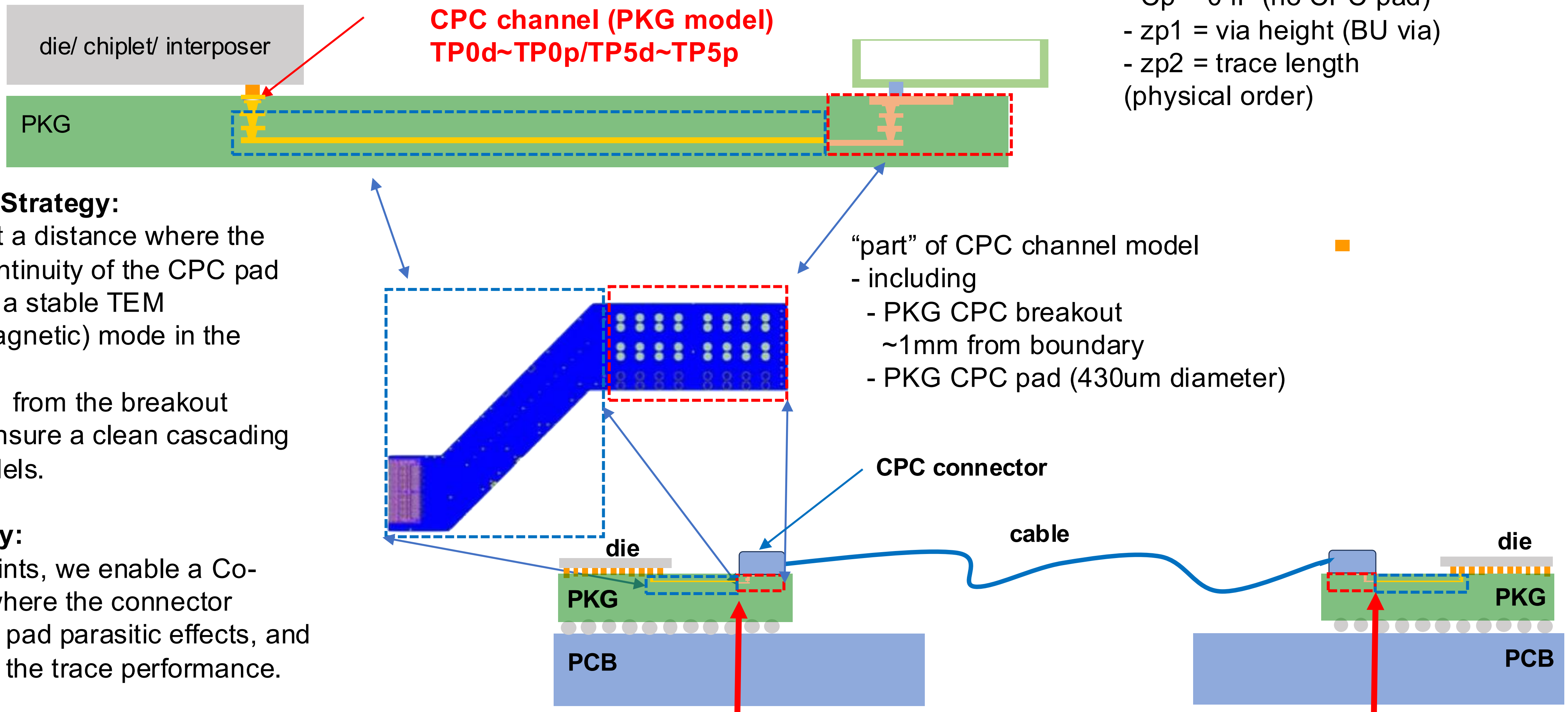
C.2 CPC Test Point: TP0p/TP5p (COM PKG model)

Boundary Definition Strategy:

- Define TP0p/TP5p at a distance where the electromagnetic discontinuity of the CPC pad has fully decayed into a stable TEM (Transverse Electromagnetic) mode in the package trace.
- Current Assumption: from the breakout boundary is used to ensure a clean cascading plane for channel models.

Mechanical Necessity:

- By defining these points, we enable a Co-Design environment where the connector vendor owns the CPC pad parasitic effects, and the PKG vendor owns the trace performance.



CPC channel (PKG model)
TP0d~TP0p/TP5d~TP5p

COM PKG model assumption
- Cp = 0 fF (no CPC pad)
- zp1 = via height (BU via)
- zp2 = trace length
(physical order)

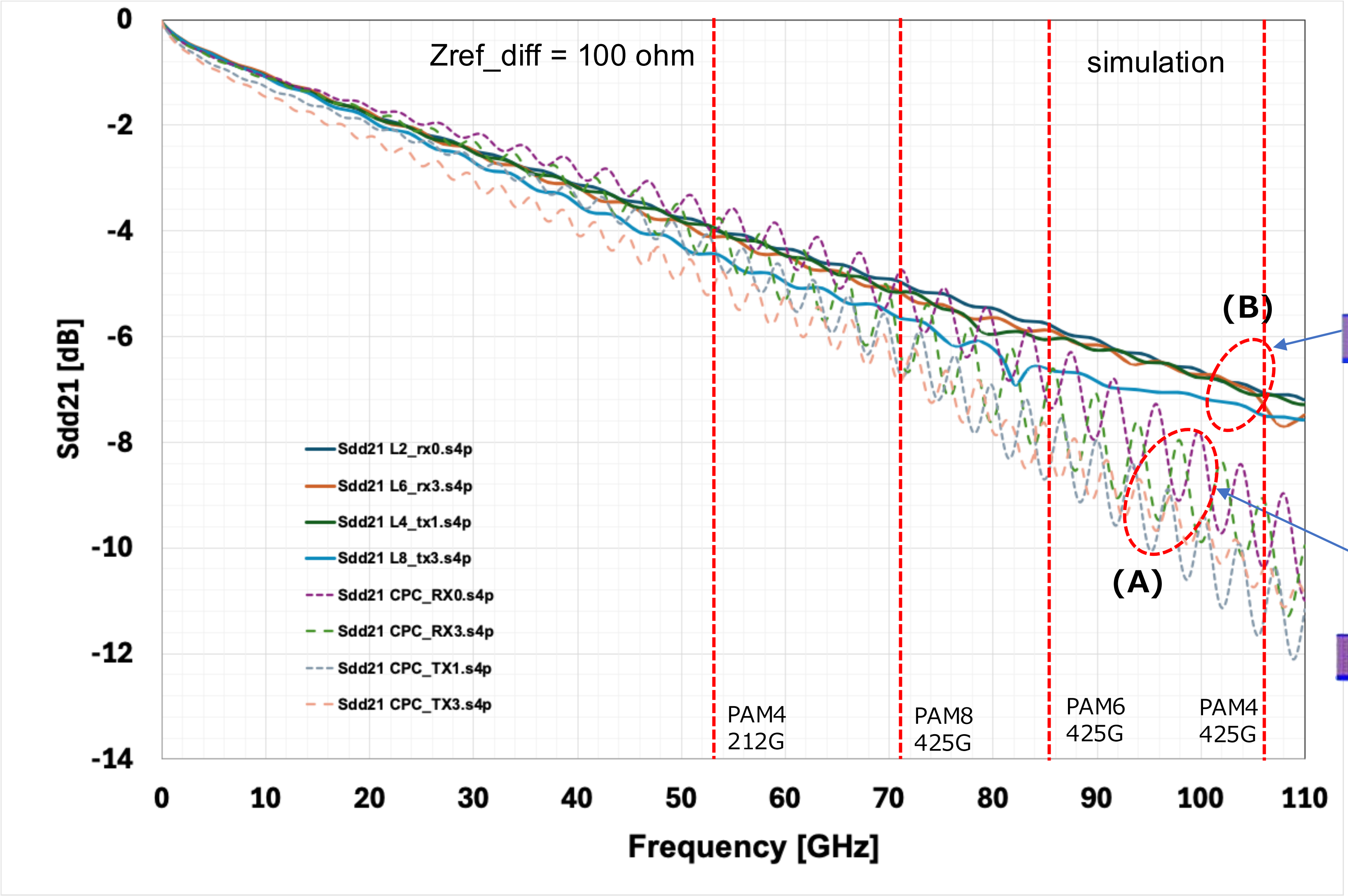
“part” of CPC channel model
- including
  - PKG CPC breakout
    ~1mm from boundary
  - PKG CPC pad (430um diameter)

TP0p
- CPC boundary is included in CPC channel model.
- ~1mm PKG trace included

TP5p

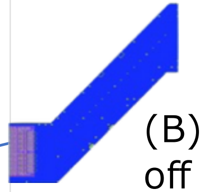
C.3 Excluding Measurement Effects

	RF probe pad	CPC pad/ breakout	bump pad	PKG channel
(A)	no	yes	yes	TP0d/TP5d ~ TP0p/TP5p
(B)	no	no	yes	TP0d/TP5d ~ TP0/TP5

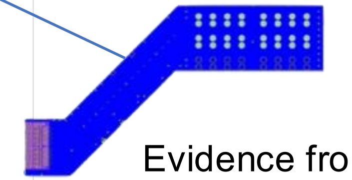


trace length [mm]

trace	(A)	(B)
L2_rx0	19.6	16.9
L6_rx3	19.5	15.8
L4_tx1	23.3	16.5
L8_tx3	25.2	16.0



(B) **Without CPC pad**, no significant roll off is observed even with bump pad.



(A) Without RF probe pad and **with CPC pad**, significant roll off is still observed.

Evidence from Model (B):

- When the CPC pad is removed (Model B), the insertion loss follows a standard linear-root frequency roll-off:

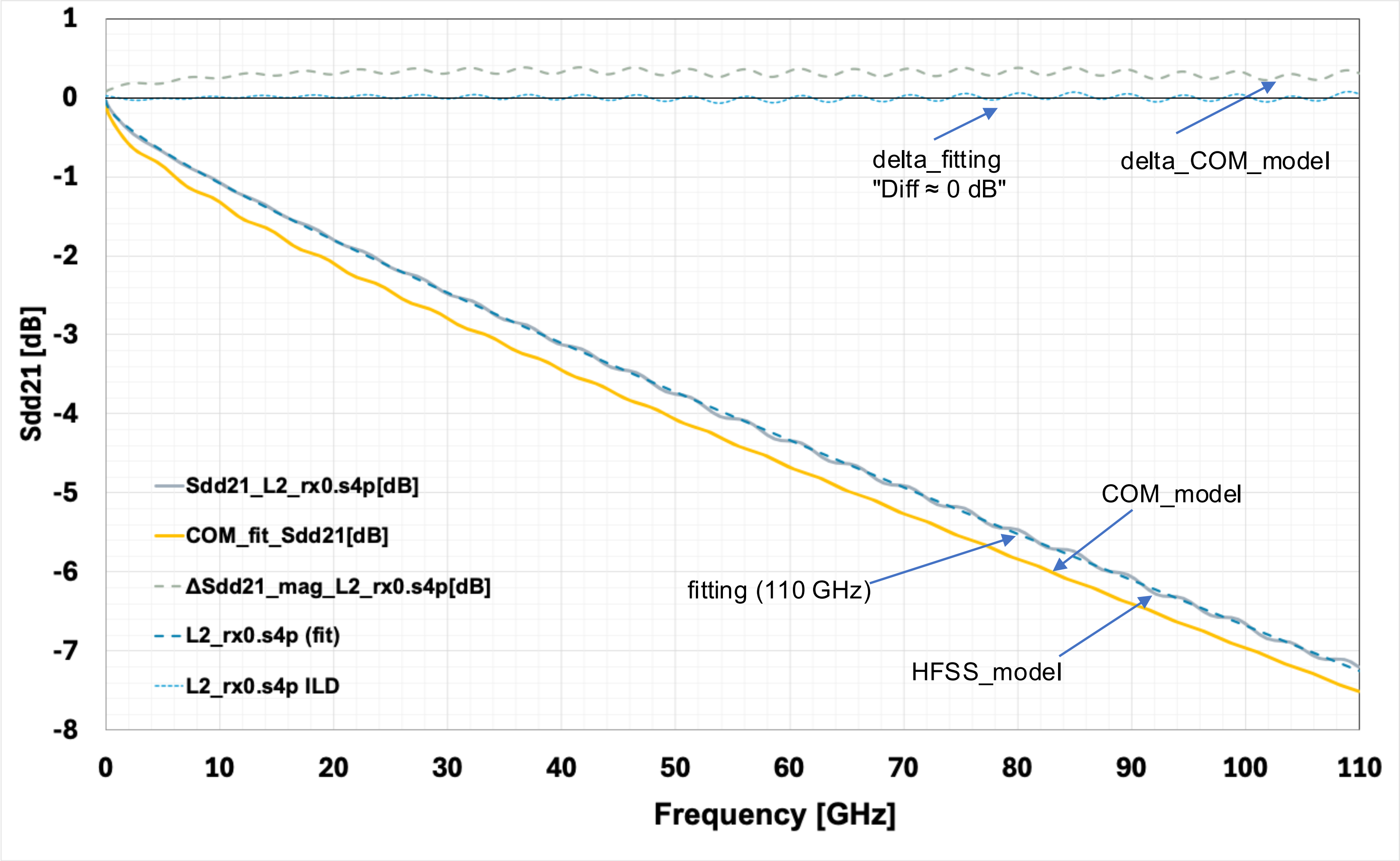
- Agreement is within up to 110 GHz, proving that dispersion and dielectric loss are the only significant factors for the trace itself.

D. COM PKG model Assumptions and Scope

- Setting **Cp = 0 fF** is necessary to decouple the frequency-dependent interface transfer function (including radiation and mode conversion from intrinsic substrate trace.).
- **Boundary**: PKG COM model defined from TP0/TP5 to tentative TP0p/TP5p.
- **Applicable**: Intrinsic PKG trace evaluation and fair COM comparison.
- **Not applicable**: Models including CPC pad, CPC breakout, or CPC mating transitions.
  - This means TP0d/TP5d to CPC pad part in PKG will be included in “CPC channel model”.
  - It is crucial for PKG designers to work tightly with CPC vendors.
  - In OIF, CPC/CPO connector standardization direction is now under discussion.
  - Once CPC footprint is standardized, co-modeling (CPC pad, CPC breakout, or CPC mating transitions) will be much easier and feasible.
- B**enefit**: Avoids over-pessimistic COM caused by measurement and simulation artifacts.
  - Modeling only PKG portion will not work in this frequency range.

D.1 COM PKG model (CPC, TP0d/5d~TP0p/5p)

For “generic” COM PKG model generation, it is necessary to gather more data, and set appropriate parameters.
- material, manufacturing process, and design dependency



(1) Use physical size of trace (zp2) and via (zp1)
(2) Use some parameters from class B PKG:
Zc1, Zc2, gamma_0, a1, and tau.
(3) Sweep a1 to fit HFSS model.
(4) Cp = 0fF, as there is no CPC pad at TP0p/TP5p.

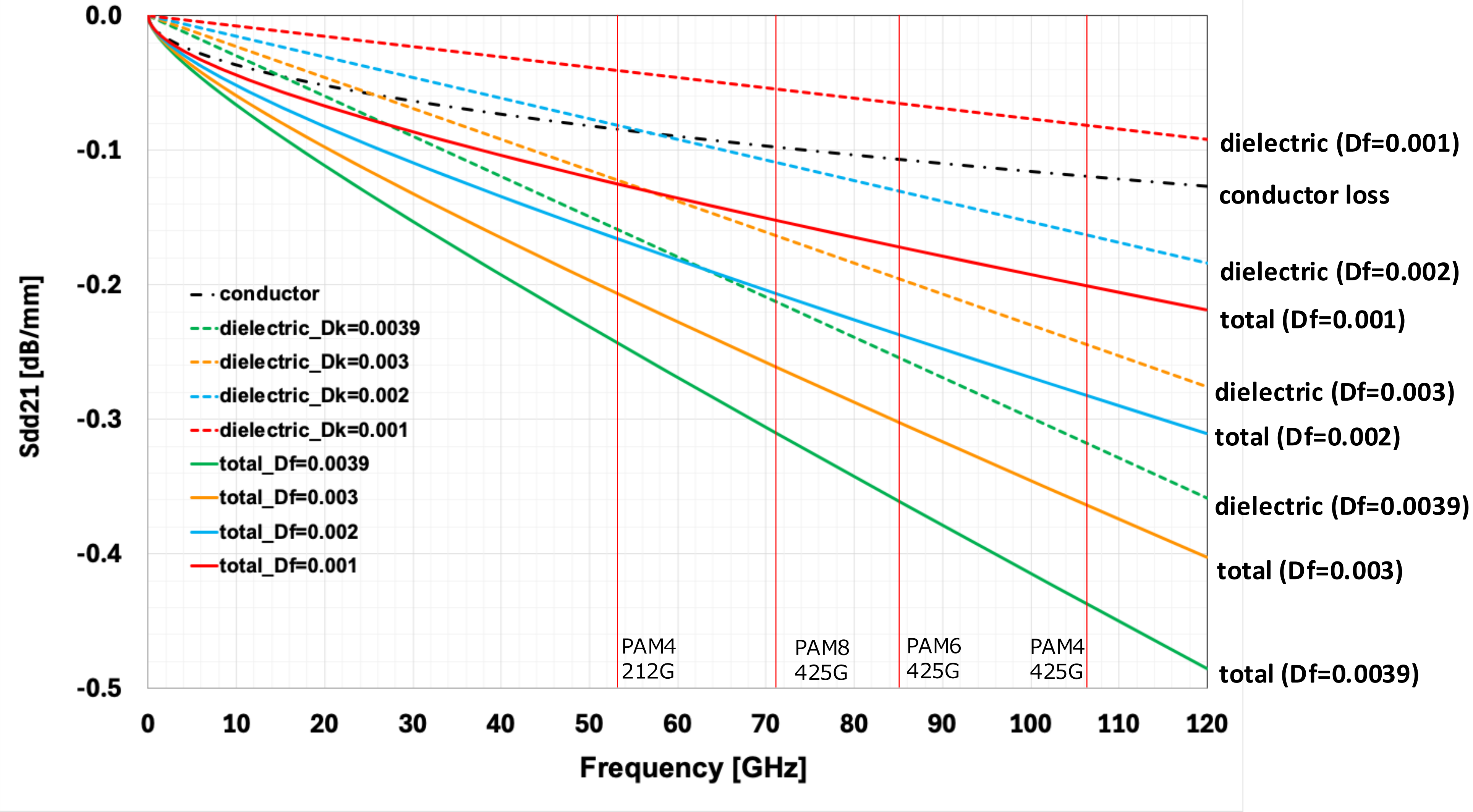
	Cp	Zc1	zp1	Zc2	zp2	Zc3	zp3	Zc4	zp4
trace	[fF]	[ohm]	[mm]	[ohm]	[mm]	[ohm]	[mm]	[ohm]	[mm]
L2_rx0	0	95	0.045	87.5	16.9	95	0	100	0
L6_rx3	0	95	0.225	87.5	15.8	95	0	100	0
L4_tx1	0	95	0.135	87.5	16.5	95	0	100	0
L8_tx3	0	95	0.315	87.5	16.0	95	0	100	0

PKG model	gamma_0	a1	a2	tau
unit	[1/mm]	[ns$^{1/2}$ /mm]	[ns /mm]	[ns /mm]
class A	5.00E-04	8.90E-04	2.00E-04	6.141E-03
class B	5.00E-04	6.50E-04	2.93E-04	6.141E-03
CPC	5.00E-04	1.725E-03	2.93E-04	6.141E-03

delta_COM_model = HFSS_model – COM_model
delta_fitting = HFSS_model - fitting

E. Material Sensitivity

For the PKG traces, reduction of Df is effective.
Further work is on going.



CPC PKG model
(no CPC pad)
16mm trace (L2/4/6)

This estimation is based on the fitting coefficient.

fitting function

$$Sdd21_{fit} = \underbrace{a1 \cdot f^{0.5}}_{\text{conductor}} + \underbrace{a2 \cdot f}_{\text{dielectric}}$$

- Simply scale “a2”, relative to original Df=0.0039*.
- Same conductor loss “a1” is used.

* Df=0.0039 number is at 85C.
- Larger than room temperature number.

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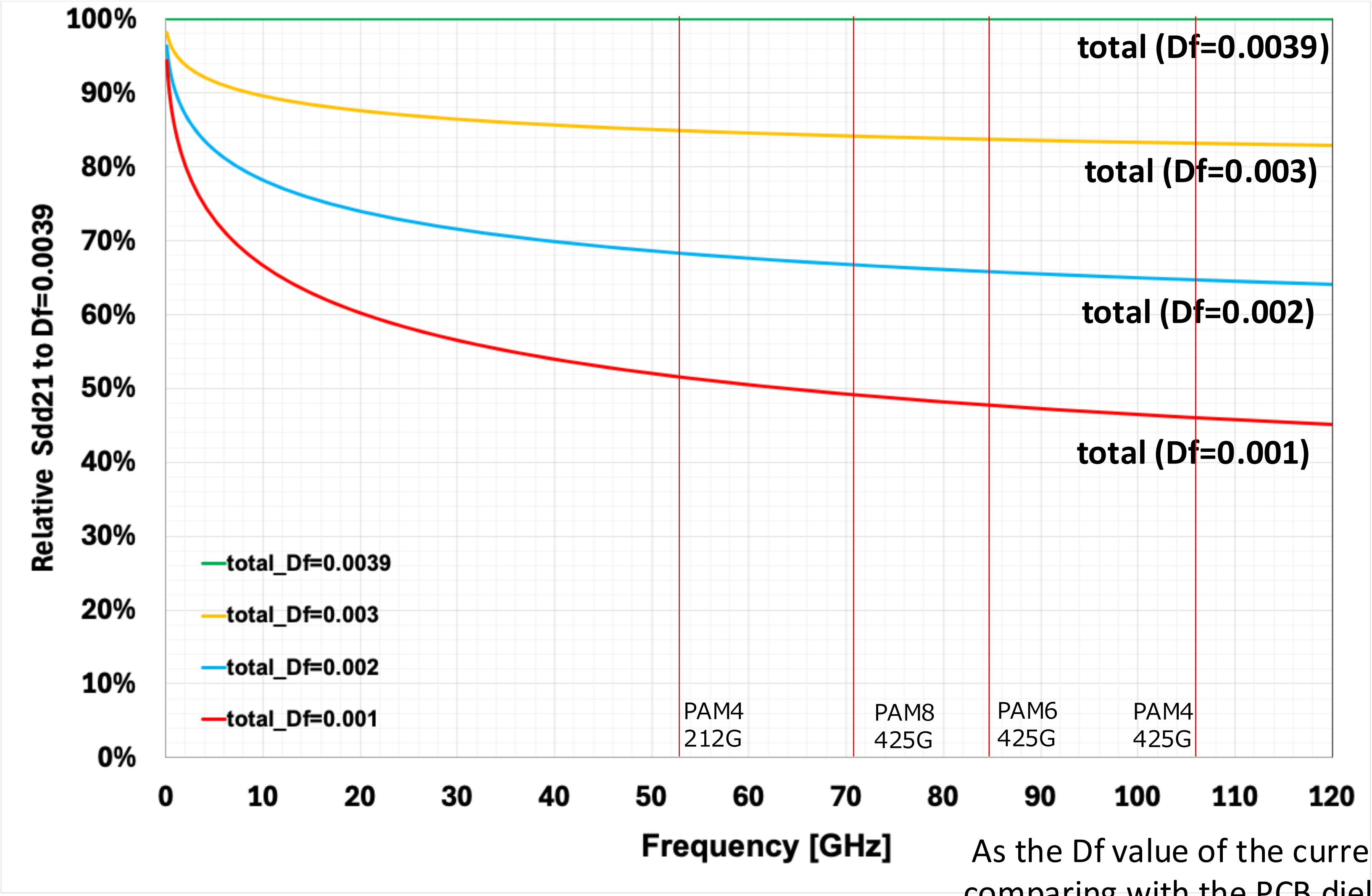

CPC PKG model (no CPC pad)
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- Simply scale “a2”, relative to original Df=0.0039*.
- Same conductor loss “a1” is used.

* Df=0.0039 number is at 85C.
- Larger than room temperature number.

As the Df value of the current PKG dielectric material is relatively high comparing with the PCB dielectric material, Df reduction is effective.

With low Ra Cu and treatment, conductive loss is relatively small comparing with dielectric loss.

Thank you!

Questions?

contact: sakai.toshiaki@socionext.com