Considerations for Electrical Interfaces Beyond 200Gb/s per lane (*Revisited*)

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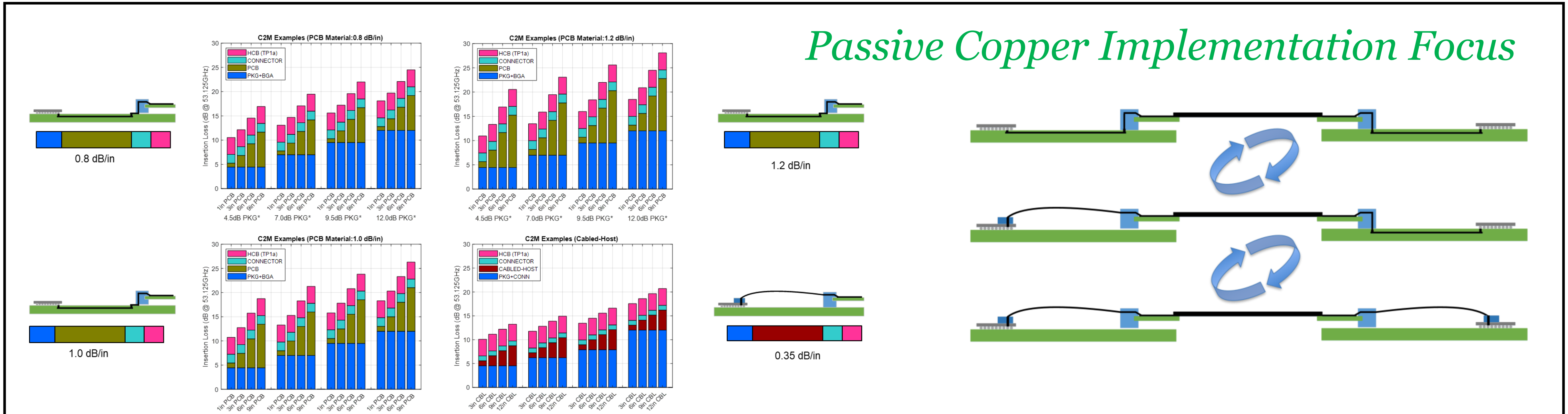
We have a Copper Cable Objective!

Actually, (3)...

- Define a single-lane, 400Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter.
- Define a two-lane, 800Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter.
- Define a four-lane, 1.6Tb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter.

Motivation

- Goal: To stimulate discussion related to Copper Cable Objectives
- Assumptions: Data rate, modulation, form factor are unknown



From Kocsis_b400g_01a_210826

Beyond 200Gb/s per lane…

	"224G"				"448G"		
Number of signal levels (M)	8	6	4		8	6	4
Bits per symbol	3	2.5	2		3	2.5	2
Signaling rate*, GBd	75	90	112		150	180	224
Nyquist frequency, GHz	37.5	45	56	…	75	90	112

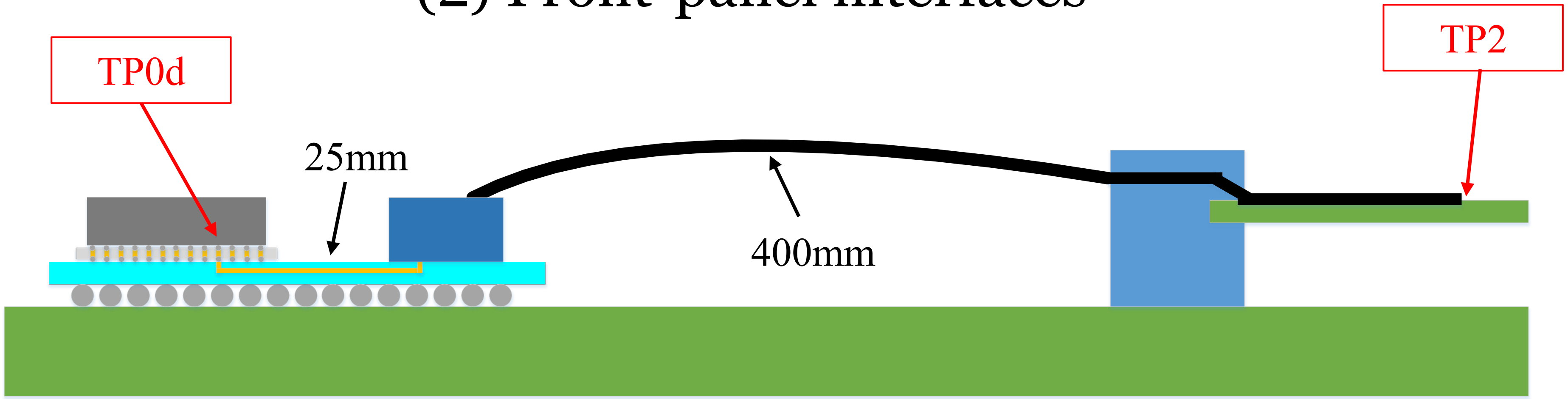
* Signaling rate rounded for simplicity

For now, we can evaluate trade-offs of channel performance (bandwidth) at a per lane basis

From Kocsis_e4ai_01_250327

Defining the Electrical Interface

At 200Gb/s per lane there are two bottlenecks in need of attention:
(1) Chip package breakout
(2) Front-panel interfaces

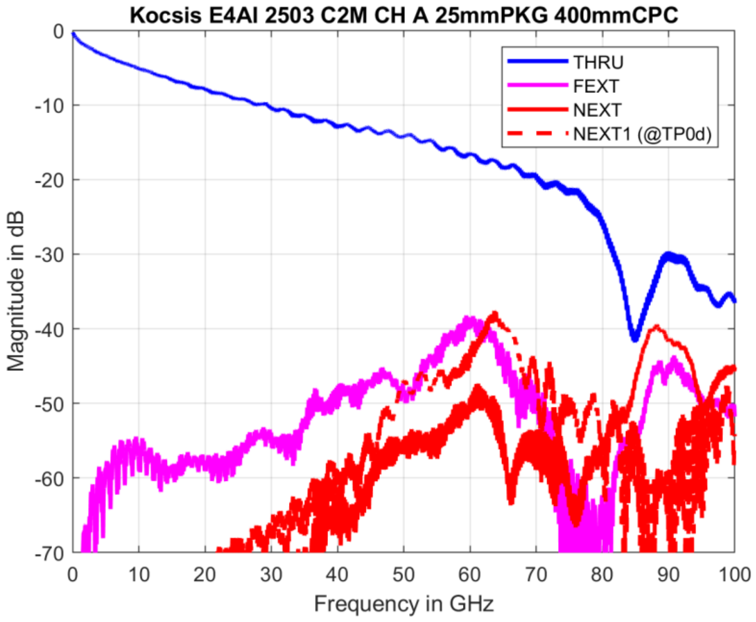


The channels in this contribution will focus on implementation options for the topology above.

- Die-to-Package-to-Connector is a real, manufacturable model, not lumped elements
- Module interface options are swapped ("A,B,C") to highlight different performance profiles
- Module ends at TP2, no coax point, or module package

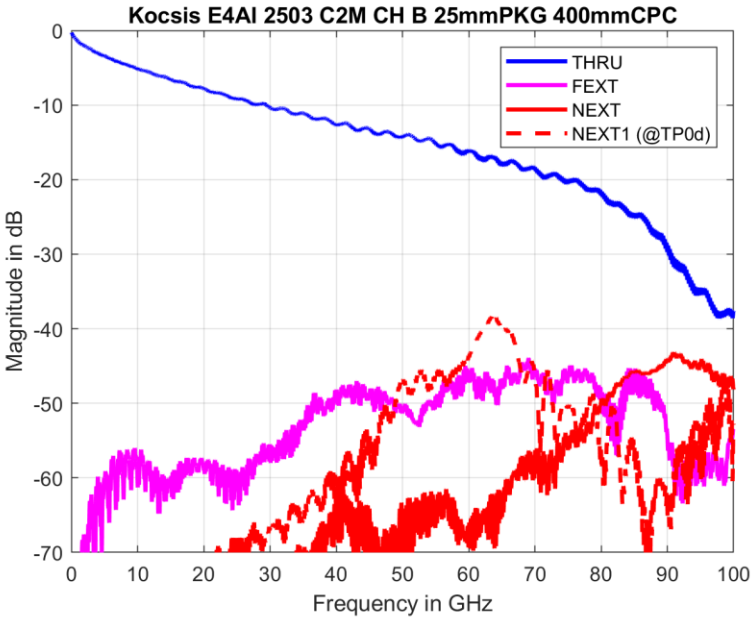
From Kocsis_e4ai_01_250327

Ethernet for AI - Interconnect Options



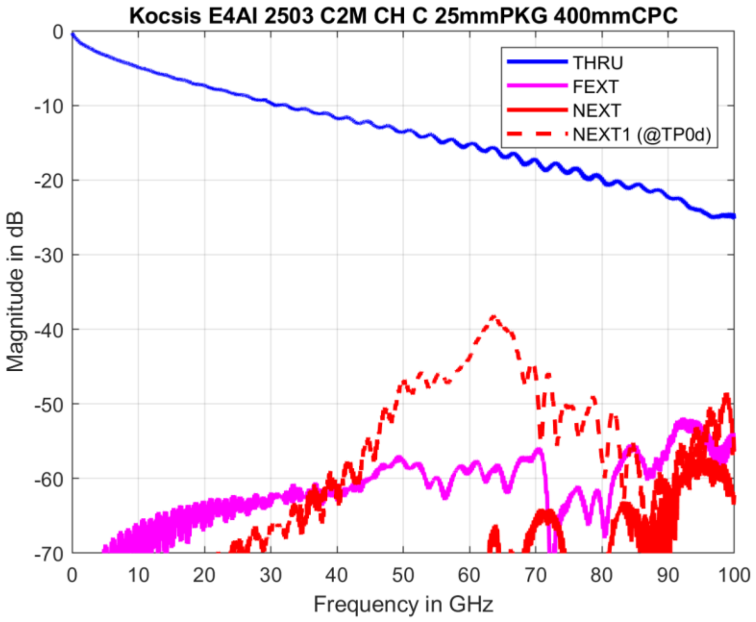
Channel A

“Limit of today’s Pluggable”



Channel B

“New Pluggable, Familiar Feel”



Channel C

“New Pluggable, New Paradigm”

From Kocsis_e4ai_01_250327

Ethernet for AI - Interconnect Options

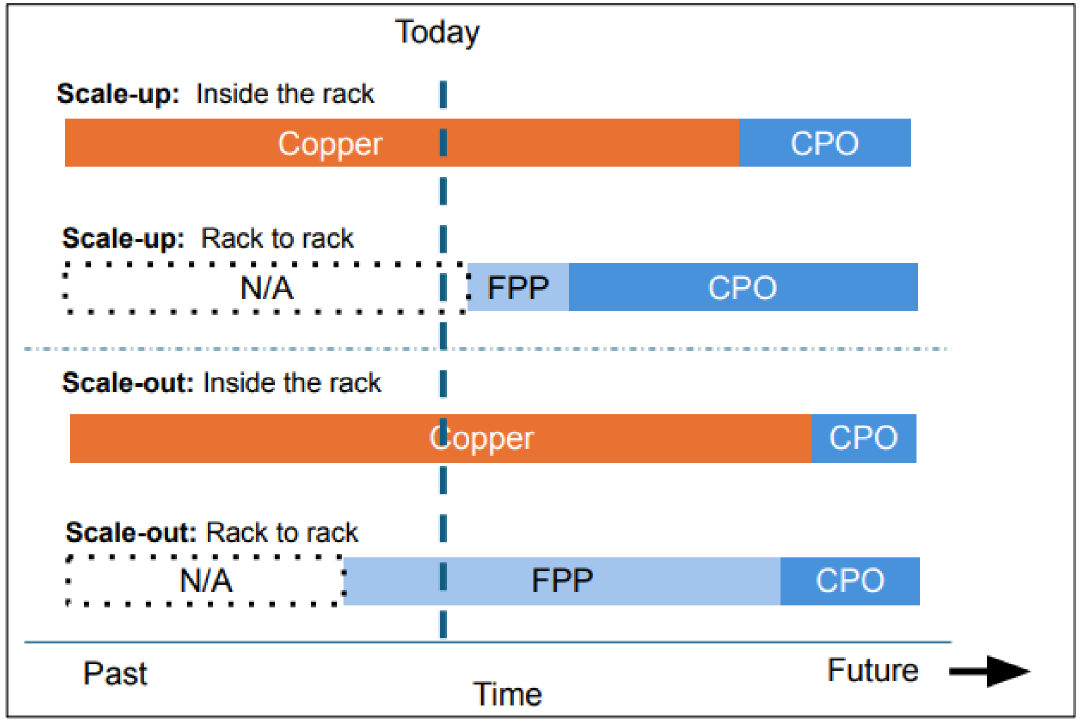
	Channel A	Channel B	Channel C	Comments
Backwards Compatible	++	-	-	**Mechanical** compatibility not required
Interface Bandwidth	85 GHz	95 GHz	100 GHz+	At least 130GHz modeled bandwidth
Crosstalk	-	-	-	Package *must* improve, Connector *should*
Supported Modulation	PAM-8	PAM-8/6	PAM-8/6/4	Channel C preferred for all signaling rates
HVM Readiness	++	+	-	Time to market is critical
Form Factor TTM	2Q	3Q	6Q	As a “standard” solution

Channel performance has and will likely continue to improve throughout the Study Group and Task Force phases of the project

The optimal paths forward for Copper Cable and Optical Modules may be different

Ethernet for AI – Passive Copper

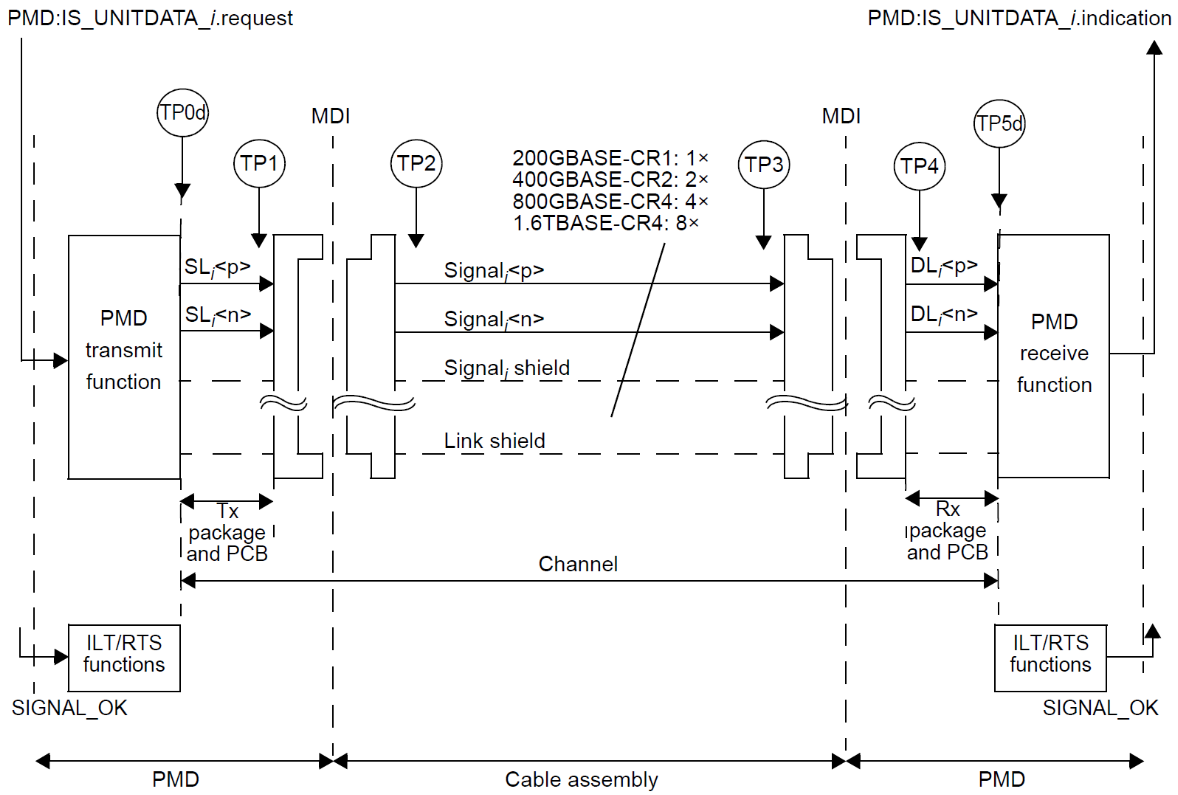
- (3) Types of Networks
  - Front-End / Traditional
  - Back-End / Scale-up intra-rack
  - Back-End / Scale-out intra-rack
- Bandwidth Density is critical
- Interconnect requirements are
  - Modular compatibility unknown
  - Architectural compatibility unknown
  - Latency/Power critical



Based on AI Networking: What do scaleup and scaleout really mean for networking demand, Alan Weckel (650 Group), https://www.ieee802.org/3/ad_hoc/E4AI/public/25_0327/weckel_e4ai_01_250327.pdf

Standardizing Passive Copper Cabling

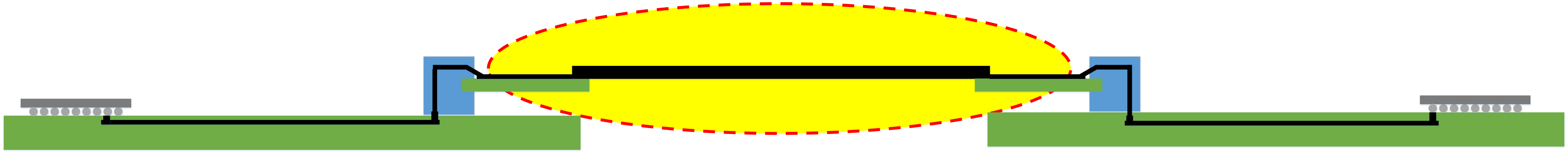
- Reference channel
  - Reference Tx/Rx
  - Reference termination
  - Reference package
  - Reference host
- Host / Interconnect performance defined at measurable test points
- MDI *was* critical to map the connection between independent and unaware PMDs



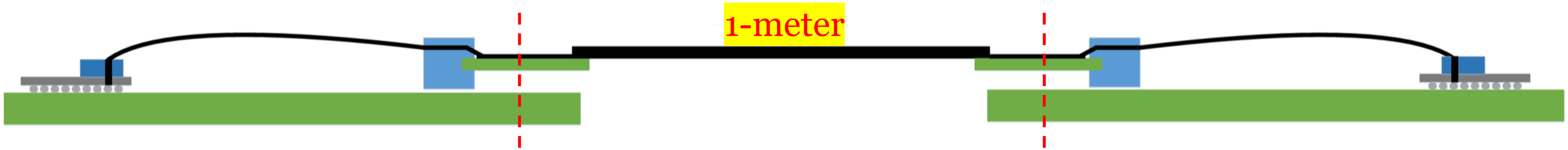
NOTE 1—The source lane (SL) signals SL_i<p> and SL_i<n> are the positive and negative sides of the transmitter's differential signal pair on lane *i* and the destination lane (DL) signals DL_i<p> and DL_i<n> are the positive and negative sides of the receiver's differential signal pair on lane *i*.
NOTE 2—The test points TP1, TP2, TP3, and TP4 are associated with test fixtures as described in Table 179–6.

Standardizing Passive Copper Cabling

- Goal: To define methodology for compliant cable assemblies



Some topologies have more than one cable assembly…



The critical requirements remain focused on the host(s) input/output and the cable assembly

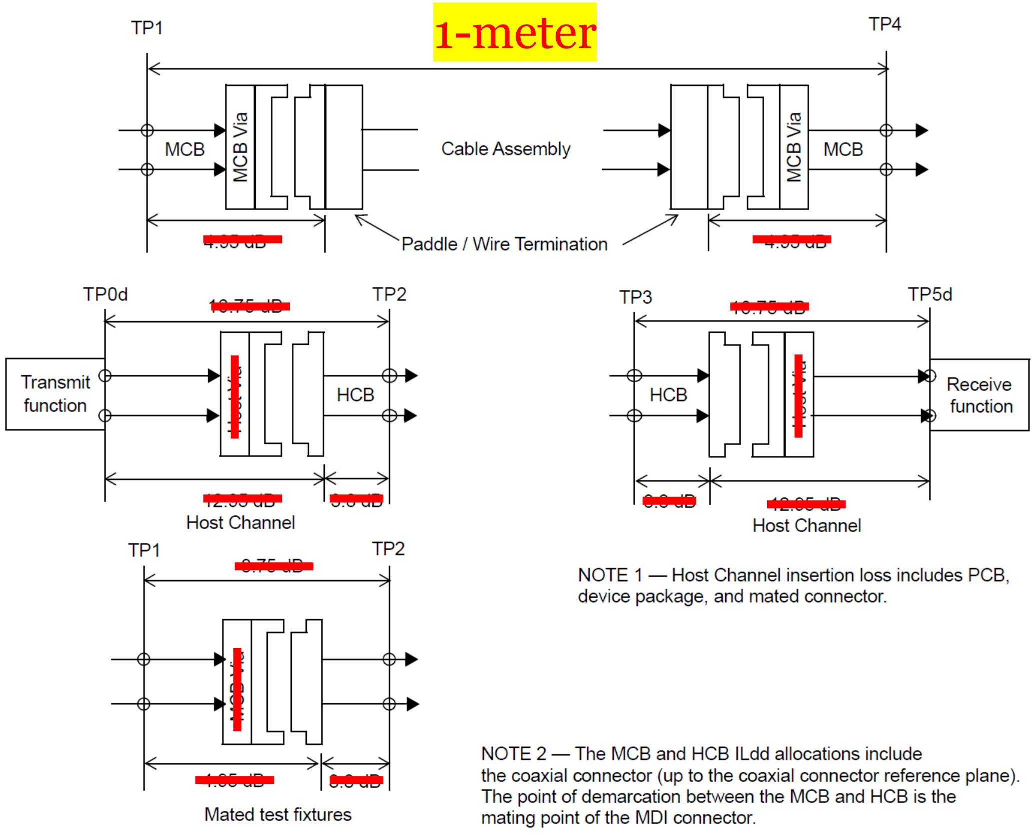
Standardizing Passive Copper Cabling

- Both Hosts and Cable assemblies have "classes"
- *All* Hosts are <u>not</u> compatible with *all* Cable assemblies
- Knowledge of the full link is common for passive copper cabling
- *CR* deployments …resembling *KR*

Cable assembly class	Host classes, transmitter side	Host classes, receiver side	Number of combinations
CA-A	HN or HL	HL, HN, or HH	6
	HH	HL or HN	2
CA-B	HL	HL, HN, or HH	3
	HN	HL or HN	2
	HH	HL	1
CA-C	HL	HL or HN	2
	HN	HL	1
CA-D	HL	HL	1

Standardizing Passive Copper Cabling

- End-to-End Loss Budget
  - Reference package
  - Reference host
  - 1-meter cable assembly
- Mapping of the Tx/Rx to the Host I/O interface may incorporate a variety of implementations
- 400GPL passive copper likely to include cabled-backplane



MCB = Module Compliance Board, 179B.3
HCB = Host Compliance Board, 179B.2
MCB Via = transition via to MDI connector on an MCB
Host Via = transition via to MDI connector on a Host Channel
Paddle/Wire Termination = transition structure(s) in a Cable Assembly not present on an HCB

Definition of the MDI

- Lane mapping from the package to the Host I/O interface may be different for the same interface depending on application
- Are we providing a spec, or just an example?
- MDIs only defined for copper PMDs (currently)

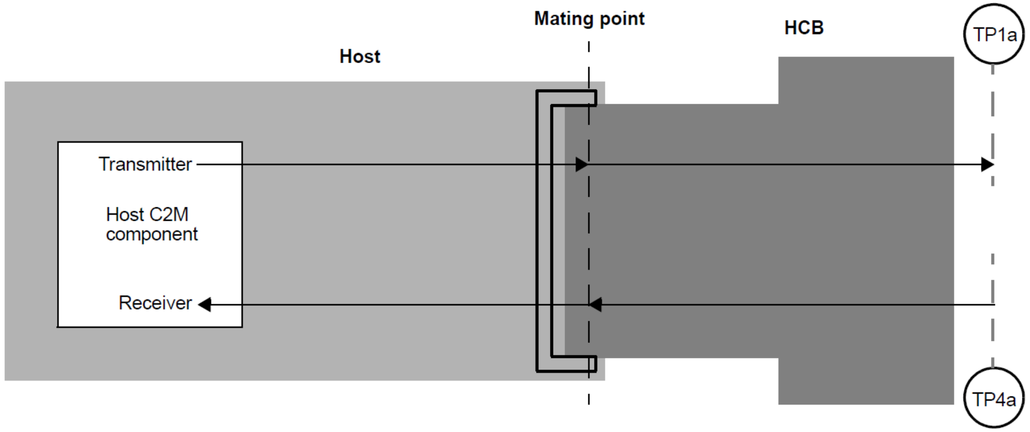
Table 179C–2—PMD to connector signal assignments

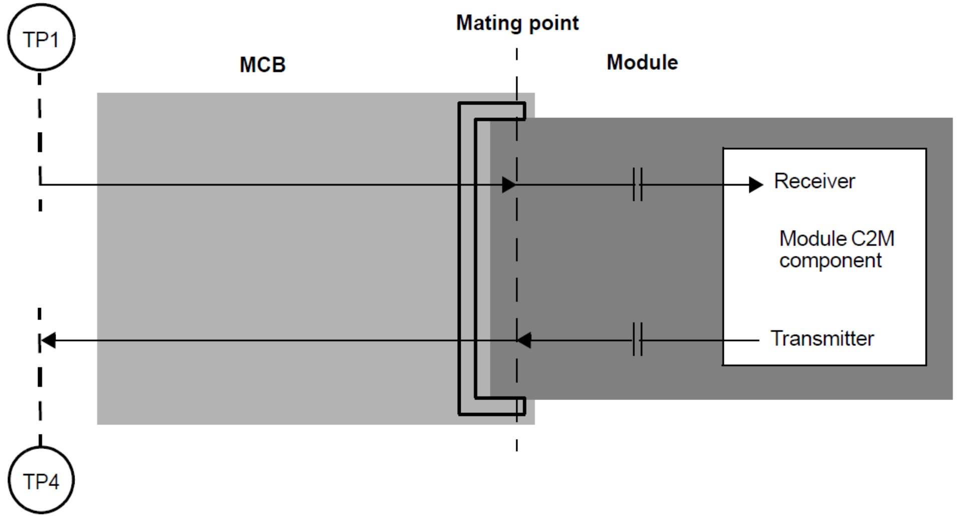
PMD signal <PMD number>:<PMD signal>				
200GBASE-CR1	400GBASE-CR2	800GBASE-CR4	1.6TBASE-CR8	Connector signal
0:DL0n	0:DL0n	0:DL0n	0:DL0n	DL0n
0:DL0p	0:DL0p	0:DL0p	0:DL0p	DL0p
1:DL0n	0:DL1n	0:DL1n	0:DL1n	DL1n
1:DL0p	0:DL1p	0:DL1p	0:DL1p	DL1p
2:DL0n	1:DL0n	0:DL2n	0:DL2n	DL2n
2:DL0p	1:DL0p	0:DL2p	0:DL2p	DL2p
3:DL0n	1:DL1n	0:DL3n	0:DL3n	DL3n
3:DL0p	1:DL1p	0:DL3p	0:DL3p	DL3p
4:DL0n	2:DL0n	1:DL0n	0:DL4n	DL4n
4:DL0p	2:DL0p	1:DL0p	0:DL4p	DL4p
5:DL0n	2:DL1n	1:DL1n	0:DL5n	DL5n
5:DL0p	2:DL1p	1:DL1p	0:DL5p	DL5p
6:DL0n	3:DL0n	1:DL2n	0:DL6n	DL6n
6:DL0p	3:DL0p	1:DL2p	0:DL6p	DL6p
7:DL0n	3:DL1n	1:DL3n	0:DL7n	DL7n
7:DL0p	3:DL1p	1:DL3p	0:DL7p	DL7p
0:SL0n	0:SL0n	0:SL0n	0:SL0n	SL0n
0:SL0p	0:SL0p	0:SL0p	0:SL0p	SL0p
1:SL0n	0:SL1n	0:SL1n	0:SL1n	SL1n
1:SL0p	0:SL1p	0:SL1p	0:SL1p	SL1p
2:SL0n	1:SL0n	0:SL2n	0:SL2n	SL2n
2:SL0p	1:SL0p	0:SL2p	0:SL2p	SL2p
3:SL0n	1:SL1n	0:SL3n	0:SL3n	SL3n
3:SL0p	1:SL1p	0:SL3p	0:SL3p	SL3p
4:SL0n	2:SL0n	1:SL0n	0:SL4n	SL4n
4:SL0p	2:SL0p	1:SL0p	0:SL4p	SL4p
5:SL0n	2:SL1n	1:SL1n	0:SL5n	SL5n
5:SL0p	2:SL1p	1:SL1p	0:SL5p	SL5p
6:SL0n	3:SL0n	1:SL2n	0:SL6n	SL6n
6:SL0p	3:SL0p	1:SL2p	0:SL6p	SL6p
7:SL0n	3:SL1n	1:SL3n	0:SL7n	SL7n
7:SL0p	3:SL1p	1:SL3p	0:SL7p	SL7p

OSFP1600	Connector signal name	Description
1	GND	Ground
2	SL1p	Transmitter non-inverted data input
3	SL1n	Transmitter inverted data input
4	GND	Ground
5	SL3p	Transmitter non-inverted data input
6	SL3n	Transmitter inverted data input
7	GND	Ground
8	SL5p	Transmitter non-inverted data input
9	SL5n	Transmitter inverted data input
10	GND	Ground
11	SL7p	Transmitter non-inverted data input
12	SL7n	Transmitter inverted data input
13	GND	Ground
18	GND	Ground
19	DL6n	Receiver inverted data output
20	DL6p	Receiver non-inverted data output
21	GND	Ground
22	DL4n	Receiver inverted data output
23	DL4p	Receiver non-inverted data output
24	GND	Ground
25	DL2n	Receiver inverted data output
26	DL2p	Receiver non-inverted data output
27	GND	Ground
28	DL0n	Receiver inverted data output
29	DL0p	Receiver non-inverted data output
30	GND	Ground
31	GND	Ground
32	DL1p	Receiver non-inverted data output
33	DL1n	Receiver inverted data output
34	GND	Ground
35	DL3p	Receiver non-inverted data output

Definition of the MDI

- MDI definition is most helpful for form factors combining passive copper and optical functions into a single interface
- MDI for AUI is not form factor specific/limited
    - SFP (as example)
    - OSFP-XD (as example)
    - XPO (as example)

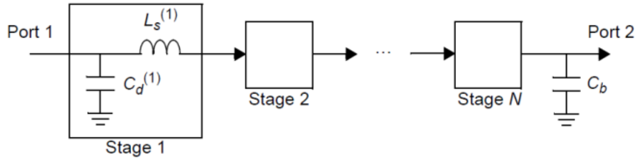




Considerations Moving Forward

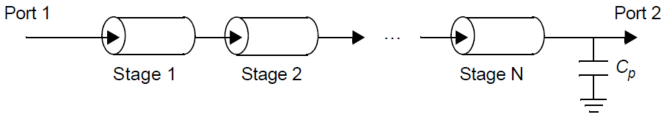
- What is critical for IEEE?

Reference Termination

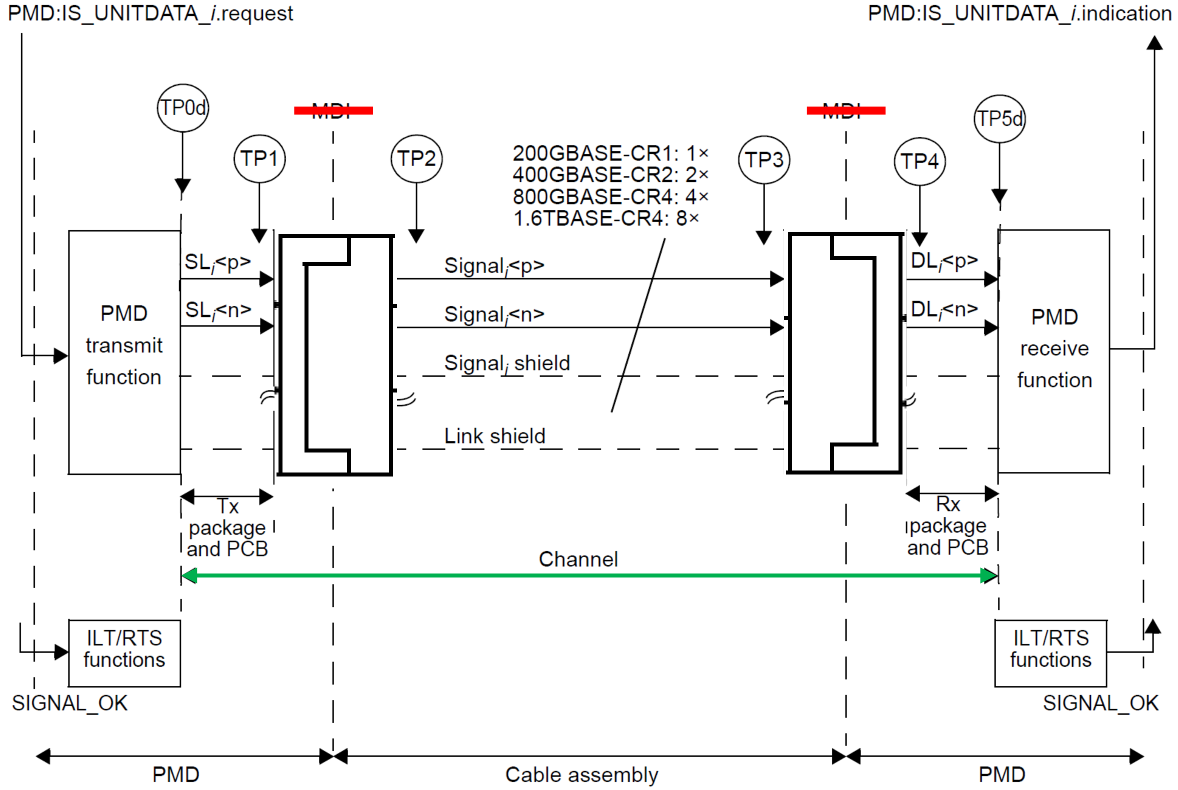


Helps target impedance requirements

Reference Package



Leave flexibility for Host to trade off implementation options



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Summary / Discussion

- Goal: To stimulate discussion related to Passive Copper Objectives

- Future contributions TP0d-TP5d, TP0d-Tp2, TP3-TP5d are expected
- …alignment on the reference termination is beneficial to all
- …alignment on model bandwidth is helpful for comparisons
- …are new test points needed?

- Definition of the test points, test fixtures is critical
- …is the MDI definition critical to the success of the Passive Copper?